Impact of the interface layer on the cycling behaviour and retention of ferroelectric hafnium oxide

Maximilian Lederer¹ · Konstantin Mertens¹ · Alireza M. Kia¹ · Jennifer Emara¹ · Ricardo Olivo¹ · Yannick Raffel¹ · David Lehninger¹ · Tarek Ali¹ · Kati Kühnel¹ · Konrad Seidel¹ · Thomas Kämpfe¹ · Lukas M. Eng²

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Abstract

Reliability is a central aspect of hafnium oxide-based ferroelectric field effect transistors (FeFETs), which are promising candidates for embedded non-volatile memories. Besides the device performance, understanding the evolution of the ferroelectric behaviour of hafnium oxide over its lifetime in FeFETs is of major importance for further improvements. Here, we present the impact of the interface layer in FeFETs on the cycling behaviour and retention of ferroelectric silicon-doped hafnium oxide. Thicker interfaces are demonstrated to reduce the presence of antiferroelectric-like wake-up effects and to improve endurance. However, they show a strong destabilisation of one polarisation state in terms of retention. In addition, measurements of the Preisach density revealed additional insight in the wake-up effect of these metal-ferroelectric-insulator-semiconductor (MFIS) capacitors.

Introduction

Ferroelectric field effect transistors based on hafnium oxide have become a viable option as embedded non-volatile memory solution due to their high coercive field as well as their compatibility to complementary metal-oxide-semiconductor (CMOS) processes [1]. In comparison to ferroelectric capacitors, these devices comprise an additional interface layer, which impacts the electrical field distribution in the gate stack and yields a depolarisation field counteracting the polarisation of the ferroelectric, affecting properties like endurance and retention [2, 3]. In consequence, this is expected to affect the wake-up behaviour of the hafnium oxide layer. This has recently been underlined by structural and electrical characterisation of silicon-doped HfO₂ (HSO) in metal-ferroelectric-insulator-semiconductor (MFIS) stacks [4–6]. These layers exhibited pronounced $\langle 110 \rangle$ and $\langle 111 \rangle$ out-of-plane textures for the ferroelectric orthorhombic phase as well as dendritically shaped grains [5]. This is in stark contrast to commonly investigated capacitor structures,

which have been reported to consist of disc-shaped grains with $\langle 100 \rangle$ out-of-plane textures [7–9]. Furthermore, the polarisation hysteresis behaviour ranged from ferroelectric to strongly asymmetric antiferroelectric (AFE)-like behaviour [4, 6]. Additionally, it has been reported that the interface layer is changing in thickness and chemical composition during the dopant activation and crystallisation anneal of the ferroelectric [4, 5]. How this affects the cycling behaviour as well as retention of ferroelectric HSO layers in MFIS stacks is investigated in this article.

Experimental

To investigate the cycling behaviour in HSO-based MFIS capacitors, a controlled chemical oxidised interface with a thickness of 1.2 ± 0.2 nm is formed on highly-doped 300 mm Si wafers. The 10 nm hafnium oxide layer is deposited using atomic layer deposition with HfCl₄ and SiCl₄ precursors (16:1 cycling ratio). Afterwards, a 10 nm TiN layer is added by physical vapour deposition. Crystallisation anneals are performed with rapid thermal annealing (RTA) at 650 °C, 800 °C, and 1000 °C, respectively.

For a more detailed study of the interface layer influence on retention, the thickness of the interface layer is modified prior to hafnium oxide deposition by rapid thermal oxidation, resulting in a thickness of 2.7 ± 0.3 nm and

✉ Maximilian Lederer
maximilian.lederer@ipms.fraunhofer.de

¹ Fraunhofer IPMS, An der Bartlake 5, Dresden 01109, Germany

² Institut für Angewandte Physik, Technische Universität Dresden, Nöthnitzer Straße 61, Dresden 01187, Germany

3.7 ± 0.4 nm, respectively. These samples as well as a reference sample with chemical oxidised interface are annealed at 650°C . No significant interface growth is expected at this temperature [4].

Dynamic hysteresis measurements are performed using an aixACCT TF 3000 Analyser at a frequency of 1 kHz. Electric field cycling was performed under identical conditions. In addition, Preisach densities were measured using first-order reversal (FORC) measurements with a maximum bias of ± 4.5 V. Grazing-incident X-ray diffraction (GIXRD) patterns were recorded using a Bruker D8 Discover XRD system scanned over the 2θ range from 15° to 45° at a fixed incident angle of 0.5° . In order to extract retention behaviour of these samples, a polarisation state is written and after a certain time, a positive-up-negative-down (PUND) measurement is performed, with a preceding X pulse applied in the same direction as the write pulse. Retention loss (P_{loss}) is extracted by normalising the difference of initial polarisation of the X pulse (P_X) and remanent polarisation P_R to the full $2P_R$ extracted from the PUND measurement. Loss of P_{R+} is given as $1 - P_{\text{loss}}$, loss of P_{R-} is given as P_{loss} and triangular signal is pulsed from the bottom.

Results and discussion

The resulting stack structure of the MFIS samples is given in Fig. 1a. Here, the interface growth during crystallisation is clearly visible in case of the 1000°C RTA. Temperature dependent interface growth has been reported previously for Si and SiGe substrate as well [4, 5]. For the latter, an interface thickness of 0.67 nm and 1.99 nm for 650°C and 1000°C has been reported, respectively [4]. As a result, electrical behaviour of samples annealed at different temperatures differs strongly, as depicted in Fig. 1b and c. While the sample annealed at 1000°C (Fig. 1c) behaves already ferroelectric at the beginning, the slope of the hysteresis becomes much steeper during wake-up, and can be therefore

classified as non-split wake-up [6]. Samples annealed at lower temperatures on the other hand show an asymmetric wake-up [6]. Here, the pinching of the hysteresis is reduced with cycling, resulting in a more ferroelectric behaviour (see Fig. 1b).

More detailed insight into the evolution of the switching behaviour during wake-up can be gained by investigating the Preisach density using FORC measurements. The sample annealed at 800°C shows initially three clear peaks (see Fig. 2). In contrast to metal-ferroelectric-metal (MFM) capacitors, these do not form an isosceles triangle nor do they have a mirror axis along the dashed diagonal (see Fig. 2) [10, 11]. This distortion is most likely a result of the non-linear capacitance of the substrate and/or defect in the interface layer. In addition, band alignment can shift the triangle from the central diagonal. However, after cycling (Fig. 2) a very different Preisach density is observed. In contrast to ferroelectrics, where only one peak is present, two peaks are observed here. The lower distorted one is most likely the ferroelectric one. The upper one, however, would fit to an antiferroelectric-like peak, but is missing its twin. This results in a peculiar behaviour, being ferroelectric in one direction, but antiferroelectric-like in the other one. This behaviour is currently not fully understood, but with the recent proof of ferroelastic switching in polycrystalline hafnium oxide films [6], this is most likely a result of interplay of mechanical stress, band alignment, non-linear silicon capacitance, and defects in the interface layer.

For the sample annealed at 1000°C on the other hand, two peaks appear initially (Fig. 2) even though it appears ferroelectric in the dynamic hysteresis measurement (Fig. 1c). The additional faint dark blue line is most likely a measurement artefact. Upon cycling these peaks merge and a purely ferroelectric behaviour is observed (Fig. 2). This suggests the presence of ferroelastic switching and reduction of stress during the first cycles of non-split wake-up.

Besides differences in the wake-up behaviour, differences in the endurance can be observed as well (see Fig. 3). Earlier

Fig. 1 Structural and electrical characterisation of MFIS stacks. **a** Transmission electron microscopy (TEM) image of 1000°C annealed HSO MFIS cross section. Evolution of the polarisation hysteresis

upon electric field cycling for samples annealed at 800°C (**b**) and 1000°C (**c**). An AFE-like behaviour is observed for 800°C

Fig. 2 FORC measurements of samples annealed at 800 °C (**a**, **b**) and 1000 °C (**c**, **d**). AFE-like behaviour (peak splitting) is observed for both samples initially. Sample annealed at 1000 °C behaves ferroelectric after field cycling

Fig. 3 Endurance behaviour of HSO MFIS stacks. Samples annealed at lower temperatures show early breakdown

breakdown is observed for samples with lower annealing temperatures and therefore thinner interface layer for a constant amplitude of 5 V. While this appears to be reasonable from changes in the field-drop across the interface layer and ferroelectric layer due to changes in the interface capacitance [12], no significant shifts in the switching voltages are observed for the different samples. This is most likely a result of band alignment, changes in the crystallographic texture combined with only small changes in the interface layer thickness. As a result, improved ferroelectric properties as well as endurance can be achieved by high temperature annealing and therefore increased interface thickness. However, recent studies have shown that the high temperature anneal modifies the crystallographic texture of the ferroelectric [5] and results in a strongly reduced retention of one state [4]. In addition, fatigue of the ferroelectric is observed, as P_R reduces close to 10^4 cycles.

In order to decouple these effects, samples with thermal oxidised interfaces of different thickness are investigated. Since the density might differ compared to chemical

oxidised interfaces, the actual equivalent-oxide-thickness will be slightly different. GIXRD patterns of these samples (Fig. 4a) do not show significant differences suggesting no major difference in the crystallographic texture. Dynamic hysteresis measurements of the samples with thicker interfaces already differ in the wake-up behaviour, as depicted in Fig. 4c and d and show non-split wake-up in contrast to the previously observed asymmetric wake-up (see Fig. 4b) for this annealing temperature (650 °C). Consequently, the difference in wake-up are not originating from the difference in crystallographic texture, but is a direct result of changes in the interface layer. In addition, the impact of the thicker interface layer is strongly reflected in the required switching voltage, as expected for the capacitance change [12].

Furthermore, retention measurements of these samples (see Fig. 4e) show similar trends as previously observed. In consequence, the strong destabilisation of one state is a direct result of the increased interface layer thickness. Therefore, optimising interface thickness for ferroelectric-like wake-up comes with a trade-off in retention. However, changes in the chemical composition of the interface layer and therefore the permittivity of the interface layer material could offer a way to circumvent this trade-off.

Conclusion

In conclusion, the interface layer has a major impact on the behaviour and reliability of ferroelectric hafnium oxide in MFIS capacitors, and consequently FeFETs. Thin interface layers result in asymmetric wake-up, during which hysteretic behaviour with ferroelectric and antiferroelectric-like behaviour on either side of the hysteresis, respectively, can be observed. Furthermore, thicker interface layers result in an initially ferroelectric-like behaviour, with the trade-off of reduced retention of one polarisation direction. Changes in the interface permittivity might help to overcome this trade-off.

Fig. 4 Impact of interface layer thickness for samples annealed at 650 °C. No increased line intensities are observed for low angles in the GIXRD pattern (a). While AFE-like wake-up is observed for 1.2 nm thick interface (b), ferroelectric-like wake-up is observed for

thicker interfaces, as shown for 2.7 nm (c) and 3.7 nm (d), respectively. Retention loss in the negative P_R state (e) becomes more severe with increasing interface thickness

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Data availability Research data are not shared.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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References

1. J. Müller, P. Polakowski, S. Müller, T. Mikolajick, *ECS J. Solid State Sci. Technol.* **4**(5), N30 (2015). <https://doi.org/10.1149/2.0081505jss>
2. J. Müller, P. Polakowski, S. Müller, H. Mulaosmanovic, J. Ocker, T. Mikolajick, S. Slesazek, S. Flachowsky, M. Trentzsch, in *Non-Volatile Memory Technology Symposium, NVMTS (IEEE, Piscataway, NJ, 2016)*, pp. 1–7. <https://doi.org/10.1109/NVMTS.2016.7781517>
3. N. Gong, T.P. Ma, *IEEE Electron Device Lett.* **37**(9), 1123 (2016). <https://doi.org/10.1109/LED.2016.2593627>
4. M. Lederer, F. Müller, K. Kühnel, R. Olivo, K. Mertens, M. Trentzsch, S. Dinkel, J. Müller, S. Beyer, K. Seidel, T. Kämpfe, L.M. Eng, *IEEE Electron Device Lett.* **41**(12), 1762 (2020). <https://doi.org/10.1109/LED.2020.3031308>
5. M. Lederer, A. Reck, K. Mertens, R. Olivo, P. Bagul, A. Kia, B. Volkmann, T. Kämpfe, K. Seidel, L.M. Eng, *Appl. Phys. Lett.* **118**(1), 012901 (2021). <https://doi.org/10.1063/5.0029635>
6. M. Lederer, R. Olivo, D. Lehninger, S. Abdulazhanov, T. Kämpfe, S. Kirbach, C. Mart, K. Seidel, L.M. Eng, *Physica Status Solidi (RRL)* (2021). <https://doi.org/10.1002/pssr.202100086>
7. M. Lederer, T. Kämpfe, R. Olivo, D. Lehninger, C. Mart, S. Kirbach, T. Ali, P. Polakowski, L. Roy, K. Seidel, *Appl. Phys. Lett.* **115**(22), 222902 (2019). <https://doi.org/10.1063/1.5129318>
8. M.W. Lederer, T. Kämpfe, N. Vogel, D. Utess, B. Volkmann, T. Ali, R. Olivo, J. Müller, S. Beyer, M. Trentzsch, K. Seidel, L.M. Eng, *Nanomaterials (Basel, Switzerland)* **10**(2), 384 (2020). <https://doi.org/10.3390/nano10020384>
9. T. Schenk, C.M. Fancher, M.H. Park, C. Richter, C. Künneth, A. Kersch, J.L. Jones, T. Mikolajick, U. Schroeder, *Adv. Electron.*

- Mater. **5**, 1900303 (2019). <https://doi.org/10.1002/aelm.201900303>
10. T. Schenk, E. Yurchuk, S. Müller, U. Schröder, S. Starschich, U. Böttger, T. Mikolajick, Appl. Phys. Rev. **1**(4), 041103 (2014). <https://doi.org/10.1063/1.4902396>
 11. C. Mart, K. Kühnel, T. Kämpfe, M. Czernohorsky, M. Wiatr, S. Kolodinski, W. Weinreich, ACS Appl. Electron. Mater. (2019). <https://doi.org/10.1021/acsaelm.9b00591>
 12. K. Ni, P. Sharma, J. Zhang, M. Jerry, J.A. Smith, K. Tapily, R. Clark, S. Mahapatra, S. Datta, IEEE Trans. Electron Devices **65**(6), 2461 (2018). <https://doi.org/10.1109/TED.2018.2829122>