



#### ULTRA-WIDE BANDGAP MATERIALS, DEVICES, AND SYSTEMS

## Inversion-type p-channel diamond MOSFET issues

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This article reviews the state of the art in inversion-type p-channel diamond MOSFETs. We successfully developed the world's first inversion-channel homoepitaxial and heteroepitaxial diamond MOSFETs. We investigated the dependence of phosphorus concentration ( $N_p$ ) of the n-type body on field-effect mobility ( $\mu_{FE}$ ) and interface state density ( $D_{it}$ ) for the inversion channel homoepitaxial diamond MOSFETs. With regard to the electrical properties of both the homoepitaxial and heteroepitaxial diamond MOSFETs. With regard to the electrical properties of both the homoepitaxial and heteroepitaxial diamond MOSFETs, they suffer from low  $\mu_{FE}$  and one main reason is high  $D_{it}$ . To improve the interface quality, we proposed a novel technique to form OH-termination by using H-diamond followed by wet annealing, instead of the previous OH-termination formed on O-diamond. We made precise interface characterization for diamond MOS capacitors by using the high-low C–V method and the conductance method, providing further insights into the trap properties at Al<sub>2</sub>O<sub>3</sub>/diamond interface, which would be beneficial for performance enhancement of the inversion-type p-channel diamond MOSFETs.

### Introduction

Diamond is considered as an ultimate material for powerelectronics applications owing to its superior physical properties, such as a wide bandgap (5.5 eV), high breakdown electric field (>10 MV/cm), high carrier mobility (7300 and 5300 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> for electron and hole, respectively), and high thermal conductivity (2200 Wm<sup>-1</sup>K<sup>-1</sup>) [1-5]. Therefore, diamond-based devices are promising for power applications and have been receiving more and more attention in recent years [6-13]. Among diamond power devices, the diamond metal-oxide-semiconductor field-effect transistor (MOSFET), a kind of popular power switching device, has been intensively investigated worldwide. Many studies have been devoted to the development of hydrogenated diamond (H-diamond) MOSFETs because the H-diamond surface can accumulate two-dimensional hole gases [14-23]. Recently, Kawarada's group reported the first vertical H-diamond MOS-FETs [24, 25]. In addition, Pernot's group proposed the deep depletion concept and concentrated on the oxygen-terminated diamond (O-diamond) MOSFETs [26-28]. However, both Hand O-diamond MOSFETs basically demonstrate normally on characteristics. Recently, a few accumulation-channel H-diamond MOSFETs with normally off properties have been developed [29-32]; however, it is difficult for them to control the threshold voltage by selection of metal work function. In contrast, diamond MOSFETs with inversion channels are more competitive because they can modulate the threshold voltage by changing the impurity concentration in the body and thus control the electric power. Our group has been focusing on the development of inversion-type p-channel diamond MOSFETs with normally off operation in recent years. We concentrated on the hydroxyl (OH)-terminated diamond (111) surface formed by O-diamond followed by wet annealing, and successfully fabricated the world's first inversion-type p-channel homoepitaxial diamond MOSFETs [33]. We characterized the corresponding electrical properties and evaluated the effect of the surface roughness on the field-effect mobility  $(\mu_{\rm EE})$ . Besides, we investigated the dependence of phosphorus concentration ( $N_{\rm P}$ ) of the n-type body on  $\mu_{\rm FE}$  and interface state density  $(D_{it})$  for the inversion channel homoepitaxial diamond MOSFETs [34]. Considering the commercialization, the application of the homoepitaxial diamond MOSFETs are limited due to the small size of High-pressure High-temperature



(HPHT) diamond substrates and their high cost. Concerning this issue, we attempted to develop the inversion-type p-channel heteroepitaxial freestanding diamond MOSFETs where the diamond epitaxy was realized on Iridium (Ir)/intermediate layer/Si substrates [35]. With regard to the electrical properties of both the homoepitaxial and heteroepitaxial inversionchannel diamond MOSFETs, they suffer from low  $\mu_{\text{FE}}$  and one of the main limiting factors is high  $D_{it}$ . Aiming at this problem, we focused on the interface evaluation of Al<sub>2</sub>O<sub>3</sub>/ diamond from the perspective of diamond MOS capacitors by employing the high-low capacitance-voltage (C-V) method [36]. To reduce  $D_{it}$  and to improve the interface quality, we proposed a novel technique to form OH-termination by using H-diamond followed by wet annealing [37], instead of the previous OH-termination formed on O-diamond. And we made more precise interface characterization by using the high-low C-V method at various temperatures and with wide frequency ranges [38]. Furthermore, we employed the hightemperature conductance method by considering the surface potential fluctuation to gain further insights into the properties of interfaces states at Al<sub>2</sub>O<sub>3</sub>/diamond interface, including the capture cross section, time constant of interfaces states and the trap type, which would be beneficial to have a profound understanding of the Al<sub>2</sub>O<sub>3</sub>/diamond interface [39]. The purpose of this paper is to review the current progress of the studies of the inversion-type p-channel diamond MOSFETs and the corresponding interface characterization of diamond MOS capacitors. Specifically, in Sec. I.A and Sec. I.B, the work about inversion-channel homoepitaxial and heteroepitaxial diamond MOSFETs is introduced. In Sec. II.A and II.B, we exhibit the work about the interface characterization and comparison for two kinds of Al<sub>2</sub>O<sub>3</sub>/diamond MOS capacitors where OH-termination was formed on O-diamond or H-diamond. Finally, we give a brief conclusion.

#### **Results and discussion**

#### Inversion-type p-channel diamond MOSFETs

#### Inversion-type p-channel MOSFETs on homoepitaxial diamond substrates

Figure 1a and b demonstrate the schematic cross-section and top-view optical microscope image of the inversion-type p-channel HPHT diamond MOSFETs. Figure 2a shows the drain current density-drain voltage ( $I_{\rm ds}$ - $V_{\rm ds}$ ) characteristics at various gate voltages ( $V_{\rm gs}$ ) for a typical diamond MOSFET with gate length (L) of 5 µm and gate width (W) of 150 µm. The MOSFET clearly shows the normally off feature and saturation characteristics. The maximum value of  $I_{\rm ds}$  is – 1.6 mA/mm and the peak drain conductance is 0.73 mS/mm, respectively. Figure 2b shows  $I_{\rm ds}$  in the linear scale and transfer conductance  $g_{\rm m}$  vs  $V_{\rm gs}$  characteristics where  $V_{\rm ds}$  was set as – 0.1 V. The maximum  $g_{\rm m}$  is 30  $\mu$ S/mm at  $V_{\rm gs} = -10.7$  V. According to the  $I_{\rm ds}$ – $V_{\rm gs}$  characteristics, the threshold voltage ( $V_{\rm T}$ ), determined from the fitting of the  $I_{\rm ds}$ – $V_{\rm gs}$  curve in the  $V_{\rm gs}$  range from – 7 to – 9 V, was 6.3 V. The field effect mobility ( $\mu_{\rm FE}$ ) was estimated using the following equation [40]:

$$\mu_{\rm FE} = g_{\rm m} \frac{L}{W C_{\rm ox} V_{\rm ds}},\tag{1}$$

where  $C_{\text{ox}}$  is the gate oxide capacitance per unit area (dielectric constant of Al<sub>2</sub>O<sub>3</sub>: 7.3). The maximum  $\mu_{\text{FE}}$  was estimated to be 8.0 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>. Based on the log  $|I_{\text{ds}}|-V_{\text{gs}}$  characteristics, the sub-threshold swing (*S*) can be evaluated by [40]

$$S = ln10 \frac{dV_{\rm gs}}{d(lnI_{\rm ds})} \cong ln10 \frac{kT}{q} \left(1 + \frac{C_{\rm d} + C_{\rm it}}{C_{\rm ox}}\right), \qquad (2)$$

where k is the Boltzmann constant, T the absolute temperature, q the electronic charge,  $C_d$  the depletion-layer capacitance, and C<sub>it</sub> the capacitance contribution from the interface sates and it is equal to  $qD_{it}$ , where  $D_{it}$  the density of interface states [40]. The subthreshold swing S, calculated from the fitting of the  $I_{\rm ds}$ - $V_{\rm gs}$  curve in the  $V_{\rm gs}$  range from – 3.0 to – 3.5 V, was around 380 mV/dec. Note that we calculated the theoretical value of  $C_d$ and found that it was much lower than  $C_{ii}$ ; thus, we can deduce that the S value was dominated by  $C_{it}$ . According to the S value, the corresponding D<sub>it</sub> was evaluated from the subthreshold region, with the value of about  $6 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>. Note that the D<sub>it</sub> estimated from S value can only reflect a small fraction of the interface states that locate between flatband and weak inversion conditions. We can deduce that the high D<sub>it</sub> would be one reason for the low channel mobility. Besides, we employed the transmission electron microscopy (TEM) and atomic force microscopy (AFM) measurements to further examine the MOS structure under the gate and the diamond surface of the phosphorus-doped n-type body. From Fig. 3a, we can observe the dark line existing at the interface between the Al<sub>2</sub>O<sub>3</sub> layer and the n-type diamond body, which indicates the presence of bunching steps, consistent with the AFM result demonstrated in Fig. 3b. The existence of the bunching steps implies that the surface morphology was not that good, which would result in low  $\mu_{\rm FE}$ . In addition, it is significant to improve the quality of the phosphorus-doped n-type diamond body to achieve high  $\mu_{\rm FE}$ . In terms of the phosphorus doping, fortunately, we successfully realized the reproducible control of phosphorus doping  $(N_n)$ from  $2 \times 10^{15}$  to  $3 \times 10^{17}$  cm<sup>-3</sup> for diamond films in a previous study [41]. Therefore, we further investigated the  $N_p$  dependence of  $\mu_{\rm FE}$  and  $D_{\rm it}$  in the inversion channel homoepitaxial diamond MOSFET to understand its electrical and physical characteristics. We fabricated four inversion-type p-channel homoepitaxial diamond MOSFETs where the n-type bodies have different  $N_p$ 





Figure 1: (a) Schematic cross-section and (b) top-view image of the inversion-type p-channel HPHT diamond MOSFETs by optical microscopy. Reprinted with permission from Ref. [33] (https://creativecommons.org/licenses/by/4.0/).



Figure 2: (a) Drain current density-drain voltage ( $I_{ds}-V_{ds}$ ) and (b) drain current density-gate voltage ( $I_{ds}-V_{gs}$ ) characteristics for the inversion-type p-channel HPHT diamond MOSFET. Reprinted with permission from Ref. [33] (https://creativecommons.org/licenses/by/4.0/).

concentrations of  $2 \times 10^{15}$ ,  $1 \times 10^{16}$ ,  $3 \times 10^{16}$ , and  $6 \times 10^{16}$  cm<sup>-3</sup>. The specific fabrication conditions were introduced in our previous paper [34]. Here, we mainly focused on the electrical characteristic comparison. Figure 4a shows the  $I_{ds}$  and  $\mu_{FE}$  vs  $V_{gs} - V_T$ for the four homoepitaxial diamond MOSFETs with various doping concentrations. Note that the  $V_{\rm T}$  was subtracted from the applied gate voltage for accurate comparison. The absolute value of  $V_{\rm T}$  increases with increasing the phosphorus doping concentration (not shown), indicating the good  $V_{\rm T}$  modulation for the inversion-type diamond MOSFETs.  $\mu_{\rm FE}$  was estimated from the slope of each  $I_{ds}$ - $V_{gs}$  curve. It is obvious that  $I_{\rm ds}$  and  $\mu_{\rm FE}$  increase when  $N_{\rm p}$  decreases. And  $\mu_{\rm FE}$  reached 20  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  for the MOSFET with  $N_{\text{P}}$  of  $2 \times 10^{15}$  cm<sup>-3</sup>. To further examine the dependence of  $N_{\rm p}$  on  $\mu_{\rm FE}$ ,  $D_{\rm it}$  was evaluated from the threshold slope of the  $I_{\rm ds}-V_{\rm gs}$  characteristics using the subthreshold swing method. Figure 4b shows the dependence of the phosphorus doping concentration on interface state density. It is obvious that  $D_{\rm it}$  increases with decreasing  $N_{\rm p}$ . Figure 4c demonstrates the correlation between the maximum  $\mu_{\rm FE}$  and D<sub>it</sub> for the inversion channel diamond MOSFETs. Note that the reported  $D_{it}$ - $\mu_{FE}$  results of other diamond MOSFETs with

different surface terminations are also inserted in Fig. 4c [21, 42, 43]. We can see that the  $\mu_{FE}$  and  $D_{it}$  are inversely correlated. Thus, the high  $D_{it}$  is one main limiting factor for the channel mobility of diamond MOSFETs. From the changing tendency of  $D_{it}$ - $\mu_{FE}$  demonstrated by the arrow inserted in Fig. 4c, we can expect that  $\mu_{FE}$  can exceed 1000 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> if  $D_{it}$  is reduced to lower than 10<sup>11</sup> cm<sup>-2</sup>eV<sup>-1</sup>. This is consistent with the theoretical mobility calculation by considering four scattering mechanisms for the H-diamond MOSFET by Sasama et. al. [44]. Therefore, in our case, it is also very important to develop effective passivation processes to reduce  $D_{it}$  and improve the interface quality between Al<sub>2</sub>O<sub>3</sub> and diamond and thus fabricate the diamond power MOSFETs with superior electrical properties.

# Inversion-type p-channel MOSFETs on heteroepitaxial diamond substrates

As we introduced in Sec. I.A, we developed the world's first inversion type p-channel homoepitaxial diamond MOSFETs and made the corresponding electrical and physical analysis. Despite the significant breakthrough, given the commercialization and mass production, the substrate size and cost need





Figure 3: (a) TEM image of Al<sub>2</sub>O<sub>3</sub>/diamond interface. (b) AFM image of surface of n-type diamond body. Reprinted with permission from Ref. [33] (https://creativecommons.org/licenses/by/4.0/).

to be considered. It is known that the size of HPHT diamond substrates is limited within several square millimeters, which is not beneficial to the commercialization of diamond power MOSFETs. Regarding this issue, using heteroepitaxial diamond substrates would be one solution. Diamond epitaxy has been studied for decades and different materials have been explored for heteroepitaxial diamond growth [45-56]. Among them, the silicon (Si)-based substrate is one promising candidate for fabrication of diamond power devices due to its large wafer size and low cost. Kawashima et al. and Murooka et al. have fabricated the heteroepitaxial diamond Schottky barrier diodes (SBDs) on Ir/intermediate layer/Si and 3C-SiC/Si substrates, respectively [47, 54]. However, the potential of the inversiontype heteroepitaxial diamond MOSFET has not been evaluated yet. Based on the fabrication technique of the inversion-channel HPHT diamond MOSFETs, we successfully fabricated the inversion-channel heteroepitaxially-grown freestanding diamond MOSFET where the diamond heteroepitaxy was realized on Ir/intermediate layer/Si (111) substrate [35]. We examined the electrical properties of the heteroepitaxial diamond MOSFET and the surface morphology by AFM.

Figure 5a shows the top-view optical microscope image of the inversion-type p-channel heteroepitaxial diamond MOS-FETs. Figure 5b and c illustrate the  $I_{ds}$ - $V_{ds}$  and  $I_{ds}$ - $V_{gs}$  characteristics for a typical heteroepitaxial diamond MOSFET with L of 15 mm and W of 150 mm.  $I_{\rm ds}$ - $V_{\rm ds}$  properties clearly show the normally off feature and a saturation tendency. The maximum drain current density is about 0.35 mA/mm. From  $I_{ds}$ - $V_{gs}$  characteristics shown in Fig. 5c, the  $V_{\rm T}$  determined by linear extrapolation of the  $I_{ds}$ - $V_{gs}$  curve to zero [40], is about – 5.1 V. The  $\mu_{\rm FE}$ - $V_{\rm gs}$  characteristic is shown in Fig. 5d. The maximum of  $\mu_{\rm FE}$ was about 2.7 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>. This value is slightly lower than the  $\mu_{\rm FF}$ reported in homoepitaxial diamond MOSFETs, as mentioned in Sec. I.A. For the heteroepitaxial diamond MOSFET,  $\mu_{\text{FE}}$ first increases with the negative  $V_{\rm gs}$  lower than – 7 V and then decreases with higher negative  $V_{\rm gs}$ . The latter would be caused by acoustic phonon or surface roughness scattering [44, 57-59]. According to the log  $|I_{ds}| - V_{gs}$  characteristics, S is estimated to



**Figure 4:** (a)  $I_{ds}$  and  $\mu_{FE}$  vs  $V_{qs} - V_T$  for the four homoepitaxial diamond MOSFETs with various doping concentrations, (b) the dependence of  $N_p$  on  $D_{it}$  and (c) the correlation between  $D_{it}$  and maximum  $\mu_{FE}$  of the inversion channel HPHT diamond MOSFETs. Note that the reported  $D_{it}$  vs  $\mu_{FE}$  of other terminated MOSFETs were also summarized. (a) and (b) reprinted with permission from Ref. [34] (https://creativecommons.org/licenses/by/4.0/).



be 355 mV/dec. And the corresponding  $D_{it}$  extracted from the subthreshold region is about  $5.5 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>. This value is not significantly different from the  $D_{it}$  of the homoepitaxial diamond MOSFETs. To discuss scattering by surface roughness, the surface properties of the n-type body of the heteroepitaxial diamond MOSFET has been characterized by AFM measurements, as illustrated in Fig. 5e. The root mean square roughness (RMS) of the n-type diamond surface is 30.6 nm with the scanning area of 15  $\mu$ m × 15  $\mu$ m. The AFM image demonstrates two local regions with distinct differences of surface morphologies. To investigate the detailed surface properties, AFM measurements were performed with typical scanning areas of 500 nm × 500 nm. The results are shown in Fig. 5e: see lower left and lower right insets. The RMS varies from 2.2 (left) to 13.8 nm (right). The RMS difference may be correlated with the different crystalline phases generated from the non-uniformity of the defect dislocation during the heteroepitaxial diamond growth. Nevertheless, the RMS of 2.2 nm is still larger than that of HPHT diamonds (below 1 nm within a comparable scanning area). The origin of this roughness after polishing the hetero-diamond layer is not clear up to now. It indicates that, however, this may be one limiting factor of the channel mobility. Besides, the relatively

poor quality of the heteroepitaxial diamond, with the dislocation density of around 10<sup>8</sup> cm<sup>-2</sup> [54], would also lead to the low  $\mu_{\rm FF}$  of the heteroepitaxial diamond MOSFET. It should be noted that the channel mobility of the inversion-type p-channel MOSFET on the heteroepitaxial diamond is lower than those of the H-terminated diamond MOSFETs or MISFETs fabricated on polycrystalline or heteroepitaxial diamonds [48, 60-62]. One possible reason is due to the uneven quality and resultant different surface roughnesses of the heteroepitaxial or polycrystalline diamond films formed by this work and others. Besides, the higher density of interface states in our inversion-type diamond MOSFETs, more than one order of magnitude higher than the H-terminated diamond surface (below 10<sup>11</sup> cm<sup>-2</sup>eV<sup>-1</sup>), would be another main reason for the low channel mobility. In addition, the carrier density in our case is low, around  $0.8 \sim 4.3 \times 10^{12}$  cm<sup>-2</sup>. For the H-terminated diamond devices, their carrier density is on the order of  $10^{13}$  cm<sup>-2</sup> and the high density of channel carriers would bring about the screening effect and thus lead to the high channel mobility. Obviously, heteroepitaxial growth of diamond requires further improvements before high-quality MOSFETs can be realized. With the "lateral overgrowth technique" [63-68], a better surface can be



**Figure 5:** (a) Top-view image of the inversion-type p-channel heteroepitaxial diamond MOSFETs by optical microscopy, (b)  $I_{ds}-V_{ds'}$  and (c)  $I_{ds}-V_{gs}$  characteristics for a typical MOSFET with  $L/W = 15/150 \mu$ m, (d)  $V_{gs}$  dependence of  $\mu_{FE}$  for the inversion type p-channel heteroepitaxial diamond MOSFET and (e) three-dimensional AFM images of the n-type diamond body. Reprinted with permission from Ref. [35] (https://creativecommons.org/licenses/by/4.0/).



grown to form atomically flat diamond surfaces, with the aim to reduce the RMS significantly. By these ways, the device performance of the inversion-type p-channel heteroepitaxial diamond MOSFETs can be improved, which would facilitate the commercialization of diamond electronic applications like power devices significantly.

#### Al<sub>2</sub>O<sub>3</sub>/p-type diamond MOS interface

We have successfully developed the inversion-type p-channel MOSFETs on both homoepitaxial and heteroepitaxial diamond substrates. However, the low channel mobility is one big challenge for their practical application. From the electrical property characterization, the  $D_{it}$  is considered as one of the main reasons for the low channel mobility. As mentioned above, the  $D_{it}$  estimated from the log  $|I_{ds}| - V_{gs}$  characteristics and the relevant *S* value of the MOSFETs can just reflect a small fraction of the interface states located in the energy interval between flatband and weak inversion conditions. The more precise evaluation of  $D_{it}$  is required by focusing on the Al<sub>2</sub>O<sub>3</sub>/diamond MOS capacitors. We would like to introduce the relevant work in detail in the following sections.

# Interface of Al<sub>2</sub>O<sub>3</sub>/p-type OH-diamond formed by wet annealing on O-diamond

Regarding the studies of diamond MOS capacitors, we just concentrated on the HPHT diamond substrates. The specific fabrication process was introduced in our previous report [36]. Figure 6a shows the capacitance–voltage (C–V) characteristics of the p-type diamond (111) MOS capacitor at frequencies of 10 Hz and 10 kHz. Note that the leakage current was low enough. Based on the high-low C–V method,  $D_{it}$  can be calculated as [40]

$$D_{\rm it} = \frac{C_{\rm ox}}{q^2} \left( \frac{C_{\rm lf}/C_{\rm ox}}{1 - C_{\rm lf}/C_{\rm ox}} - \frac{C_{\rm hf}/C_{\rm ox}}{1 - C_{\rm hf}/C_{\rm ox}} \right), \tag{3}$$

where  $C_{ox}$  is the oxide capacitance, q the elementary charge,  $C_{\rm lf}$  the capacitance at a low frequency and  $C_{\rm hf}$  the capacitance at a high frequency. The energy distribution of  $D_{\rm it}$ is shown in Fig. 6b. The estimated  $D_{\rm it}$  was in the range of  $4-9\times10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>. Note that the frequency range is relatively narrow. The low frequency is not low enough and a fraction of slow interface states cannot follow the ac signal; therefore, the  $C_{\rm lf}$  is not able to contain all the capacitance contribution of interface states. Likewise, the high frequency is not high enough and the  $C_{\rm hf}$  cannot exclude the capacitance components of the fast interface states. Thus, we should say the true  $D_{\rm it}$  would be higher than the estimated value. Therefore, the diamond MOS characterization also verifies that the high  $D_{\rm it}$  would be one main limiting factor for the low  $\mu_{\rm FE}$ . However, the origin of the high D<sub>it</sub> is still unclear. Here, we would like to discuss the possible reason. With regard to the O-terminated diamond surface, the possible candidates of surface states are considered as two types of surface oxygen sites; one is bridge site (C-O-C) and the other is on top site (C=O) [69, 70], which has been detected for O-terminated diamond surface by Fourier transform infrared (FTIR) spectroscopy in our previous work [37]. The presence of C-O-C and C=O makes it less effective to form C-OH termination by employing subsequent wet annealing process. For the subsequent ALD process, it would be difficult for C-O-C and C = O to react with  $Al(CH_3)_3$  (TMA) and both would still remain at the interface, which may be responsible for high  $D_{it}$ of the OH-terminated diamond MOS formed on O-terminated one. Therefore, the reduction of C-O-C and C=O may be beneficial to improve the interface properties of Al2O3/diamond and further to enhance device performance of diamond MOSFETs.

# Interface of $Al_2O_3$ /p-type OH-diamond formed by wet annealing on H-diamond

Considering the possible origin of high  $D_{it}$  as analyzed above, we developed a novel technique to form OH-termination on H-diamond surface, instead of on O-diamond one, with the purpose of the reduction of C-O-C and C = O. We found that the two-dimensional hole gas layer disappeared when the wet annealing temperature exceeded 500 °C. From the measurements by FTIR spectroscopy, we observed the C-O-H peak. Moreover, the surface morphology was not degraded before and after wet annealing [37]. Therefore, we employed this OH-formation technique on H-diamond surface to fabricate the Al<sub>2</sub>O<sub>3</sub>/ diamond MOS capacitors and carefully evaluated the interface properties by using high-low C-V method and conductance method. The frequency-dependent C-V characteristics at 300 K for the p-type diamond MOS capacitor was demonstrated in Fig. 7a. We can observe a hump at 1 Hz and its magnitude decreases with increase in the measurement frequency. We can deduce that the hump would be attributed to the response of the interface states at deep energy levels. Because the interface states at deep energy levels have long emission time constants, they can follow the ac signal at low frequencies and thus contribute to the capacitance, whereas they cannot immediately change occupancy in response to the ac gate voltages at high frequencies, resulting in the frequency dispersion. Considering the time constant property of interface states at deep energy levels, measurements at higher temperatures are indispensable to detect them because their thermal emission would become faster and even deeper interface states can be detected within the same given frequency range. Figure 7b and c illustrate the frequency-dependent C-V characteristics at 350 and 400 K. The frequency dispersion of C-V curves in the depletion region





Figure 6: (a) C–V characteristics at 10 Hz and 10 kHz and (b) D<sub>it</sub> vs energy position from E<sub>v</sub> of diamond for the p-type diamond (111) MOS capacitor where OH-termination was formed on O-diamond followed by wet annealing.

increases as the measurement temperature increases, indicating that interface states at deep energy levels can be detected at 400 K. Note that the frequency dispersion of the accumulation capacitance was also observed, which would be attributed to the border traps, often observed in InGaAs and SiC MOS structures [71-74]. The effect of series resistance on the accumulation capacitance was examined by a standard correction method [75], but the dispersion was unchanged after the correction. The frequency dispersion analysis of the accumulation capacitance requires a distributed circuit model which could quantify the impendence components of the border traps and is essential to investigate in the next step. Here, let us focus on the depletion region and the interface states at deep energy levels. According to the C-V dispersion from 1 Hz and 10 MHz at 400 K and highlow method, we evaluated  $D_{it}$  vs the energy position from  $E_v$  of diamond, as demonstrated in Fig. 7d. We should point out that the surface potential was determined by the Berglund integral, and the integral constant ( $\psi_{s0}$ ) was determined from the flatband voltage in the C-V curve at 10 MHz [76]. With respect to the energy position dependence of D<sub>it</sub>, D<sub>it</sub> first increases dramatically from 0.23 to 0.6 eV and then gradually saturates at energy position deeper than 0.6 eV from  $E_v$  of diamond. Even though the detectable energy range is limited, the decrease in  $D_{it}$  in the energy levels deeper than 0.76 eV from  $E_{y}$ , corresponding to the gate voltage higher than 1.6 V, can be expected from the reduced frequency dispersion of the C-V characteristics. The estimated trap density was  $(0.4-1.5) \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup>, lower than that of the Al<sub>2</sub>O<sub>3</sub>/diamond MOS with a value of  $(4-9) \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$ in which the OH-terminated diamond surface was formed on the O-terminated diamond, as we introduced in Sec. II.A. Even though the measurement temperature and frequency ranges are different, the Al<sub>2</sub>O<sub>3</sub>/diamond interface quality is improved. Here, we would like to discuss the possible reason. When the OH-termination is formed by H-plasma and subsequent wet annealing, the C-OH bonds were formed [37]. Then during the ALD growth of Al<sub>2</sub>O<sub>3</sub>, these C–OH bonds can react with TMA to form C–O–Al. However, it is difficult for C–O–C and C=O to react with TMA to form C–O–Al in the case of the Al<sub>2</sub>O<sub>3</sub>/OH-terminated diamond formed on O-terminated treatment. Thus, there would be more C–O–C and C=O for OH-terminated diamond formed by O-terminated treatment than that formed by H-terminated treatment. Given that C–O–C and C=O could be responsible for the high  $D_{it}$ , we can deduce that  $D_{it}$  is lower for the OH-terminated diamond formed on H-terminated diamond followed by wet annealing than that by O-termination and subsequent wet annealing. Note that the interface states at deep energy levels can act as Coulomb scattering centers when they are positively charged and thus degrade the channel mobility of diamond MOSFETs; therefore, more effective passivation techniques are required to reduce  $D_{it}$ .

Prior to the further development of passivation techniques, it is important to make a deep understanding for the interface states at deep energy potions away from  $E_{y}$  of diamond. However, the limitation of the high-low method makes it difficult to precisely evaluate the interfaces states. Therefore, we applied the more powerful conductance method to analyze the Al<sub>2</sub>O<sub>3</sub>/diamond interface [77–79]. The conductance method can accurately determine D<sub>it</sub> and time response by detecting the time delay of carrier exchange between interface states and the energy band edge via an ac conductance component. To be specific, a small ac voltage superimposed on a certain dc voltage is applied to the gate of a MOS capacitor and thus alternately moves the band edges towards or away from the Fermi level, resulting in the capture and emission of majority carrier between interface states and the energy band edge. The lag-behind of the interfaces state response would lead to the energy loss. The energy loss caused by interface states can be reflected by the measurement parameter of parallel conductance G<sub>p</sub>. Therefore, the information of interface states can be obtained from  $G_p$ [80]. This approach has been extensively applied for Si, Ge, SiC,





**Figure 7:** Frequency dispersion of C-V characteristics at (a) 300, (b) 350, and (c) 400 K for the p-type diamond (111) MOS capacitor where OH-termination was formed on H-diamond with wet annealing, and (d) the extracted  $D_{it}$  vs energy position from  $E_v$  of diamond at 400 K. Reprinted with permission from Ref. [38] (https://creativecommons.org/licenses/by/4.0/).

and GaN MOS structures [77, 81-83]. However, the interface of diamond MOS structures has been seldom investigated by this method. Pham et al. performed the conductance analysis for the Al<sub>2</sub>O<sub>3</sub>/O-terminated diamond capacitors with assuming the single-level interface states, and the surface potential fluctuation was neglected [84]. Likewise, Saha et al. employed the conductance method with assumption of single trap levels to characterize the Al<sub>2</sub>O<sub>3</sub>/H-terminated MOS structures [85]. They supposed two distinctive peaks to analyze the broadening of conductance peaks without consideration of surface potential fluctuation, where the two peaks correspond to interface traps and border traps. However, it should be noted that the assumption of the single energy level of interface states is the ideal case and cannot reflect the practical device-grade interfaces. A spatial distribution of interface state levels in energy over the semiconductor bandgap is the common case [80]. In fact, the broadening of the conductance peak indicates that the energy levels of interface states are spatially distributed in the semiconductor bandgap [80]. Moreover, surface potential fluctuation generated by the interface charge inhomogeneity should be taken into account, which is significant to elucidate the interface state properties, such as the interface state density,

trap type (donor-like or acceptor-like), capture cross section and time constant. The neglect of surface potential fluctuation would lead to errors when extracting interface state density.

Based on the introduction of the conductance method, we employed it with considering the surface potential fluctuation to gain deep insights into the properties of interface states for  $Al_2O_3/diamond$  MOS where OH-termination was formed on H-terminated diamond via wet annealing. Thus, we would like to introduce the conductance analysis in detail. We can first extract the experimental  $G_p/\omega$  by the equation as follows [80]:

$$\left(\frac{G_{\rm p}}{\omega}\right)_{\rm exp} = \frac{\omega G_{\rm exp} C_{\rm ox}^2}{G_{\rm exp}^2 + \omega^2 (C_{\rm ox} - C_{\rm exp})^2},\tag{4}$$

where  $\omega$ ,  $G_{exp}$ ,  $C_{ox}$ , and  $C_{exp}$  respectively represent the angular frequency, the experimental conductance, the oxide capacitance, and the experimental capacitance at a certain voltage and frequency. Note that series resistance ( $R_s$ ) has been extracted and  $G_{exp}$  and  $C_{exp}$  have been corrected. It was found that  $R_s$  has almost no effect on the  $G_p/\omega$  characteristics in the depletion region. The symbols in Fig. 8 stand for the experimental parallel conductance vs frequency ( $G_p/\omega$ -f) characteristics at various



gate voltages at 400 K. The maximum value of  $G_p/\omega((G_p/\omega)_{max})$ , representing the density of interface states, increases with the increase in gate voltage, which agrees well with the energy dependence of  $D_{it}$  extracted by the high-low method. We can see that the  $G_p/\omega$ -*f* curves were broadening, which implies that the surface potential fluctuation occurs. According to Nicollian's theory by considering the surface potential fluctuation, the theoretical  $G_p/\omega$  can be expressed as

$$\left(\frac{G_{\rm p}}{\omega}\right)_{\rm the} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{\rm it}}{\omega \tau_{\rm it}} ln \left[1 + (\omega \tau_{\rm it})^2\right] P(U_{\rm s}) dU_{\rm s}, \quad (5)$$

where  $U_{\rm s}$  and  $\tau_{\rm it}$  respectively represent the normalized surface potential and the interface state time constant [80].  $P(U_{\rm s})$  is a probability distribution of the surface potential fluctuation, expressed by

$$P(U_{\rm s}) = \frac{1}{\sqrt{2\pi\sigma_{\rm s}^2}} exp\left[-\frac{\left(U_{\rm s}-\overline{U_{\rm s}}\right)^2}{2\sigma_{\rm s}^2}\right],\tag{6}$$

where  $\overline{U_s}$  and  $\sigma_s$  represent the normalized mean surface potential and the standard deviation due to surface potential fluctuation [80]. These two equations indicate that we can employ Gaussian approximation to analyze the  $G_p/\omega$ -f properties. Here, Brews's graphical approach with assuming the validity of the Gaussian approximation to broadening of the conductance peak, was employed to extract the parameters of interface states, including  $D_{it}$ , hole capture cross section ( $\sigma_n$ ), time constant of interface states ( $\tau_{it}$ ), and standard deviation of surface potential fluctuation ( $\sigma_s$ ) [86, 87]. The experimental and theoretical  $G_{\rm p}/\omega$ -f curves were compared to confirm the fitting results and thus the accuracy of the extracted parameters. The solid lines in Fig. 8 represents the obtained theoretical  $G_p/\omega - f$  curves at various gate voltages. The good fitting was clearly observed from Fig. 8, suggesting the accuracy of the extracted parameters. The energy distribution of  $D_{it}$  is illustrated in Fig. 9a. Note that we also demonstrate the energy dependences of D<sub>it</sub> extracted by the high-low method and conductance method without considering surface potential fluctuation to make a comparison. The  $D_{\rm it}$  result extracted by conductance method is in accordance with that by high-low method; however, a big error occurs for the case without considering the surface potential fluctuation. Besides, the detectable energy range of  $D_{it}$  is narrow by using conductance method, owing to the measurement limitation that the peak frequencies  $(f_p)$  of  $G_p/\omega$  at other energy positions were out of the measurement frequency range and cannot be detected. Figure 9b and c show the energy dependence of the extracted  $\sigma_{\rm p}$  and  $\tau_{\rm it}$  of interface states. The extracted  $\sigma_{\rm p}$  was on the order of around  $10^{-17}$  cm<sup>2</sup>, comparable to the hole capture cross section at SiO<sub>2</sub>/Si interface [81]. According to the dependence of energy position on  $\tau_{it}$ , which reflects the characteristic time required to fill and empty interface traps at various levels, it can



**Figure 8:** Frequency dependence of experimental (denoted by circles) and theoretical (denoted by lines)  $G_p/\omega$  at 400 K. Reprinted with permission from Ref. [39] (https://creativecommons.org/licenses/by/4. 0/).

be deduced that the capture and emission of holes by interface states obey the Shockley-Read-Hall (SRH) statistics [88]. Figure 9d demonstrates  $\sigma_s$  as a function of the energy position from  $E_{\rm v}$  of diamond.  $\sigma_{\rm s}$  decreases as the trap energy level becomes away from  $E_v$  of diamond, which is a feature of donor-like traps. Here, we use the schematic band diagram illustrated in Fig. 10 to explain this phenomenon and the feature of donor-like traps. Donor-like traps are positive when empty, and neutral when full of electrons. When  $E_{\rm F}$  moves towards  $E_{\rm v}$  of diamond, as shown in Fig. 10a, the donor-like traps above  $E_{\rm F}$  remain positive and the ones below  $E_{\rm F}$  become neutral because they have occupied electrons. Note that the positive charging states can affect the surface potential fluctuation. Therefore, the  $\sigma_s$  is large when  $E_{\rm F}$  is close to  $E_{\rm v}$  of diamond. When  $E_{\rm F}$  moves far from  $E_{\rm v}$ , as shown in Fig. 10b, more donor-like traps will capture electrons and become neutral; therefore, the positive charging states will decrease. As a result, they can hardly affect the surface potential fluctuation and thus  $\sigma_s$  decreases. In terms of other oxide/ semiconductor MOS structures, the lower part of the bandgap generally is occupied with donor-like traps and the upper half is occupied with acceptor-like traps [40, 89]. To date, the investigation of diamond MOS interfaces is far from satisfactory and the origin of donor-like interface states is still not clear in the Al<sub>2</sub>O<sub>3</sub>/diamond interface [90, 91]. Concerning the oxide/Si interface, the P<sub>b</sub> centers are considered as the main reason for interface states and they are amphoteric. They behave acceptor-like in the upper half of the bandgap whereas they behave donor-like in the lower half of the bandgap [92]. Based on the Electrically-Detected-Magnetic-Resonance (EDMR) Study for SiO<sub>2</sub>/SiC interface, the C-related defects act as interfacial hole traps via their donor level and result in the negative threshold voltage shift for SiC MOSFETs [93]. Even though our interface





**Figure 9:** Energy distribution of (a) interface state density ( $D_{it}$ ), (b) capture cross section ( $\sigma_p$ ), (c) time constant of interfaces states ( $\tau_{it}$ ), and (d) standard deviation of surface potential fluctuation ( $\sigma_s$ ). Reprinted with permission from Ref. [39] (https://creativecommons.org/licenses/by/4.0/).

structure is different from the SiO<sub>2</sub>/SiC case, we can make a hypothesis that the C dangling bonds which are similar with  $P_{\rm b}$  centers could be one possible candidate for the donor-like interface traps in the Al<sub>2</sub>O<sub>3</sub>/diamond interface. However, further theoretical and experimental investigations are required to clarify the physical mechanism of the donor-like interface states.

### Conclusion

In conclusion, the research progress of the inversion-type p-channel diamond MOSFETs and corresponding p-type MOS capacitors have been reviewed in this paper. The inversion-channel homoepitaxial and heteroepitaxial diamond MOS-FETs were developed on OH-terminated diamond formed on O-diamond followed by wet annnealing. Aiming at the low  $\mu_{\text{FE}}$  for both kinds of MOSFETs, one of main limiting factors is the high  $D_{\text{it}}$ . Concerning the high  $D_{\text{it}}$ , we proposed a novel technique to form OH-termination to improve the interface quality of Al<sub>2</sub>O<sub>3</sub>/diamond by using H-diamond followed by wet

annealing, instead of the previous OH-termination formed on O-diamond. The interface quality was significantly improved based on our precise interface characterization and comparison for diamond MOS capacitors by using the high-low C-V method. Furthermore, we employed the conductance method to give further insights into the trap properties at Al2O3/diamond interface, which would be beneficial for deep understanding of the interface states and would facilitate the exploration of more efficient passivation techniques to improve the interface quality and device performance. Besides, with respect to the effect of the surface roughness on channel mobility, we should focus more on the fattening of the diamond surface in the next step, for example, we can employ the lateral overgrowth technique to form a better atomically flat diamond surface. With these efforts of surface roughness and interface quality, the device performance of the inversion-type p-channel diamond MOSFETs can be improved and their commercialization can be promoted. Besides, we desire to develop the trench-type inversion-channel diamond MOSFETs to facilitate their power application based on our novel technique that the V- and U-shaped diamond



#### Schematic band diagram and feature of donor-like traps

**Figure 10:** Interpretation for the feature of donor-like traps using the band diagrams of (a) Fermi level ( $E_F$ ) close to valence band edge ( $E_v$ ) and (b)  $E_F$  level far from  $E_v$  of diamond. Reprinted with permission from Ref. [39] (https://creativecommons.org/licenses/by/4.0/).

trench structures were successfully formed using Ni etching in high-temperature water vapour [94, 95].

#### **Experimental methods**

#### Inversion-type p-channel MOSFETs on homoepitaxial diamond substrates

We used the HPHT synthetic Ib (111) semi-insulating singlecrystal diamond substrates to fabricate the inversion-type p-channel homoepitaxial MOSFETs. First, the phosphorusdoped n-type body layer was deposited with a concentration of about ~  $1 \times 10^{17}$  cm<sup>-3</sup> by microwave plasma-assisted chemical vapor deposition (MPCVD). The methane concentration was 0.4%, plasma power 3.6 kW, and chamber pressure 150 Torr, respectively. The thickness of the deposited n-type body was ~ 10 µm. Then, a boron-doped p<sup>+</sup>-layer with a concentration of about  $1 \times 10^{20}$  cm<sup>-3</sup> was selectively grown by MPCVD using a metal mask of Ti/Au (10 nm/200 nm). The methane concentration, plasma power and chamber pressure were respectively 0.2%, 1200 W and 50 Torr. The thickness of the p<sup>+</sup>-layer was around 50 nm. After removing the metal mask by acid cleaning, the samples were subject to water vapor annealing to realize OH terminated diamond surface. The water vapor treatment was conducted by bubbling of N2 carrier gas through de-ionized water at 500 °C for 60 min in a quartz tube of an electric furnace. After that, 34 nm thick Al<sub>2</sub>O<sub>3</sub> film was deposited by atomic layer deposition (ALD) process at 300 °C. Finally, Ti/Pt/Au were evaporated to form gate, drain and source electrodes and their thicknesses were 30, 30, and 100 nm, respectively. The electrical properties of the diamond MOSFET were measured with a Keithley 4200-SCS parameter analyzer at room temperature. The surface roughness of the n-type diamond body was examined with a SHIMADZU SPM-9700 atomic force microscopy (AFM). Cross-sectional transmission electron microscopy (TEM) images were obtained using a JEOL JEM-ARM200F TEM system operated at an acceleration voltage of 14.5 keV.

# Inversion-type p-channel MOSFETs on heteroepitaxial diamond substrates

The Ir/intermediate layer/Si (111) substrate with a diameter of 10 mm was used to grow the heteroepitaxial diamond film using DC plasma CVD. Then, the heteroepitaxial diamond surface was mechanically polished to form the free-standing diamond substrate in 104 mm thick. After that, the free-standing heteroepitaxial diamond with size of 2 mm  $\times$  2 mm was cut from the hetero substrate to fabricate the inversion-channel diamond MOSFET. Due to the similarity of the fabrication process with the homoepitaxial diamond MOSFETs, the specific fabrication conditions would not be explained here.

# Fabrication of $Al_2O_3/p$ -type OH-diamond MOS capacitors on O-diamond

The OH-terminated diamond was formed on O-terminated one followed by wet annealing. Specifically, the wet annealing was performed under an atmosphere of N<sub>2</sub> gas bubbled through ultrapure water in a quartz tube in an electric furnace at 500 °C for 60 min. Then, ALD process was performed at 300 °C to deposit a 34-nm-thick  $Al_2O_3$  layer, where the thickness was confirmed by an ellipsometer for the sample with the identical ALD process on Si. Ti/Pt/Au (30 /30/ 100 nm) were then deposited to form top and bottom electrodes. All electrical properties were measured at room temperature in an ambient air atmosphere.



# Fabrication of $Al_2O_3/p$ -type OH-diamond MOS capacitors on H-diamond

The HPHT synthetic IIb 2.6° off-axis (111) single-crystal diamond substrate was used. In terms of the backside of diamond, a heavily boron-doped diamond layer with a concentration of ~  $1 \times 10^{21}$  atom/cm<sup>3</sup> was deposited, with the purpose of forming excellent ohmic contact. After cleaning with sulfuric-peroxide mixture, the diamond sample was subject to hydrogen plasma to form hydrogen termination in the MPCVD chamber. The pressure, microwave power, temperature and time of the plasma were 225 Torr, 800 W, 900 °C and 10 min, respectively. Then, OH-termination of wet annealing was performed at 500 °C for 60 min in a quartz tube of an electric furnace. As always, the wet ambient was formed by bubbling of N2 carrier gas through de-ionized water. Then, a Al<sub>2</sub>O<sub>2</sub> film in 50 nm thick was deposited by ALD at 300 °C. Finally, Au electrodes were deposited to form gate and backside ohmic contacts. The circular gate electrodes were 200 µm in diameter.

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### **Data availability**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Declarations** Conflict of interest The authors declare that there is no conflict of interest.

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