

Fabrication of Sub-45-nm Structures for the Next Generation of Devices: A Lot of Effort for a Little Device

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Guest Editors

Abstract

For the last four decades, the feature sizes of electronic devices for computers have been reduced by a factor of two roughly every 18 months. The result has been a tremendous increase in computational power and reduction in the cost of computing, as measured by cost per function, of nearly 30% annually, so that computations can be done for a billionth of the cost of using the technology of the 1950s. However, devices will soon be so small that the current technology used to produce them will have reached its limits, and the graininess of individual atoms will affect their behavior. This issue focuses on techniques to make tiny devices with dimensions under 45 nm (45 billionths of a meter) for the next generation of devices. Techniques start with coupling currently used 193-nm and 157-nm optical lithography with liquid immersion to reduce the effective wavelength. Other techniques include microprinting, self-assembly, templating, and using supercritical fluids to avoid the effects of surface tension while enabling solution-based processing at such small dimensions. The development of three-dimensional structures that are approaching this scale is also discussed. The methods presented will have an effect on many areas of technology, including, in addition to electronics, advanced sensor technology, energy conversion, catalysis, and nanoelectromechanical systems.

Keywords: lithography, self-assembly, supercritical fluids, nanoelectromechanical systems.

The silicon VLSI* juggernaut is approaching an interesting transition period. For the last four decades, progress in

*VLSI stands for very-large-scale integration, referring to electronic chips with 10^5 – 10^6 transistors onboard.

miniaturizing microprocessors has been on an exponential curve, with feature sizes being reduced by a factor of two roughly every 18 months. The result has been not only a tremendous increase in computational power, but also a substantial reduction in the cost of computing, as measured

by cost per function, of nearly 30% annually.¹ Today, we fabricate transistors at literally one-billionth the cost of 1950. This kind of progress is almost without precedent in human history. The printing press did not make books a billion times cheaper. Modern agribusiness did not make food a billion times cheaper. The loom did not make clothes a billion times cheaper. But VLSI did make transistors a billion times cheaper. As a result, the world as we know it has been remarkably changed over the last 50 years. The challenge now facing us is how to stay on that exponential curve, known popularly as Moore's law, for the next 50 years. It will be quite a trick.

There are three basic challenges to maintaining Moore's law: processes and materials that allow continued reductions in size, device physics at the nanoscale, and economics. The basic working assumption of the standard CMOS (complementary metal oxide semiconductor) transistor is that matter is continuous and uniform, and devices can be continuously shrunk without having to worry about the fundamental graininess of matter, the atoms. With device features measured in micrometers, this has been a reasonable assumption for four decades. As device structures shrink to well below 100 nm, this basic working assumption will completely break down in 10–20 years. It will be impossible to build a 10-nm device that works anything like the current CMOS transistor. It will be a nanodevice with new operating principles and physics. It will also require a completely new way of making it.

That is not to say that the challenges facing VLSI fabrication based on the current CMOS design for the next 10 years will be trivial. Far from it. The international roadmap for semiconductors predicts that devices at the 45-nm node will be in production by 2010, with 32-nm devices to follow by 2013.¹ Manufacturing of these devices will require new approaches to patterning, deposition, and etching as current techniques run into fundamental roadblocks. The winning technical solution must also be an economical one: the cost of scaling to smaller dimensions cannot raise the cost of computing, storage, or memory. Moreover, any new process technology for CMOS devices will need to be seamlessly integrated into the existing Si wafer fabrication infrastructure to be broadly adapted.

In this *MRS Bulletin* theme on nanoscale device fabrication, we focus primarily on recent developments that offer great promise for the fabrication of structures below 45 nm. Much of the discussion is framed in the context of integrated circuits and data storage, but the methods dis-

cussed will have an impact on many areas of technology, including advanced sensor technology, energy conversion, catalysis, and nanoelectromechanical systems (NEMS).

As features get progressively smaller and approach molecular dimensions, the clean separation between lithography, deposition, function, and material that we were used to dealing with begins to blur. In the old days, one had a lithography tool that could pattern metals or oxides and another set of tools and techniques that could put down gold or aluminum. One could then make a transistor or an interconnect and build a DRAM (dynamic random-access memory) cell or a microprocessor. In the new nanoworld we are entering, the patterning, desired function, preparation, and material must become much more connected.

One way of achieving this is to incorporate "bottom-up" approaches such as directed self-assembly to define the smallest device features in a way that allows their marriage to traditional "top-down" techniques to functionalize the features and complete the device hierarchy. Better still is a process that yields a patterned functional material directly from a self-assembled template. Both approaches are now possible, but every function we need will require us to engineer the entire process from lithography/patterning to materials selection. It is the steps along this path that we explore in this issue.

Our general approach is to describe work that ranges from the near-term to farther out as one goes through the issue. In the first article, Rothschild and co-authors talk about UV optical lithography, the workhorse of the industry. They describe a number of novel techniques based on lens immersion that demonstrate that 193-nm and 157-nm UV light can be used

to produce high-quality 32-nm features that will find application in large-area devices, nanophotonics, nano-biology, and molecular self-assembly.

In the next article, Stewart and Willson discuss a completely new approach for nanolithography, the use of nanoimprinting, with a focus on those techniques that are assisted by ultraviolet light. In ultraviolet-assisted nanoimprint lithography (UV-NIL), a low-viscosity photosetting polymer precursor is molded using a transparent master and cross-linked by UV exposure. The technique is low-cost, rapid, and has been demonstrated for sub-5-nm horizontal pattern resolution. While the primary focus is on pattern generation for sub-45-nm integrated circuits, including imprintable dielectrics, the concept has broad application in other areas, including biomaterials and NEMS/MEMS.

Hawker and Russell then discuss the use of block copolymer self-assembly as a platform for bottom-up pattern generation. Block copolymers spontaneously organize by microphase separation into a range of well-ordered morphologies with periodicities ranging from 5 nm to 50 nm. In a crude sense, it is how biological organisms such as spiders can use local rules to produce large ordered structures such as webs. Recent advances in directed and self-orienting assembly of block copolymers now allow nearly complete control of domain alignment, orientation, and registration. The authors show how one can use these materials to create templates and structures for addressable high-density media, among other applications.

In the next article, O'Neil and Watkins talk about how we can use supercritical fluids (SCFs) to produce novel nanostructures. The properties of SCFs blur the distinction between gases and liquids, enabling solution-based processing in the

very smallest of features without concern for limitations to flow or damage from surface tension. This situation is ideal for fabrication at the nanoscale. One application is conformal metal deposition in high-aspect-ratio features. Another is the combination of SCF processing with self-assembled templates to yield precisely defined metal oxide or carbon films directly.

Finally, Yang et al. show how to use the nonlinear two-photon effect to create a novel 3D lithography. Just as multiphoton effects can be used to create new types of microscopy, they can be used to create new types of lithography that yield 3D structures directly. While the technique cannot yet be used at the 45-nm length scale, 100-nm resolution is on the way, and it will provide a means for creating topographically complex substrates for integration with the device structures produced using the methods described throughout this issue. The ability to directly write complex structures is a compelling concept, and we thought it important to include it as part of the tool kit for nanostructured devices.

One of the pleasures of being the guest editors of a special theme on nanotechnology is that one can create an entire issue on things one finds fascinating. In this issue, we have done just that. We believe that you will find the work interesting and provocative, and the results well written and engaging. We suspect that, like us, you will be in awe of what is now becoming possible. We hope that you will enjoy reading this issue as much as we enjoyed putting it together.

Reference

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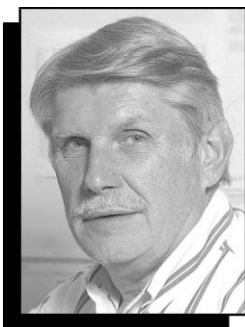
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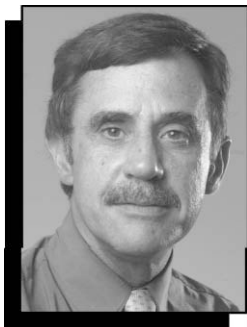


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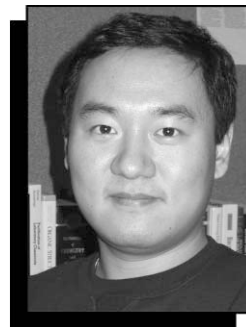


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