Microelectronics Packaging and Integration

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Guest Editors

Abstract

The focus of this issue of MRS Bulletin is to explore the impact of materials science and technology on microelectronics packaging and integration. Progress in microelectronics packaging has been intimately tied to the continuous advances made in the associated materials, process technologies, and design tools. This is especially true now, as packaging moves into an era driven by the need for complex system-level solutions. This issue is our attempt to present the current status of microelectronics packaging technology and integration and to highlight various perspectives on the future evolution of the field.

Keywords: microelectronics packaging and integration, microelectronic materials, technology roadmaps.

Introduction

The intent of this issue of *MRS Bulletin* is to review a range of microelectronics packaging challenges and the associated integration issues. Historically, microelectronics packaging has been driven primarily by the needs of the high-performance computing industry. However, with the advent of portable consumer electronics as the major application driver, the requirements for microelectronics packaging have been rapidly diversifying. This is especially true in the case of wireless and hand-held devices, where low-power and high-performance device technology coupled with cost sensitivity has resulted in a redefining of the role of infrastructure in microelectronics packaging. The result has been a greater push toward the rapid adaptation of system-in-a-package (SiP) solutions. Even in the case of high-performance computing, interconnects and packaging are reaching a critical point wherein interconnects, assembly, and packaging have become a significant factor in determining the cost and overall system performance of the device or module.

While our primary objective is to present a review of the status and future directions of various microelectronics packaging technologies, we can cover only a small spectrum of the many important topics. Microelectronics packaging is a diverse subject driven by the needs of myriad applications. For example, the packaging needs of high-performance microprocessors are quite different from those of hand-held devices like personal digital assistants (PDAs) and cellular telephones. However, most applications share the need for low power consumption, high performance, and low manufacturing cost. Along with high-performance computing, emerging applications in communications, transportation, and consumer electronics require enhanced packaging capabilities. Other important applications such as optical microelectromechanical systems (MEMS), storage devices, and medical electronics have their own unique sets of packaging requirements.

We invited a number of leading materials and device technologists to provide their views of critical aspects of microelectronics packaging and to offer their insights on future directions, especially on the materials involved and related processes. Given the diversity of microelectronics packaging and the problems to be addressed, this attempt is no doubt incomplete. However, we hope that we have provided a useful starting point for those seeking to better understand the challenges of this critical technology.

Leading the issue is a review by Atluri et al. on the critical aspects of high-performance microprocessor packaging. This team of Intel engineers shows how the package has evolved from a simple enclosure into a critical part of the overall system in a high-performance microprocessor assembly. As processor speeds move into the multi-gigahertz range, package design has become more significant. In fact, from an overall system-design view, the package has to be seen as a complex microassembly of a diverse set of materials and process technologies. Most all of, it is important to realize that the interconnection, assembly, and packaging of chips are not separate functions, but should be viewed as the incorporation of diverse materials into functional, integrated device structures.

To fully utilize the manufacturing advantages of complementary metal oxide semiconductor (CMOS) processing, there has been a sustained effort to produce complete system-on-a-chip (SoC) solutions. Even though SoC is conceptually the most desirable technical solution, true wafer-level integration of heterogeneous functionality has so far been difficult to achieve. For example, a brief look at the inside of a typical cellular telephone (Figure 1) highlights the issue. Despite the high degree of wafer-level integration, the number of discrete components still remains very high. However, on-wafer integration, if successful, allows for mixed-signal functionality, integrated passives (i.e., resistors and capacitors embedded in the packaging), and smart power-management tools. To accomplish this, there is a significant amount of activity in integrated passives and, increasingly, three-dimensional (3D) integration. Three-dimensional integration involves embedding transistors on multiple layers throughout the volume of the package, instead of confining the transistors to a single two-dimensional (2D) layer; the challenge of interconnecting devices on multiple levels adds significantly to the complexity of the process. To a certain degree, passive elements have been incorporated into integrated circuits (ICs). However, these passives are typically fabricated with standard semiconductor processing methods using materials such as doped monocrystalline or polycrystalline silicon, silicon oxides, and oxynitrides. As such, these integrated passives are located adjacent to the silicon substrate and consequently suffer decreased performance, especially in rf and high-speed applications. Thus, until high-performance passives can

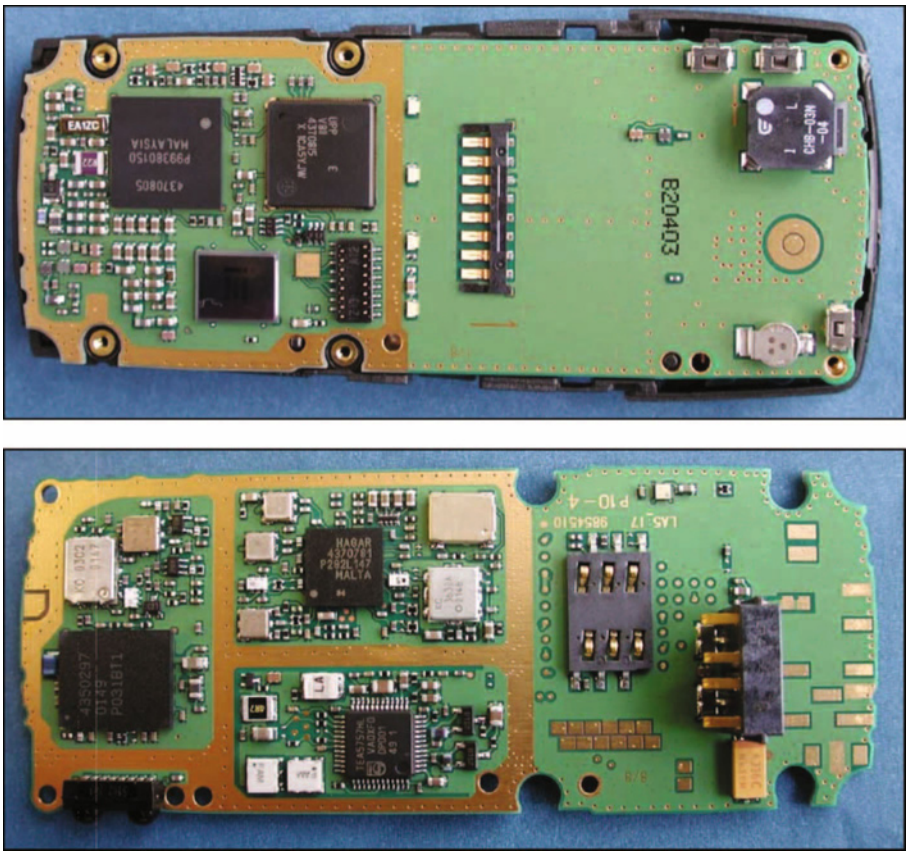

Figure 1. Photos of the interior of a cellular telephone, showing the large number of discrete components. Despite the high level of integration possible today, a cell phone still has hundreds of components and almost a thousand solder joints.

be readily integrated as part of the wafer fabrication process, the integration of passive and active elements at the package level (SiP) will be critical for continued increases in microelectronics performance.

While significant progress has been made in both 2D and multichip packaging, the development of true 3D ICs is still in its infancy. Wafer-level 3D integration can lead to interconnect, circuit, and system solutions that could result in high-performance devices. However, even for planar CMOS technology, the increased design complexity and long lead time to production often render SoC an impractical or cost-ineffective solution for many applications. This is especially true in the case of heterogeneous systems, where a combination of analog, digital, and rf functionality is required. Performance, cost, and time-to-market limitations also preclude SoC as a viable approach in many cases. SiP offers the most flexible solution. Where there has been tremendous progress in SoC development, it has been primarily for digital logic with limited analog and rf functionality.

Whereas SoC suffers from difficulties of mixed-signal functionality, packaging-driven approaches based on SiP do not have that problem. In fact, the well-established packaging infrastructure and low-cost manufacturing provide tremendous advantages for SiP in heterogeneous integration. It is anticipated that the advantages associated with SiP will make such multichip packages a solution of choice for a considerable period of time. In this regard, SiP-based technology has become the vanguard of true heterointegration.

Until recently, wireless and display devices have driven the integration of rf components, high-speed signal processors, sensors, and optical components on high-performance substrates. However, this is changing rapidly as new systems increasingly demand low-power, ultralight, and portable devices. This is where SiP-based 3D integration becomes relevant. SiP-based 3D integration is essentially a materials-based packaging technology. In their article, Ozguz and Yamaguchi review the materials requirements and challenges for 3D packaging of electronic and optoelectronic systems. Three-dimensional SiP requires the use of a variety of materials within a small volume. The materials selection for 3D packaging is critical from electrical, optical, mechanical, thermal, and manufacturability viewpoints. The materials combination depends also on the intended application for the 3D packaged modules. Three-dimensional packaged systems offer performance advantages that cannot be provided by planar implementation when materials are judiciously selected. But perhaps the biggest challenge for SiP is the development of an integrated design methodology that allows for a systematic approach to SiP product development. This would include all the tools necessary for a complete thermoelectromechanical analysis and evaluation of design requirements. Furthermore, it would facilitate intelligent partitioning of the system based on both technical and cost factors.

Packaging for solid-state power electronics is an important area that is often overlooked. In fact, power electronics provide the primary function of converting or controlling electrical energy according to the desired device or module requirements. Power-electronics components perform various essential power-conversion and control functions, including control of power levels, power densities, voltages, currents, frequencies, duty cycles, and chemical environments. Power components include motor drives; ac/ac, ac/dc, and dc/dc converters; and rf and microwave electronics. Given the voltages and current levels required for power-electronics applications, this area stresses materials requirements perhaps more than any other aspect of microelectronics packaging. Not only must the package protect the chip from environmental factors, but the packaging materials must also be capable of insulating the environment from current and voltage spikes associated with a power device. Shaw succinctly summarizes the materials science aspects of packaging high-power electronics in his article.

Many advances will be achieved only by integrating IC packaging more closely into the wafer fabrication or board assembly, since the interconnect solutions must be developed in a total system approach to design and manufacturing. This will cause quality and reliability issues to be further complicated as this move toward system integration develops, especially with MEMS and integrated optical elements. MEMS devices are delicate structures sensitive to damage due to handling or environmental influences. Their functionality depends on either sealing out the environment or being in direct contact with it in order to analyze its characteristics. Stress,

thermal load, and contaminants may change the operating characteristics of the MEMS device. Here, packaging technology is challenged to extend from microelectronics toward MEMS and micro-optical devices for telecom and optical markets. Most current methods heavily rely on single-chip packages derived from the microelectronics industry, wafer-level capping to enable the device to be packaged like an IC, or highly specialized packages designed to complement the function of the MEMS device itself. MEMS packaging is steadily moving toward chip-scale packages (CSPs) and flip-chip-based packaging solutions. Chip-scale packaging is done at the wafer or die level, while flip-chip technology involves the deposition of solder bumps on two separate die, then flipping one on top of the other to join them together. In this important and still-emerging area, we have two articles exploring packaging, materials, and reliability issues for MEMS devices. Jung provides an overview of MEMS packaging and various methods available to fabricate these sophisticated structures. Gooch and Schimert focus on two approaches to vacuum packages and the corresponding materials challenges.

Improvements in electrical performance and a reduction in the cost of packages both lead to a reduction in the number of steps in the packaging process. Chip-scale and wafer-scale packaging are the industry trends. Bakir et al. discuss progress in the development of high-density interconnects for substrate-compliant wafer-level packaging. Another area that poses extremely difficult materials and packaging challenges is high-speed digital (e.g., microprocessors, digital memory) and mixed rf devices (i.e., rf devices coupled with analog or digital components). The fundamental materials characteristics—dielectric constant, dielectric loss, conductivity, resistivity, moisture absorption, glass-transition temperature, strength, time-dependent deformation (creep), and fracture toughness—must be thoroughly understood for high-speed digital and rf device operation. Frear and Thomas highlight the key issues in electronic packaging for high-performance digital and rf devices.

As components move toward smaller and smaller dimensions, interconnects and packaging will have to be viewed with a different eye—not as two distinct functions, but as interwoven pieces of the same puzzle. The use of copper interconnects with low-κ dielectrics along with reduced feature sizes has already resulted in higher operating frequencies at lower voltages. With the reduction in feature sizes, thermal management at both the package level and board level has become a major issue. Most notable is the need for heat removal in applications with very high power dissipation. The problem of heat transfer is exacerbated by the close packing of the chips, the higher heat fluxes required (higher-power chips), and the need for reduced junction temperatures. Thermal issues will be more difficult to manage going forward, and they need to be viewed as a major bottleneck to further progress.

New Packaging Technology Challenges

One of the most difficult challenges faced by the microelectronics packaging industry is not a technical one, but a business one. Viable solutions here are as important as overcoming technical challenges. Advanced microelectronics packaging is both a labor- and cost- intensive enterprise. The changes occurring in the microelectronics packaging industry are in many ways an outgrowth of what happened to semiconductor device manufacturing during the 1990s. The move toward outsourcing of microelectronics packaging is rapidly gaining momentum, resulting in the growth of several dominant packaging foundries. The internal packaging efforts at a number of major semiconductor device manufacturers are shrinking, and the move toward wholesale outsourcing of packaging operations is only going to accelerate in the future. Ironically, this move away from vertical integration is happening as the distinct separation of wafer fab, packaging, and board assembly processes and services is becoming less clear. The package is no longer just an afterthought; it is an integral part of the total system solution. However, if there are to be two distinct entities, chip manufacturing and stand-alone packaging, both types of organizations must be able to interact to solve the myriad technology challenges while remaining economically viable.

As a partial response to these trends and to develop better and more coordinated roadmaps for chip-scale and wafer-level packaging, several key package tool vendors have formed consortia to accelerate the development of volume production with 300-mm wafers. The principal consortia in this area include the Advanced Packaging and Interconnect Alliance (APiA) and the Semiconductor Equipment Consortium for Advanced Packaging (SECAP). These are intended to enable back-end process and packaging equipment vendors to provide comprehensive tools and support with total packaging solutions for the chip-level and wafer-level packaging areas. APiA has established 300-mm pilot lines for developing solder bumping (the placement of solder balls on a wafer for wire bonding or flip-chip interconnecting), wafer-level packaging, and wafer-level interconnect processes. SECAP is working on delivering optimized process equipment for bumping, wafer-level packaging, and high-density interconnect technology. However, wafer-level packaging is still at a very early state in the packaging technology life cycle.

The 2001 International Technology Roadmap for Semiconductors (ITRS) identified several key challenges for the interconnect, assembly, and packaging areas. These major roadblocks are grouped into two segments: short-term for the ≥65-nm node (through 2007), and long-term for the <65-nm node, where solutions will be required in the time frame beyond 2007. The assembly and packaging grand challenges from the ITRS are listed in Table I. Each major challenge requires progress in the introduction of a number of new materials and process technologies for semiconductor assembly and packaging. For example, the introduction of Pb-, Sb-, and Br-free packaging materials must be accomplished, along with the use of lower-cost materials and processes to meet these requirements while providing improved reliability. The integration of new low-loss dielectrics along with substrate technologies that allow for high-frequency operation will be necessary. No doubt many materials-compatibility challenges will arise as these new requirements are addressed.

Technological advances will spur the growth of 3D interconnects. These advances will involve not just stackable packages, but the stacking of chips and wafers as well. Device stacking can materially reduce the distance signals must travel between chips, which in turn can improve performance while reducing product size. Future systems will continue to shrink in size and use less power. Larger amounts of memory and higher-speed data processing will be required to handle the increasing amounts of data used in broad-band applications. An alternative to shorter wires is, of course, optical or rf interconnects (chip-to-chip or perhaps on-chip). It is too early to know if or how this will be done. Suffice it to say that success will require a complex set of materials-based solutions to address the performance, reliability, and cost challenges associated with such a radical departure from current practice.

Even though the integration of chip, component, and packaging design tools is becoming essential, the gap between chip-scale and package design tools appears to be widening. The continuous migration of semiconductors to smaller features, higher frequencies, higher power densities, lower voltages, and the integra-

Table I: Grand Challenges in Microelectronics Assembly and Packaging.

Short-Term (feature size ≥65 nm, through 2007)	Summary of Challenges
Improved organic substrates	Glass-transition temperature compatible with Pb-free solder processing Increased wireability at low cost Improved dimensional control and lower dielectric loss to support low-cost embedded-passive and higher-frequency applications Improved planarity and low warpage at higher process temperatures Low moisture absorption
Improved underfills for flip chips on organic substrates	Improved flow, fast dispense/cure, better interface adhesion, lower moisture absorption Higher operating range (170°C) for automotive applications in liquid-dispensed underfills Improved adhesion, small filler size, and improved flow for mold-based underfills
Coordinated design tools and simulators to address chip, package, and substrate co-design	Mixed-signal codesign and simulation environment Faster analysis tools for transient thermal analysis and integrated thermomechanical analysis Electrical issues (power disturbs, EMI,[a] signal integrity associated with higher frequencies/currents and lower voltage switching) Commercial EDA[b] supplier support
Impact of Cu/low-κ dielectrics on packaging	Direct wire bond or solder bump to Cu Bump and underfill technology to assure low-κ dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion
Pb-, Sb-, and Br-free packaging materials	Lower-cost materials and processes to meet new requirements, including higher reflow temperatures Reliability under thermal cycling (stress and moisture)
Long-Term (feature size <65 nm, beyond 2007)	
Package cost that may greatly exceed die cost	Die cost continues to drop, while package cost continues to increase, but research investments in packaging are decreasing in the short term
Small, high pad count; high-frequency die	Array I/O[c] pitches below 50 μm Substrate wiring density to support >20 lines/mm Lower-loss dielectrics Skin effect above 10 GHz
Close gaps between substrate technology and the chip	Interconnect density scaled to silicon (silicon I/O density increasing faster than the printed circuit)
System-level design capability to integrated chips, passives, and substrates	Partitioning of system designs and manufacturing across numerous companies will make required optimization of performance, reliability, and cost of complex systems very difficult; complex standards for information types and management of information quality, along with a structure for moving this information, will be required

Source: 2001 International Technology Roadmap for Semiconductors (http://public.itrs.net).
[a] EMI = electromagnetic interference.
[b] EDA = Electronic Design Automation. The EDA industry provides products and services to chip and package designers/manufacturers.
[c] I/O = input/output interconnects

tion of mixed signals demands a very aggressive packaging technology roadmap. Otherwise, packaging will become *the* (not just *one*) limiting factor in the continued evolution of semiconductor technology. It is necessary to develop integrated design tools and simulation technology that will simultaneously consider items such as electrical characteristics, thermal dissipation, thermomechanical stress, physical requirements, and environmental impact. Such tools and technology are needed throughout the design process in order to reliably mount a chip in a package/module or a chip/package on a board. Support from commercial EDA suppliers is indispensable in this regard (the Electronic Design Automation industry supports chip and package designers with tools, products, and related services). The acceleration of the development of coordinated design tools and simulators has been identified as a major challenge by the ITRS. Materials development and characterization will be essential if truly integrated design tools are to become a reality.

Both SoC and SiP are solutions to system integration that are available today. Certainly, more tools and other infrastructure will be needed to fully realize their individual potential, but the basic building blocks are in place. For the longer term, an alternative solution may become available, at least for some classes of macroelectronic system-integration problems. Two trends suggest this potential. First, display technology has become more pervasive in the overall system and more microelectronics-like with the advent of active-matrix liquid-crystal displays (AMLCDs) and organic light-emitting diode display technology. As thin-film transistors (TFTs) are integral to the operation of these devices, it becomes attractive to consider what other functions can be implemented with the "free" transistors available from display fabrication. In this sense, such integration on a display substrate is analogous to the driving force for SoC. Of course, the dimensions and material performance of amorphous/poly-Si or organic TFTs cannot compete with those of advanced Si ICs. However, as the TFT technology improves, so will device performance. Probably more critical is to consider the problem from a system perspective and analyze what features can be implemented with TFTs—and whether doing so would provide sufficient cost, reliability, or performance benefits. The use of inferior TFT devices is counterintuitive to the IC industry. But, as the use of poly-TFT onboard driver ICs for LCDs has shown, there can be overall system advantages. This leads to the second trend that may help create

a macroelectronic system integration approach. The evolution of circuit-board technology has a similar history. Originally, the board functioned only as a substrate to interconnect the various components. But the constant demand for more performance at lower cost has led to the use of metal interconnect lines and dielectric layers for the fabrication of "free" embedded passive components. Board technology based on polymeric dielectrics offers the potential of compatibility with organic TFTs. Thus, significant built-in functionality may be possible at little extra cost or complexity. In the case of both display and board technology, some of the materials and processes could become part of a macroelectronic, system-on-substrate approach. However, the bigger driving force is conceptual. Once the size of the system has been determined by its intended function, smaller and smaller components may no longer be an advantage. Rather, using materials and devices integral to the fabrication process to reduce the system complexity and cost or improve its reliability may be much more beneficial. The macroelectronics approach to systems integration provides yet another opportunity to enhance system capability. Techniques for the fabrication of TFTs on polymeric substrates may lead to various fold-out features that make up in applications flexibility what they lack in performance capability. Fold-out features are created by integrating chips on a flexible substrate like Kapton (a polymer film) and then sandwiching the chips by folding the substrate in order to make the devices fit in a small volume.

Future Opportunities

In this overview, we have covered a range of topics. We could also touch on several other significant or emerging areas. For instance, advances in microelectronics, MEMS, and wireless devices promise revolutionary advances in medical electronics. The realization of these long-sought advances will be critically dependent upon the kinds of package advances (size, cost, reliability) described here. However, a further challenge in many applications will be delivering the desired functionality while achieving biocompatibility. This may be one of the most difficult challenges for the packaging community to overcome.

While perhaps not as daunting as *in vivo* operation, the desire for novel electronic form factors will add to the already formidable list of packaging materials technology issues. Examples include electronic textiles and large-area electronics. Systems based on such concepts represent a novel packaging challenge. Not only must the materials provide all of the attributes associated with the usual package requirements, but in addition, the "package" must be flexible, conformable, or perhaps even washable.

Large-area, printable electronics is another emerging area that can be expected to introduce new materials challenges at all levels. While display products are the best known example of large-area electronics, significant interest and development in other applications is occurring. These include rf tags, smart cards, and sensor arrays. Regardless of the end application, such systems comprise a "chip" that is from several square centimeters to perhaps several square meters in size. The underlying premise for this technology is that the electronic components can be fabricated by a printing-type technology rather than by conventional wafer fabrication approaches. For this concept to be viable, it is obvious that the "package" must also be fabricated by analogous, low-cost, high-volume methods. Novel concepts such as these promise to open entirely new fields of electronics development, with advances in interconnect, package, and assembly materials technology acting as key enablers.

For Further Information

The 2001 International Technology Roadmap for Semiconductors (ITRS) is a summary document on the needs of the semiconductor industry. The full document can be found on the Web at http://public.itrs.net. The sections relevant to this issue of *MRS Bulletin* are "Assembly and Packaging" and the ITRS public roadmaps Web site. The National Electronics Manufacturing Initiative Inc. (www.nemi.org) maintains a comprehensive roadmap (NEMI 2001 Roadmap) for a broad variety of electronics manufacturing technologies including components, packaging, and assembly. Similarly, the Electronic Industries Association of Japan (www.jeita.or.jp/eiaj/english/) maintains the Jisso Technology Roadmap 2000, which is relevant for interconnects, assembly, and packaging. However, starting with the 2001 ITRS, the assembly and packaging section is a worldwide coordinated effort and includes contributions from NEMI and EIAJ. However, these are mostly industry-driven initiatives to create awareness and stimulate development toward solving critical problems that cannot be solved by a single company or organization.

Several professional societies are active in the area. These include the IEEE Component, Packaging, and Manufacturing Technology Society (www.cpmt.org), the International Microelectronics and Packaging Society (www.imaps.org), and the Materials Research Society (www.mrs.org), which has presented a number of symposia on this topic. □

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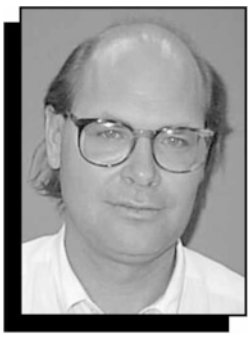

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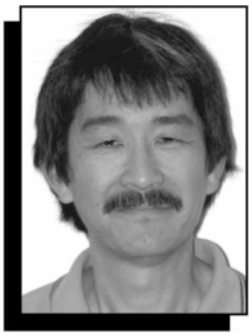

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