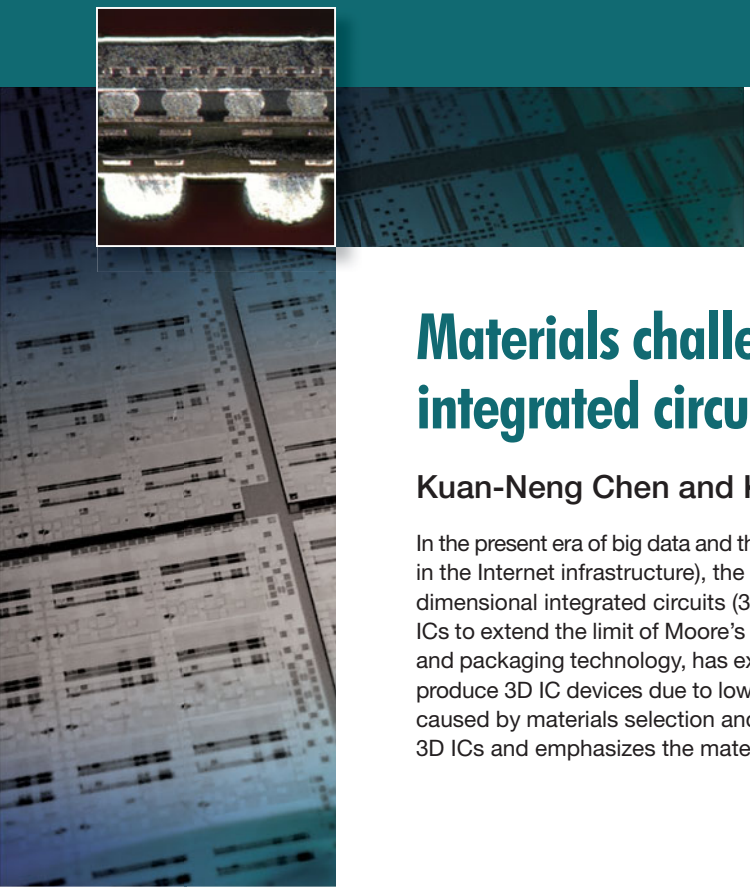

Materials challenges in three-dimensional integrated circuits

Kuan-Neng Chen and King-Ning Tu, Guest Editors

In the present era of big data and the Internet of things (the interconnection of computing devices in the Internet infrastructure), the fabrication of mobile and other electronic devices by three-dimensional integrated circuits (3D ICs) is receiving wide attention. The concept of using 3D ICs to extend the limit of Moore's Law of two-dimensional ICs, by combining chip technology and packaging technology, has existed for more than 10 years. However, we still do not mass produce 3D IC devices due to low yield and reliability, as well as high cost. Most problems are caused by materials selection and integration at the small scale. This issue offers a review of 3D ICs and emphasizes the materials challenges of this new technology.

Materials challenges

The miniaturization of semiconductor devices has been the driving force for research and development (R&D) in the microelectronics industries in the last several decades. This trend has resulted in the high usage of electronic devices in all aspects of daily life, manifested by the current ubiquitous presence of consumer electronic products. Nevertheless, in the near future, we will face the size limits of mobile devices, the need for higher power, and an increase in functional applications. Today, the iPhone is about six inches in length. As mobile phone technology develops to meet user expectations for more functions, increased power will be required. The amount of power available to a mobile phone is limited by the battery size, which cannot be too big, as well as by heat generation, which cannot be too high. It is unlikely that consumers will want future iPhones to increase much more in size. In addition to user demands for a smaller form, high reliability and low cost are also current, urgent challenges for materials selection and integration. The current basic designs of two-dimensional (2D) chip technology and packaging technology need to be reviewed such that future technology can address these challenges with high yield and reliability.

Recently, three-dimensional integrated circuits (3D ICs) have become a strong candidate to meet these challenges. Three-dimensional ICs are based on vertical integration, where two or more electronic components are homogenously or heterogeneously stacked and can be formed by chip-to-chip, chip-to-wafer, or wafer-to-wafer stacking.[1] In 2D ICs, the interconnects are horizontal and long, but in 3D ICs, most of the horizontal interconnects are replaced by short vertical interconnects. This not only offers high density integration, but also introduces heterogeneous integration of different functional materials and devices.[2] The endeavors of scientists and engineers have advanced 3D ICs from a research topic to the solution of certain advanced commercial products, such as complementary metal-oxide semiconductor (CMOS) image sensors, field-programmable gate arrays, and memories.[3]

An optical cross-sectional image of a test sample of the stacking of three components—two Si chips and a laminate substrate—is shown in **Figure 1**. The first level (lower) Si chip has Cu through-silicon via (TSV) technology. There are three levels of solder joints: a ball grid array of 250 μm diameter on the bottom row (unclear due to offset of the cross-section), flip-chip solder joints of 100 μm diameter in the middle, and microbumps of 20 μm diameter on the top, which are between two Si chips. **Figure 2** shows a synchrotron radiation tomography image of one 3D IC device sample. The blue arrows show the applied current path during an electromigration test to find the weak link for the system-level reliability. Electromigration is the enhanced atomic diffusion driven by a high electric current density. It induces open or short failures in metallic interconnects in microelectronic devices.

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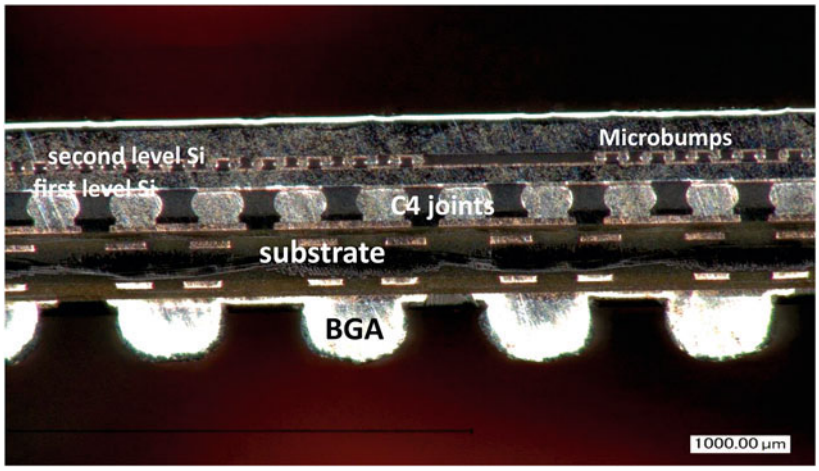

Figure 1. Optical image of the cross-section of a test sample with stacking of two Si chips on a laminate substrate. There are through-silicon vias in the first level Si chip. Three levels of solder joints are shown: ball grid array (BGA), C4 (controlled collapse chip connection) flip-chip joints, and microbumps. The thickness of the sample is about that of a US penny. Courtesy of Yingxia Liu, Department of Materials Science and Engineering, University of California, Los Angeles.

Electromigration failure will affect the use of 3D IC technologies in future products.

The success of 3D IC fabrication processes requires interdisciplinary cooperation. There are serious challenges in the mass production of 3D IC devices with regard to low cost, high yield, and excellent reliability. These issues are strongly related to materials. First, the materials characterization of bonded structures of solder microbumps and Cu TSVs cause concern, since these are both new packaging structures. Consequently, field data are unavailable, especially time-dependent data. Second, stress analysis of materials in heterogeneous integration is an intrinsic problem. More importantly, in 3D ICs, the induced stresses and strains may affect transistor performance. For example, the thermal expansion of Cu in a TSV will induce strain in the surrounding Si, thus creating a keep-out zone within which transistors should not be fabricated. Third, with the potential for 3D ICs in technology, future trends in research need to address a key concern: heat management. Researchers must determine how to reduce joule heating through careful materials selection and optimization, which will be challenging. Finally, the main concern for 3D ICs is how to achieve mass production through improvements in yield and reliability. No doubt, materials R&D is indispensable. All of these topics are covered in this issue of *MRS Bulletin*.

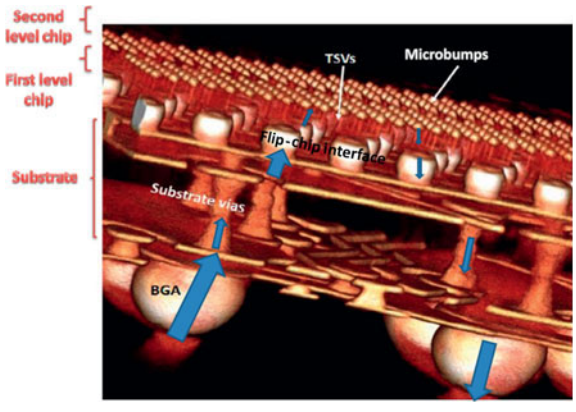

Figure 2. Synchrotron radiation tomography of a three-dimensional integrated-circuit test sample. Three levels of solder joints consisting of a ball grid array (BGA), a flip-chip joint, and microbumps are revealed. The two Si chips as well as the polymer-based substrate are invisible because of low x-ray absorption. Blue arrows depict the applied current path in the system-level electromigration test. Courtesy of Sam Gu, Qualcomm. Note: TSVs, through-silicon vias.

Issues of heat management and system level reliability

For thermal management in 3D ICs, when more chips are stacked and a dielectric underfill is used between chips, heat generation and dissipation become the most critical yield and reliability issue. Since a 3D device in operation is an open system, electric charges flow in and out. While the number of charge carriers in transport is conserved, entropy production is not. Joule heating is entropy production based on irreversible processes.[4] For conduction, Equation 1 shows that entropy production is the product of the conjugated flux of j (current density = coulomb/cm^2-sec) and the conjugated driving force of E (electric field = $j\rho$):[5]

$$\frac{TdS}{Vdt} = jE = j^2\rho, \quad (1)$$

where T is the temperature, V is the volume, dS/dt is the entropy production rate, ρ is resistivity, and $j^2\rho$ is joule heating per unit volume. The power from Joule heating is written as $P = I^2R = j^2\rho V$, where I is the applied current and R is the resistance of the sample. Thus, I^2R is Joule heating per unit time for the entire sample, and $j^2\rho$ is joule heating per unit volume per unit time of the sample.

In an Si device, Joule heating mainly comes from the transistors because Si has a much higher resistivity than metal interconnects such as Al, Cu, or solder. Producing low-power devices that are battery-operated is challenging. When chips having high density circuits are stacked closely together, the high rate of Joule heating combined with poor heat dissipation due to the dielectric underfill between chips makes heat management a critical issue in consumer electronic products. Low-temperature gas or liquid cannot be used to cool mobile devices, as with mainframe computers.

Heat dissipation or conduction depends on the thermal conductivity and temperature gradient because without a

temperature gradient, there is no thermal flux and, in turn, no heat dissipation. To facilitate heat dissipation, thermal TSVs can be used, which can be fabricated by direct Cu-to-Cu bonding. For the temperature gradient, we note that while a high-temperature gradient is better for heat conduction, it might lead to thermomigration (atomic diffusion driven by a temperature gradient) in the packaging structure causing another reliability problem.

For system level reliability, the electrical weak link is of concern because it will fail first. To find the weak link, electromigration testing is used. The 3D IC structure mostly comprises metal interconnections and wiring, and an example is given later on. Depending on the final structure, for example, in heterogeneous integration where optical elements are included, optical testing may need to be added. When performing electromigration testing, it is important to study the overall packaging system, rather than only one of the components since it is unknown, because we do not know which component is the weak link. The entire system will fail with the failure of just one component. The blue arrows in Figure 2 depict a circuit path that can be used for electromigration testing. For example, the test sample (Figures 1 and 2) failed immediately due to an open circuit upon the passage of a 100 mA current. When the applied current was kept at 50 mA, it failed after 10 hours. Synchrotron radiation tomography can be used to compare the images before and after failure in order to locate the failure site. It is possible to use an electrical method to detect the site where the open circuit occurs. By varying the applied current density, time, and temperature, we may be able to determine the mean time to failure and use the Weibull distribution function to characterize the statistical failure.

In this issue

The articles in this issue of *MRS Bulletin* expand upon the overview presented here on 3D ICs. The article by Iyer notes the absence of a viable lithographic method below the 8 nm node; this means we will need costly double exposure and etching methods to shrink features further.[6] This poses the question, "Why scale any further?" He proposes the concept of scaling the system—primarily the package and the board, rather than the chip. After introducing the viable choices to fulfill 3D ICs, he addresses different techniques highlighting the material and assembly challenges, sound materials selection, and innovative process integration for effective 3D integration.

Gu discusses materials challenges in wireless applications.[7] The current mobile revolution has enabled applications with more data bandwidth, more sensing, faster response, more process power, and smaller form factor. The benefits of 3D ICs are attractive, yet many materials challenges need to be addressed. Gu focuses on mechanical properties to reduce stress impact in device design, component warpage, and interconnect issues at the component level as well as board level reliability.

Koyanagi et al. focus on heterogeneous integration and key technologies, especially how various materials, devices, and technologies are integrated onto a Si substrate.[8] This enables 3D stacking of different kinds of chips, such as compound semiconductor chips, photonic chips, and spintronic chips, on CMOS chips. Examples including 3D microprocessors with self-test and self-repair functions, a 3D image sensor with extremely fast processing speed, and a 3D biochip fabricated by self-assembly and electrostatic temporary bonding are discussed. Finally, a technique to align and simultaneously bond more than 500 chips onto an electrostatic carrier wafer by the electrostatic force is presented.

Jiang et al. focus on the issue of stress in 3D IC integration.[9] The high aspect ratio and thermal mismatch between Si and Cu in a TSV induces complex stresses, which degrade the performance and reliability of 3D interconnects. They review current studies on thermal stresses by wafer curvature, micro-Raman spectroscopy, and synchrotron x-ray microdiffraction techniques. They explore the potential of material and processing optimization to build reliable TSV structures for 3D ICs. In addition to the effects of stress due to TSVs in this article, the fabrication of high-aspect-ratio TSVs has been widely explored and successfully demonstrated in the past several years. Critical topics of TSV fabrication include TSV drilling, insulator deposition, seed layer deposition, and Cu plating. Current technology can already achieve a reliable high-aspect-ratio Cu TSV with excellent performance and quality.[10,11] However, cost and throughput are both important concerns that need to be improved for the mass production of 3D integration.

Chen et al. discuss solder microbump selection and processing.[12] The thickness of the solder in the microbump is reduced from more than 10 microns to a range between a few microns and 10 microns. The volume reduction is approximately two to three orders of magnitude less than that of a traditional flip-chip solder joint. Consequently, the microbump is no longer a solder joint because the entire microbump is converted to intermetallic compounds of Cu-Sn and Ni-Sn, causing problems of brittleness. When multiple reflows are used in stacking technology, re-melting of previously formed joints must be prevented, which is non-trivial. The authors propose a clear solution to use direct Cu-to-Cu bonding.

Summary

As Moore's Law (the number of transistors in an integrated circuit doubles approximately every two years) nears its limits, 3D ICs not only provide a solution for "More Moore," but also create a new field for "More Than Moore," which means heterogeneous integration applications. The materials challenges discussed in this issue will propel more creative ideas and are anticipated to make significant contributions to the next generation of electronics products.

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