Contact materials for nanoelectronics

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Guest Editors

In this article, we review current research activities in contact material development for electronic and nanoelectronic devices. A fundamental issue in contact materials research is to understand and control interfacial reactions and phenomena that modify the expected device performance. These reactions have become more challenging and more difficult to control as new materials have been introduced and as device sizes have entered the deep nanoscale. To provide an overview of this field of inquiry, this issue of *MRS Bulletin* includes articles on gate and contact materials for Si-based devices, junction contact materials for Si-based devices, and contact materials for alternate channel substrates (Ge and III–V), nanodevices.

Introduction

It is well established that contact materials have a significant impact on the operation of electronic devices. In most cases, an ohmic contact, allowing unhindered current flow in and out of the device, is desired. Yet, in other cases, the contact is expected to perform a function beyond just passing current. Examples include transistor gate contacts, which determine transistor threshold voltage, and Schottky contacts, which act as rectifiers by blocking current flow in one direction. For a materials scientist, one of the key considerations in choosing contact materials is the stability of the interface between the contact material and the semiconducting film or substrate. This is because uncontrolled chemical reactions at the interface can modify the expected device performance. To realize good ohmic contacts, it is necessary to minimize the contact resistance (R_{co}) between the contact and the semiconductor materials. This has become especially important as contact areas have entered the deep nanoscale ($R_{co} = \rho_c/A_{cont}$), where A_{cont} is the contact area. The specific contact resistivity (ρ_c) depends on two key parameters at the disposal of a materials scientist—doping density (N) in the semiconductor and the barrier height (ϕ_B):[1]

$$\rho_c \propto \exp\left(\frac{4\pi\sqrt{\varepsilon_s m^*}}{h}\frac{\phi_B}{\sqrt{N}}\right), \quad (1)$$

where m^* is the carrier effective mass, h is Plank's constant, and ε_s is the semiconductor permittivity. The barrier height is ideally determined by the work functions of the contact/semiconductor pair. The Schottky-Mott theory provides that the barrier height, ϕ_B, is determined by the difference in the metal work function, ϕ_m, and the electron affinity of the semiconductor, χ_s (where $\phi_B = \phi_m - \chi_s$). However, it has been observed experimentally that the barrier height is a rather weak function of ϕ_m, and interfacial effects are the dominant factors that determine the value of ϕ_B. Such effects have been attributed to the phenomena of Fermi-level pinning or metal-induced gap states (MIGS) theory.[2,3] The engineering of these interrelated parameters (R_{co}, N, and ϕ_B) is the key to getting the desired device performance and is the central theme that cuts across the different types of devices being discussed in this issue.

Contact materials in Si-based devices

As Si devices have been scaled down in size, so has the contact area, resulting in increasing contact resistance. In fact, the overall contribution of contact resistance to the series resistance of metal oxide semiconductor field-effect transistors (MOSFETs) is expected to reach above 60% for the 32 nm node.[4,5] There are two ways to reduce the contact resistance at the silicide-Si junctions (current values are in the upper 10^{-8} Ω cm^2). The first way, traditionally used, is a higher

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active doping concentration (N) in the junction. However, this approach is limited by the solid solubility of the dopant in Si and has basically reached the limit of its benefit. An additional method to reduce ρ_c is to lower the barrier height at the silicide-Si junction (a barrier height <0.3 eV is needed to get ρ_c below $1 \times 10^{-8}\ \Omega\ cm^2$). The current preferred silicide (NiSi) forms relatively large barrier heights to n^+ and p^+ Si of 0.67 and 0.43 eV, respectively.[6] **Figure 1** summarizes the multiple approaches that can be leveraged to lower junction barrier heights to reduce ρ_c. One approach is to use a smaller bandgap material such as SiGe. In fact, SiGe junctions for p-channel devices have now been in production and provide a small reduction in the barrier height to Si (in addition to strain-enhanced mobility).[7] Another approach is to use dual-silicide junctions, shown as the black and red regions above the source and drain, respectively, in Figure 1. One silicide is optimized for n^+-Si and the other for p^+-Si. This approach has been reported using PtSi for a p-type metal oxide semiconductor (PMOS) and $ErSi_{1.7}$ for an n-type metal oxide semiconductor (NMOS) (ϕ_p,ϕ_n = 0.22 eV, 0.3 eV, respectively).[8] Yet another method takes advantage of Fermi-level pinning using surface passivation to set the effective barrier height.[9] More details on this topic are found in the article by Loh and Coss in this issue.

Increasingly, the introduction of new materials is driving improvements in Si transistor performance. One high profile example involving contacts is high-κ/metal gate materials.[10–17] Because of its lower carrier concentration compared to metals, polycrystalline silicon (poly-Si) has always exhibited a carrier depletion effect, but its impact on transistor performance became significant only as the SiO_2 gate dielectric thickness dropped below 2.0 nm. To eliminate the poly-Si depletion effect, metal gate materials with work functions comparable to heavily doped n-type silicon (4.05 eV) and p-type silicon (5.15 eV) were needed. The realization of these work functions using metal gates deposited directly on Hf-based dielectrics was not trivial even as hundreds of contact materials and compositions were evaluated[18–21] (see **Figure 2**). The vast majority showed some level of Fermi-level pinning, making it difficult to get the appropriate threshold voltage, especially with gate oxides approaching 1 nm equivalent oxide thickness.[22–24] Ultimately, two solutions emerged to overcome this issue. One was interface engineering using angstrom-level dipole interfacial layers to shift the effective work function to the desired values (4.0 and 5.0 eV for the n- and p-type silicon layers, respectively). A particularly effective oxide for NMOS was La_2O_3,[25–27] and for PMOS, Al_2O_3 was effective.[28] The second approach was to use a lower thermal budget flow to exert better control on the interface chemistry, particularly oxygen.[29,30] Please see the article by Wen and Chambers in this issue for more details.

Electrical contacts to nanoscale devices

Si nanowires and carbon nanotubes (CNTs) have attracted significant attention for nanoelectronic device applications (see **Figure 3**).[31–33] While CNTs offer exceptional mobilities, Si nanowires stand to benefit from the vast existing Si industry experience. The realization of Si nanowire devices, such as planar devices, will require low resistance contacts, controlled Fermi-level pinning, controlled doping levels and profiles, and appropriate barrier heights to be achieved. Two things make Si nanowire devices different from their planar counterparts: their large surface area-to-volume ratio and their exceedingly small size. Since contact resistance increases with the inverse of contact area, contact resistance can be large for nanowire devices. Further, obtaining ohmic contacts by relying on heavy doping of Si or Ge nanowires may not be a viable approach

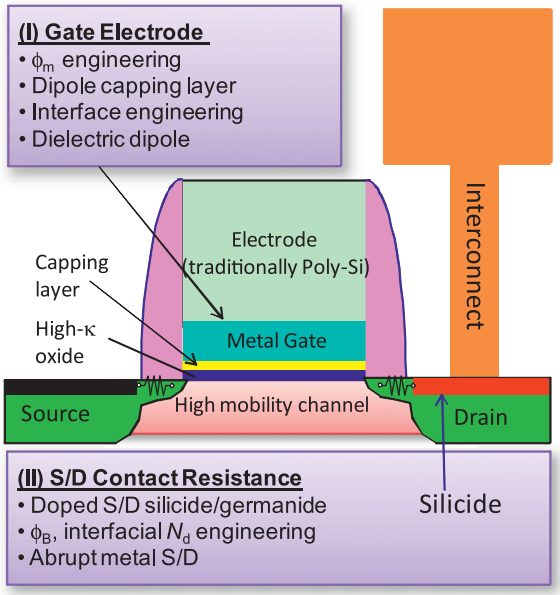

Figure 1. Research directions in nanoscale complementary metal oxide semiconductor devices. These directions include junction silicide engineering, gate stack engineering, and incorporation of alternate channel materials. S/D is source/drain, ϕ_B is the barrier height, ϕ_m is the metal work function, and N_d is the doping density.

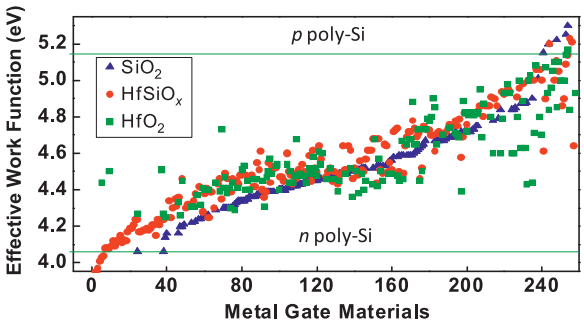

Figure 2. Effective work function of transistor gate contacts. The x-axis shows a large number of materials and compositions that have been tested as transistor metal gates. They include metals, conductive nitrides, silicides, oxides, and a combination of such materials.[18,19]

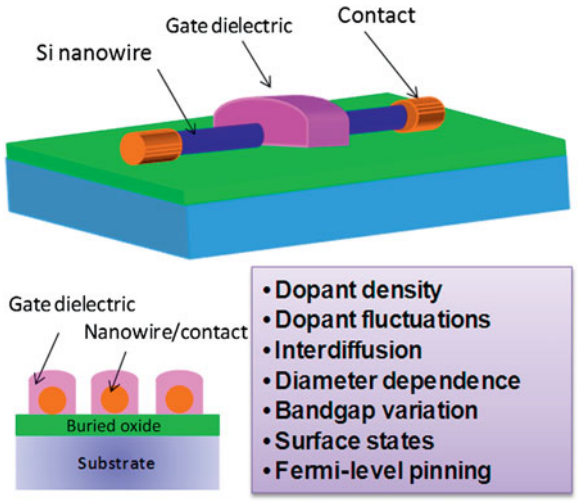

Figure 3. Potential issues in contact development for nanowire devices.

because variation in dopant concentration of only a few atoms would significantly alter the contact resistance.[34] Additionally, the realization of appropriate barrier heights may be equally challenging. This is because variation in Si nanowire size may lead to fluctuation in the bandgap[35–37] and because interfacial phenomena such as Fermi level, E_F, pinning and interface trap density can show dramatic differences from planar devices.[38–41] In fact, it has been reported that highly localized interfacial dipoles can form which, together with pinning of E_F, can result in nanoscale Schottky barriers 40% to 90% larger than the barrier at the corresponding bulk interface.[42] CNTs mostly form Schottky barrier heights, and surface treatments may be needed to reduce these barriers, while Si nanowires have been demonstrated with ohmic contacts.

Another type of nanoscale device being addressed here is the nanoelectromechanical switching device. Along with the common issues of contact resistance and barrier height, these devices will present a different set of challenges. These challenges include the requirement of low stress contacts and mechanical integrity of the contact interface with the active materials, particularly for the moving parts. Please refer to the article by Hussain and Song in this issue for more details.

Contact materials to Ge and III–V compounds

It is becoming clear that scaling of CMOS can only be realized by the continuous introduction of new materials (high-κ/metal gates,[43] SiGe-SiC,[44] Ge[45]/III–V channels[46]) and/or architectures (such as FinFET[47] [fin-shaped field-effect transistor] and triple-gated transistors,[48] and nanowires[49]). High mobility materials are strong contenders to replace Si in future generation low-power devices. These materials provide an intrinsic mobility enhancement in excess of five times over Si and hence pose a much more stringent requirement on contact resistance (to keep the external resistance, R_{ext}, a small fraction of the total resistance). To realize the true potential of devices with Ge and/or III–V channels, it is estimated that the contact resistivities for these systems should be below 10^{-8} Ω cm^2. One needs to comprehend the nanostructure of the metal-semiconductor contact and correlate this to the electrical properties of the contact. Interestingly, it has been demonstrated that most metals in contact with *p*-Ge have their work function pinned to the valence band of Ge, making it easier to form ohmic contacts to Ge for pFETs. However, for nFETs this Fermi-level pinning toward the valence band edge E_v results in a very high interfacial resistance. Some research groups have demonstrated promise in tuning this resistance by inserting a thin layer that modulates the pinning while being transparent and allowing high tunneling currents. Nevertheless, there is limited experimentally demonstrated low R_{co} for metal-Ge (*n*-type) contacts. For the III–V systems, there has been significant research on making low resistance contacts to an In-Ga-As semiconductor. The various approaches include the modulation of the interface to tune the Schottky barrier height and increasing the semiconductor dopant densities to 10^{20}/cm^3 levels by *in situ* doped junctions. It has also been surmised that the higher dopant densities create an interfacial dipole that further reduces the effective Schottky barrier height of the metal/III–V contacts. Additionally, modulation of the contact resistivity using a metal-insulator-semiconductor structure is being researched with limited, but promising, results. The article by Hu et al. in this issue summarizes the current understanding of contacts to Ge and III–V semiconductors and ongoing research directions.

Contact materials to thin-film transistors

Thin-film transistors (TFTs) have become a key technology for the electronic flat panel industry in the past 15 years, just as silicon chips have been a key technology for the electronics revolution. Multiple factories today produce millions of displays per year, with each display incorporating several million TFTs. The concept of the TFT and its potential utility significantly pre-dated the device that gave rise to the term transistor.[50] However, for many years, it was overshadowed by the astounding developments associated with the original bipolar transistor and the MOSFET. In more than six decades, thin-film transistors have undergone extensive evolution, development, and optimization. During this period of time, their intended uses went from switching systems to low-cost computer logic to flat panel displays, and new materials, structures, and fabrication techniques were introduced. TFT-based CMOS devices have also been demonstrated (**Figure 4**).[51,52]

For conventional semiconductors, including single crystal and amorphous silicon, ohmic contacts are most often formed using heavily doped semiconductor regions at metal-semiconductor interfaces. However, most oxide and organic TFT devices do not use doping to help form ohmic contacts. Instead, electrodes directly contact semiconductor regions with negligible or low doping. As a result, many oxide and organic TFTs have non-ohmic contacts. In fact, many oxide and organic semiconductor TFTs operate with Schottky source contacts, where gate field-induced charge is used to provide carriers not

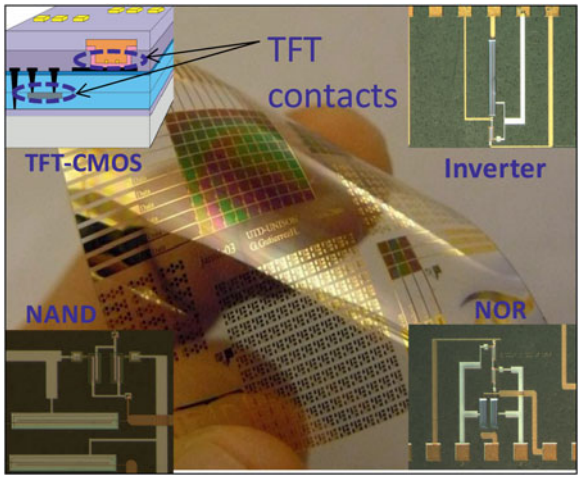

Figure 4. Complementary metal oxide semiconductor (CMOS) fabricated in thin-film transistor (TFT) technologies. Top left: Cross-section of the CMOS structure comprising both organic and inorganic thin-film transistors. Top right and bottom left and right: test structures.[51,52]

present from doping to allow tunneling between the source electrode and the TFT channel.[53] Despite the considerable progress made in recent years to improve the performance of organic and oxide TFTs, many issues are still poorly understood and poorly controlled. With decreasing device dimensions, the contact resistance as a part of the total device resistance will dominate compared with channel resistance, and therefore will play an important part in TFT operation, as well. This can be alleviated either by performing surface preparation to reduce the metal semiconductor barrier height or by increasing the effective carrier concentration of the surface, perhaps taking advantage of interface engineering.

Summary

The effect of contact resistance on the performance of devices is becoming more pronounced as devices are scaled to the nanoscale. This reality will require increased ingenuity on the part of materials scientists to control interfacial reactions and to engineer the interface. Judging from the rate at which new materials and processes have entered the microelectronic and nanoelectronic industries, the prognosis for finding solutions to mitigate these issues is quite good.

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