Protection and Control of
Modern Power Systems

ORIGINAL RESEARCH

Degradation state analysis of the IGBT module based on apparent junction temperature

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Abstract

The multi-chip parallel insulated gate bipolar transistor (IGBT) is the core device in large-capacity power electronic equipment, but its operational reliability is of considerable concern to industry. The application of IGBT online degradation state analysis technology can be beneficial to the improvement of system reliability. The failure mechanism of IGBT devices is discussed in this paper, and a technique for analyzing the degradation state of IGBT based on apparent junction temperature is proposed. First, the distortion consistency of the voltage rise time in various failures is discussed, and the junction temperature dependence of the voltage rise time is then demonstrated. Subsequently, an apparent junction temperature model based on the voltage rise time is established (the fitting accuracy is as high as 94.3%). From the high-frequency model in the switching process of the device, an online extraction technology of key parameters (e.g., voltage rise time) is developed. Finally, an experimental platform for IGBT degradation state estimation is established, and the feasibility of IGBT degradation state estimation based on apparent junction temperature is proved, especially the degradation of bonding-wire and the gate-oxide-layer. The experimental results show that the proposed IGBT degradation state estimation technique based on apparent junction temperature is a reliable online estimation method with non-contact, high accuracy, and comprehensiveness.

Keywords Degradation state analysis, Apparent junction temperature, Voltage rise time, High-frequency model

1 Introduction

The pre-diagnosis and health management system for major equipment is the frontier technique for the development of the global manufacturing equipment industry in this century [1, 2]. Power electronic devices, as the key devices for electric energy conversion, are widely used in industrial, military, aerospace, and other major equipment [2–4]. Because of the advantages of simple control, high power, high switching frequency, fast switching speed, and good thermal stability, IGBTs are used as the mainstream power electronic devices for much equipment [5]. However, the failure rate of IGBT increases with current density, voltage level, and switching frequency. Some research shows that 34% of converter system failures are caused by the failures of IGBT devices [1, 6, 7]. Therefore, the degradation state analysis technology of IGBT is important, as it helps detect the failures in advance and promote life extension for the system.

At present, research on the pre-diagnosis and health management system of major equipment mainly covers three aspects: condition monitoring, fault prediction, and health management [7]. Condition monitoring is based on fault prediction and health management, i.e., fault prediction is carried out through condition monitoring with high accuracy and low delay, and then health management can be realized. Condition monitoring mainly includes junction temperature estimation and

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degradation state estimation. Junction temperature estimation is the basis of degradation state estimation, while degradation state estimation is the key aspect. To discover defective IGBT modules in major equipment in a timely fashion, junction temperature detection and degradation state estimation of IGBTs have been extensively studied.

Various methods have been employed for detecting the junction temperature of IGBT modules, including optical non-contact measurement [8, 9], physical contact measurement [10], thermal impedance model prediction [11, 12], and temperature sensitive electrical parameter prediction methods [13–15]. However, the first two methods are not suitable for actual inspection systems as they entail long delays and require the device packages to be destroyed [9, 10].

It has been confirmed that there exists a one-to-one mapping relationship between the internal microphysical parameters of semiconductor physical devices and the device junction temperature [16]. For instance, the carrier lifetime increases with the rise in junction temperature, while the carrier mobility decreases. The characteristics of semiconductor materials exhibit a temperature-dependent variation that is correlated with the device's junction temperature, serving as the foundation for the temperature-sensitive electrical parameter extraction method. The device's internal parasitic parameters (parasitic capacitance and inductance) are also influenced by the device's degradation. Consequently, state detection of the chips can be achieved by using the temperature sensitive electrical parameter prediction method.

Reference [17] proposes a fault detection method for partial chip failure in multichip IGBT modules based on the turn-off delay time. The device failure is determined by the distortion of the turn-off delay time, but this method is only used for module-level fault detection, while the degradation degree of the internal chip cannot be accurately estimated. In [18], a health monitoring method for bond wires in IGBT modules is proposed based on voltage ringing characteristics, in which the bond wire degradation state is determined by the voltage pulse distortion rate on the anti-parallel diode. Reference [19] proposes a novel bond wire fault detection method for IGBT modules based on turn-on gate voltage overshoot, whereas [20] considers that the aging monitoring of the bonding-wire can be realized based on phase-frequency characteristics of differential mode conduction interference signals for the IGBT module. In [21], a novel online chip-related aging monitoring method for IGBTs is proposed based on the leakage current, while [22, 23] also investigate the monitoring of solder layer degradation in multi-chip IGBT modules based on combined TSEPs. However, most of the existing achievements focus on the degradation of a single type of device,

and it is impossible to comprehensively evaluate the overall degradation of the IGBT modules.

To solve the above problems, references [14, 15, 24, 25] propose a high-efficiency IGBT health state assessment method based on data-driven techniques, although the online extraction of many key electrical parameters required cannot be achieved.

To sum up, the following two difficulties still need to be overcome for IGBT module status monitoring:

- PN junction temperature monitoring of power electronic devices and characterization methods for device degradation; and
- device-oriented non-contact online monitoring.

Therefore, an IGBT degradation state analysis technique based on apparent junction temperature is proposed in this paper. First, a "voltage rise time t_{rv} – collector current I_c – junction temperature T_j" health model is established based on a calibration experiment. The apparent junction temperature of the device is then obtained based on real-time monitoring of the voltage rise time and the health model. Finally, the degradation of the IGBT is evaluated based on the apparent junction temperature overrun. More importantly, the principle of the high-frequency response current on the busbar caused by the rapid voltage change during the switching process of the IGBT device is discovered, while the high-frequency current information can be used to extract the voltage rise time during the turn-off process of the power electronic devices.

In Sect. 2, the key electrical parameters during the turn-off process are introduced and the temperature dependence of the voltage rise time is discussed. In Sect. 3, various failure conditions of the device in long-term applications are analyzed, and the degradation dependence of voltage rise time is discussed. In Sect. 4, the apparent junction temperature model based on voltage rise time is established, and a method for the degradation state estimation based on that temperature is proposed (including a monitoring scheme for key parameters t_{rv}). In Sect. 5, the IGBT degradation state monitoring simulation and experimental platforms are established in Saber and in the laboratory, respectively. Through simulation and experiment, the feasibility of degradation state analysis based on apparent junction temperature is demonstrated. Section 6 draws the conclusions.

2 Turn-off characteristics and junction temperature dependence of high-power IGBT devices

Multichip parallel IGBT modules are widely used in high-power applications because of their ability to handle high current and voltage. A typical

package structure of such modules, as exemplified by the Infineon module FF200R12KE4, is illustrated in Fig. 1a, while Fig. 1b shows the corresponding internal structure.

Different from low-power discrete IGBT devices, high-power IGBT modules consist of a group of IGBT chips in parallel with anti-parallel diode chips. Sub-modules are formed between multiple chips through aluminum bonding-wires and copper layers in parallel. Because of the existence of copper busbars between different sub-modules, parasitic inductance is inevitably introduced into the current channel. The equivalent circuit of an IGBT chip (the lower tube of the FF200R12KE4 module) containing the internal parasitic inductance is shown in Fig. 2, where L_{ac}, L_g, L_E, and L_e represent the parasitic inductances of the collector, gate, emitter and auxiliary emitter, respectively. R_g is the gate driving resistance, C_{gc} is the Miller capacitance, C_{ge} is the gate-emitter capacitance, and C_{ce} represents the collector-emitter capacitance.

2.1 Analysis of IGBT turn-off characteristics

The electrical waveforms during the IGBT turn-off process are shown in Fig. 3. The turn-off process can be mainly divided into 6 stages according to the characteristics of voltage and current. Before t_0, the IGBT is in the on state, and the gate drive voltage is V_+, while $I_g(t) = 0$, $I_c(t) = I_d$, and $V_{ce}(t) = V_{ce,on}$.

In the stage of t_0-t_1, the turn-off signal is given to the IGBT, so I_g changes rapidly. The gate capacitor begins to discharge, and the gate voltage $V_{ge}(t)$ drops rapidly, as:

$$V_{ge}(t) = V_+ - \Delta V_G * (1 - e^{-(t-t_0)/\tau_{G,L}}) \tag{1}$$

$$\Delta V_G = V_+ - V_- \tag{2}$$
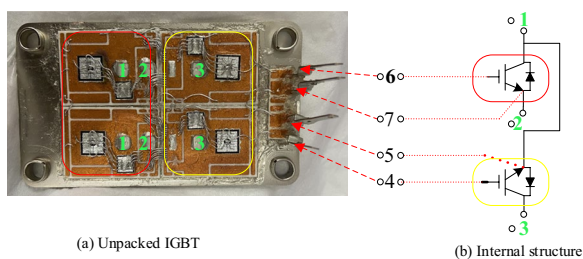
$$\tau_{G,L} = R_g * (C_{ge} + C_{gc}) \tag{3}$$
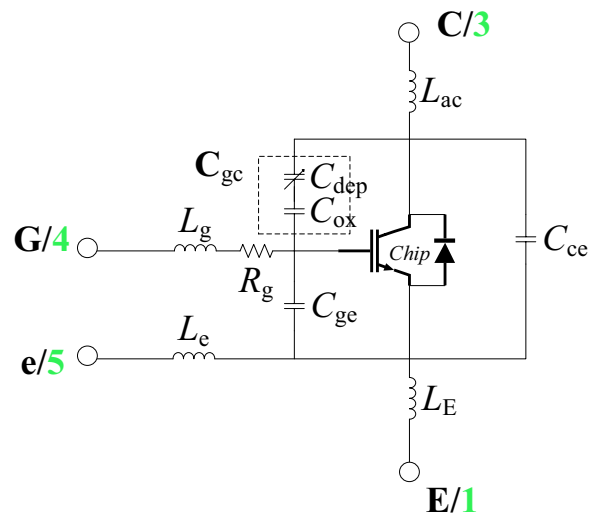
Fig. 1 Infineon IGBT modules (FF200R12KE4)

Fig. 2 Equivalent circuit of an IGBT chip

At the stage t_1-t_2, the gate voltage is clamped at the Miller plateau $V_{ge,L}$, and the gate current I_g maintains a constant output value. At this time, the gate current I_g charges the Miller capacitor C_{gc}, and the collector voltage $V_{ce}(t)$ rises slowly because of the relatively large C_{gc}. Thus:
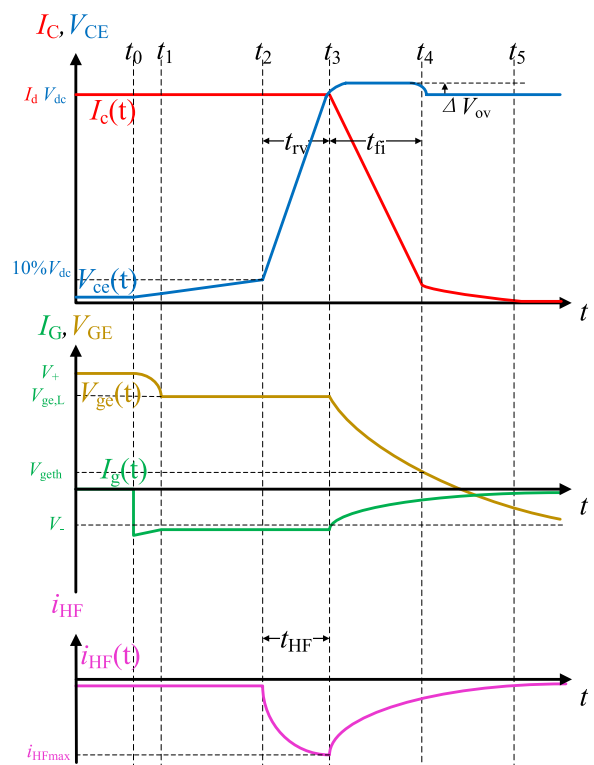
Fig. 3 The electrical waveforms of the IGBT turn-off process

$$V_{ge}(t) = V_{ge,L} \tag{4}$$

$$I_g = \frac{V_- - V_{ge,L}}{R_g} \tag{5}$$

At the stage t_2–t_3, $V_{ce}(t)$ gradually becomes higher than $V_{ge}(t)$, and it can be considered that the Miller capacitance is relatively small. At this time, the IGBT desaturation officially begins, and the collector voltage V_{ce} rises rapidly with its rising slope expressed as:

$$\frac{dV_{ce}(t)}{dt} = -\frac{dV_{gc}(t)}{dt} = -\frac{I_g}{C_{gc}} \tag{6}$$

At the stage t_3–t_4, the collector voltage $V_{ce}(t)$ rises to V_{cemax}, and the freewheeling diode is forward-biased. The load current I_c starts to transfer from the IGBT to the diode.

At the stage t_4-t_5, the gate voltage $V_{ge}(t)$ keeps decreasing, and so does the collector current I_c. At this time, the charges stored in the IGBT are gradually recombined.

At the stage after t_5, as the tail current decreases, the gate voltage $V_{ge}(t)$ continues to decrease until $V_{ge}(t) = V_-$.

According to the definition of the electrical characteristics of the semiconductor power device, t_2-t_3 is the voltage rise time t_{rv}.

2.2 Junction temperature dependence of voltage rise time during the turn-off process

In the initial stage of the IGBT turn-off process, the gate voltage decreases to 0. Since the inductive load current cannot be abruptly changed, the collector current remains at the magnitude of the on-state. At the same time, the collector voltage rises rapidly to the power supply voltage, the device is reverse biased, and the space charge region formed by the P base region/N base region is subjected to high voltage stress.

Assuming that the carrier recombination in the N base region can be ignored, the turn-off waveform of the IGBT is analyzed. The distribution of free carriers (holes) in the N base region is linear, as shown in Fig. 4, and can be expressed as:

$$p(y) = p_{WNB+} (1 - \frac{y}{W_N}) \tag{7}$$

During the initial stage of the turn-off process, the hole distribution curve does not change. However, as the space charge region widens, the hole concentration P_e at the edge of the space charge region increases [26]:
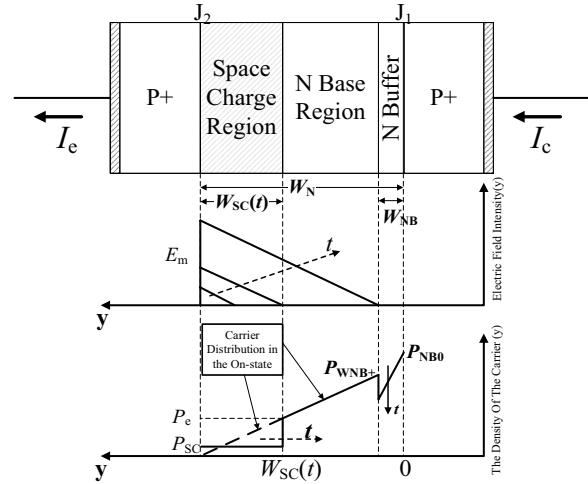

Fig. 4 The scavenging process of carriers in the n-base region during the turn-off process

$$p_e(y) = p_{WNB+} (\frac{W_{SC}(t)}{W_N}) \tag{8}$$

The number of charges removed because of the widening of the space charge region is equal to the number of charges reduced by the collector current, i.e. [27]:

$$J_{C,ON} = qp_e(t)\frac{dW_{SC}(t)}{dt} = qp_{WNB+}\left(\frac{W_{SC}(t)}{W_N}\right)\frac{dW_{SC}(t)}{dt} \tag{9}$$

$$W_{SC}(t) = \sqrt{\frac{2W_N J_{C,ON} t}{qp_{WNB+}}} \tag{10}$$

The relationship between the collector voltage V_{ce} and the space charge region width $W_{SC}(t)$ is [26, 27]:

$$V_{ce}(t) = \frac{q(N_D + p_{SC})W_{SC}^2(t)}{2\varepsilon_S} \tag{11}$$

The hole concentration P_{SC} in the space charge region is related to the collector current density $J_{C,ON}$, i.e.:

$$p_{sc} = \frac{J_{C,ON}}{qv_{sat,p}} \tag{12}$$

According to (10)–(11), we can obtain:

$$V_{ce}(t) = \frac{W_N(N_D + P_{SC})J_{C,ON}}{\varepsilon_S p_{WNB+}} t \tag{13}$$

In summary, during the device turn-off process, the voltage rise time can be expressed as [27]:

$$t_{rv} = \frac{\varepsilon_S p_{WNB+} V_{cemax}}{W_N(N_D + p_{SC})J_{C,ON}} \tag{14}$$

$$J_{C,ON} = \frac{I_c}{A_c} \qquad (15)$$

ε_s is the relative permittivity, $v_{sat,\,p}$ is the hole saturation drift velocity (about $10*10^7(300/T)^{0.87}$) [26], N_D is the doping concentration, and A_c is the chip area.

It can be found that the voltage rise time of the IGBT gradually increases with the increase of junction temperature according to (12)–(15).

3 Degradation characteristics of power device voltage rise time

Junction temperature fluctuation is one of the key factors in the failure of IGBT modules. Because of the mismatch of thermal expansion coefficients between different materials, the junction temperature fluctuation will cause huge shear stress inside the module, which can lead to the rapid failure of the IGBT module. The failures of IGBT modules are mainly divided into the following two categories: failures related to IGBT packaging and those related to IGBT chips, as shown in Fig. 5.

The failures related to the IGBT package mainly include bonding-wire degradation, solder layer degradation, heat sink degradation. Bonding-wire degradation is the most common. The failures related to the IGBT chips are mainly reflected in the gate-oxide-layer degradation and gate drive degradation. Gate-oxide-layer degradation is the most common. It is found that the voltage rise time of the IGBT gradually increases with the degradation, and this is universal for all degradation types.
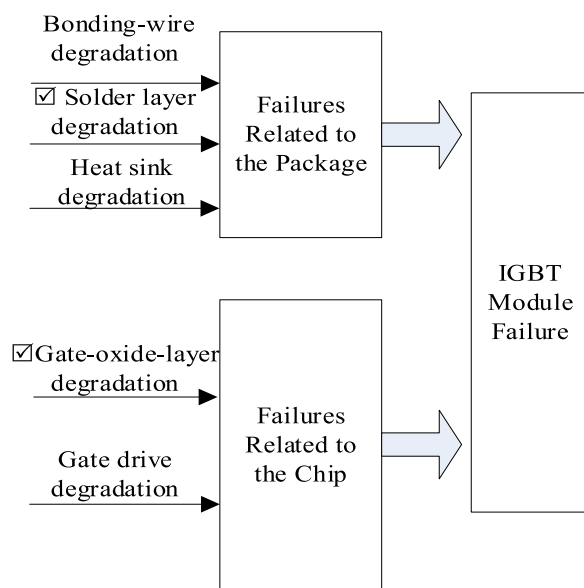
3.1 Failures related to the package
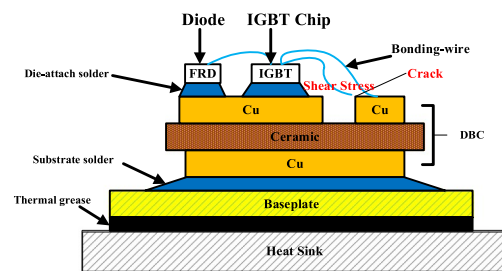#### 3.1.1 Bonding-wire degradation

The bonding-wire is one of the weakest links in IGBT modules. It is continuously impacted by temperature fluctuations during long-term operation, and this can lead to cracks in the solder joints between the bonding-wire and the silicon chip connection point, and eventually break or fall off. The schematic diagram of the failure of the IGBT bond wire is shown in Fig. 6. In actual operation, the falling off of one bonding-wire will cause the current to re-equalize, which will accelerate the falling off of other bonding-wires and cause the failure of the IGBT module.

The internal equivalent circuit of the IGBT considering the bonding-wire is shown in Fig. 7, where R_e and R_E are the parasitic resistances of the auxiliary emitter and the emitter, respectively. R_W and L_W are the equivalent resistance and inductance of the bonding-wires, respectively. V_g is the drive voltage, and V_{ge} is the gate-emitter voltage. Because of the structure of the device, the IGBT also contains parasitic capacitances, in which C_{dep} is the depletion layer capacitance, C_{ox} is the gate-oxide-layer capacitance, and C_{gc} is the gate-collector capacitance composed of C_{ox} and C_{dep} [28, 29].

As shown in Fig. 7, each metal emitter region of the module is connected to the emitter terminal through N bonding-wires. If the equivalent resistance of a single bonding-wire is R_W', the equivalent terminal resistance of the whole bonding-wire part is:

Fig. 5 The main failure types of the IGBT
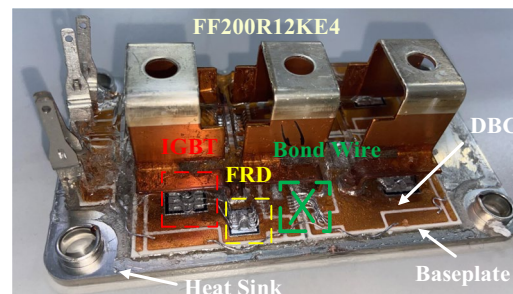
A. IGBT Bonding-wire Degradation

B. Schematic Illustration of IGBT Bonding-wire Degradation

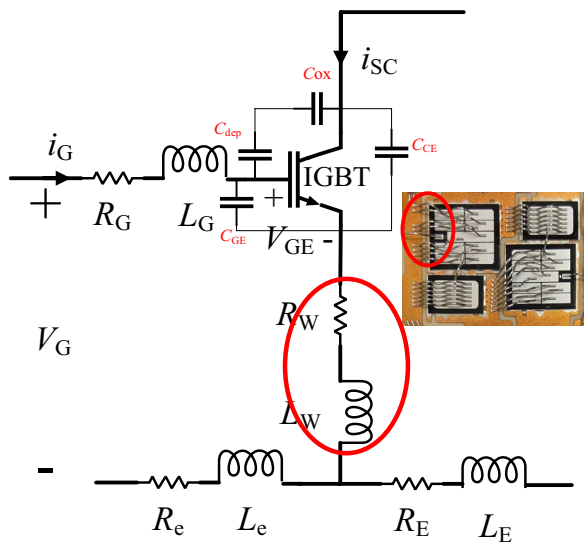**Fig. 6** IGBT bonding-wire degradation

Fig. 7 Internal equivalent circuit diagram of IGBT module

$$R_W = \frac{R'_W}{N} \tag{16}$$

During normal operation of the IGBT, temperature fluctuations will occur because of the unavoidable thermal shock. This will lead to the falling off of the bonding-wires. When there are only M bonding-wires left (M < N), the equivalent resistance of the bonding-wires is:

$$R_W = \frac{R'_W}{M} \tag{17}$$

Other parasitic parameters of the IGBT module do not change with the break of the bonding-wire. According to (16)–(17), when the bonding-wires of the IGBT deteriorate and fall off, the equivalent resistance R_W of the bonding-wires in the IGBT increases, and at the same time, the gate-driven current I_g decreases.

At the stage t_2-t_3, when the IGBT begins to desaturate, the collector voltage V_{ce} rises rapidly, and the gate voltage is shown as [30]:

$$V_g = I_g(R_g + R_W + R_e) + (L_W + L_e)\frac{dI_g}{dt} \tag{18}$$

According to (6)–(18), the voltage rise time in the turn-off process is affected by the deterioration of the bonding-wires. As the bonding-wires gradually degrade and fall off, the gate-driven current I_g (I_g is negative) decreases, and then the voltage rise time becomes longer.

3.1.2 Solder layer degradation

On the one hand, the solder layer connecting each layer of the IGBT module plays the role of electrical connection and mechanical support, while establishing the heat dissipation channel of the module. The realization of the module functions all depends on the reliable connection provided by the solder layer. The continuous thermal network model (Cauer model) reflects the physical conduction process of heat capacity of semiconductor devices with internal thermal resistance and can be established when the material properties of each layer are known. As shown in Fig. 8, each layer of the module (chip, chip connection, substrate, etc.) can be represented by an independent RC unit.

The failure evolution process of the solder layer is shown in Fig. 9. The thermal expansion coefficient of the solder layer is different from those of the silicon chip and the copper layer. Thus, when the device is heated, the expansion sizes of the solder layer, the silicon chip and the copper layer are also different. Different expansion sizes cause the solder layer to be subjected to shear stress during the operation of the IGBT. This will also change with the junction temperature fluctuation. The solder layer will be stretched and squeezed to different degrees under the action of shear stress, and eventually, cracks will occur. As the device operating time and junction temperature increase, the cracks continue to grow and form voids, which eventually lead to IGBT failure. At the same time, cracks in the solder layer lead to cracks and delamination. These increase the thermal resistance between the silicon chip and the copper substrate, and the heat dissipation of the IGBT will be affected.

When the transferred power loss P(t) and the case temperature T_C are known, the junction temperature T_j can be expressed as:
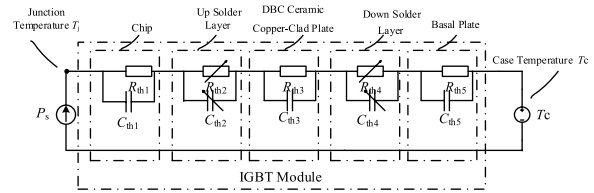

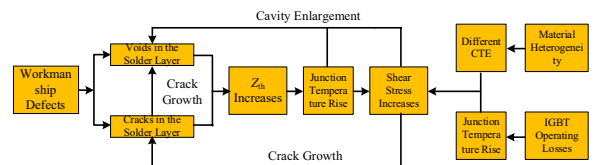**Fig. 8** Continuous thermal network model of IGBT

Fig. 9 Evolution of solder layer degradation

$$T_{\mathrm{j}} = P(t) \sum_{i=1}^{n} Z_{\mathrm{th}}(i) + T_{\mathrm{C}} \qquad (19)$$

As the solder layer degradation becomes severe, the equivalent thermal resistance will gradually increase. When the device case temperature remains unchanged, the device junction temperature will further increase, which is reflected in the increase of the voltage rise time t_{rv}.

3.1.3 Heat sink degradation

The heat sink degradation mainly includes the failure of the thermal conductive layer and the failure of the heat sink.

To improve the heat dissipation capability, IGBT power modules are installed on the air-cooled or water-cooled radiator through heat dissipation silicone grease. During long-term operation of the IGBT, the performance of the heat-dissipation silicone grease may gradually degrade or even fail. The failure of the IGBT cooling system mainly includes the failure of the thermally conductive layer or the failure of the radiator. The failure of the heat sink causes the heat dissipation performance of the IGBT to decrease, resulting in a gradual increase in the junction temperature, which is then reflected in the increase in the voltage rise time t_{rv}.

3.2 Failures related to the chip

3.2.1 Gate-oxide-layer degradation

Semiconductor devices such as IGBTs can be regarded as series or parallel systems composed of multiple components or materials [29]. In these systems, there are many solid-phase interfaces. Under the action of electrical, thermal, physical, and chemical stress, interface effects are generated, resulting in interface fatigue failure. The most common failure reasons are the time-dependent dielectric breakdown (TDDB) and the injection of hot carriers. The time-dependent dielectric breakdown means that when the electric field applied to the MOS gate-oxide-layer is lower than its intrinsic breakdown field strength, intrinsic breakdown is not caused, but the gate-oxide-layer breaks down after a certain time. The injection of hot carriers is caused by the injection of high-energy electrons and holes into the gate-oxide-layer, which will result in damage to the gate-oxide-layer.

The abrupt change of collector-emitter voltage during turn-off is mainly affected by the Miller capacitance C_{gc}. As shown in Fig. 2, the Miller capacitance C_{gc} is mainly composed of the depletion layer capacitance C_{dep} and the gate-oxide-layer capacitance C_{ox}. The degradation of the gate-oxide-layer capacitance is the main reason for the gate-oxide-layer degradation. The above capacitances can be determined as [31]:

$$C_{\mathrm{gc}} = \frac{C_{\mathrm{ox}} C_{\mathrm{dep}}}{C_{\mathrm{ox}} + C_{\mathrm{dep}}} \qquad (20)$$

$$C_{\mathrm{ox}} = A\alpha \frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} \qquad (21)$$

$$C_{\mathrm{dep}} = A\sqrt{\frac{qN_{\mathrm{D}}\varepsilon_{\mathrm{si}}}{2(V_{\mathrm{ce}} - V_{\mathrm{geth}})}} \qquad (22)$$

where A is the total chip area, α is the oxide layer overlap ratio, t_{ox} is the oxide layer thickness, $\varepsilon_{\mathrm{ox}}$ is the oxide dielectric constant, $\varepsilon_{\mathrm{si}}$ is the silicon dielectric constant, and q is the quantity of electricity.

At present, the main metal material in power semiconductor devices is aluminum, and most of the gate-oxide-layer capacitance is formed by the Al-SiO$_2$ interface. Because of the large-area erosion of SiO$_2$ by Al, the particle concentration of the SiO$_2$ layer changes, which manifests as an increase in the equivalent dielectric constant $\varepsilon_{\mathrm{ox}}$ of the gate-oxide-layer, and leads to device failure. The reaction is shown in (23) as an exothermic reaction, which can make the local temperature exceed 557 °C to form aluminum and silicon alloys. Then the gate of the IGBT will rapidly break down or become short-circuited at high current.

$$4\mathrm{Al} + 3\mathrm{SiO}_2 \rightarrow 2\mathrm{Al}_2\mathrm{O}_3 + 3\mathrm{Si} \qquad (23)$$
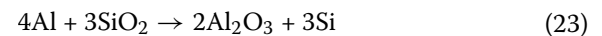
With the evolution of gate-oxide-layer degradation, the equivalent dielectric constant $\varepsilon_{\mathrm{ox}}$ increases, and the Miller capacitance C_{gc} increases, which is manifested as an increase in the voltage rise time t_{rv}, as shown in (6), and (22)-(23).

3.2.2 Gate drive degradation

As shown in Fig. 7, the gate resistance R_{g} is integrated into the IGBT module. However, as the long-term thermal cycle and power cycle, R_{g} gradually increases, while the gate-emitter drive voltage V_{ge} and drive current I_{g} decrease. According to (6) and (18), it can be found that the voltage rise time during the turn-off process is affected by the degradation of the gate resistance. With the degradation of the gate drive resistance, the gate drive current I_{g} (I_{g} is negative) decreases, which causes the collector voltage to rise more slowly (voltage rise time becomes longer).

4 Degradation state estimation of devices based on apparent junction temperature

All types of IGBT degradations can result in the increase of voltage rise time and deviations from the apparent junction temperature model. Therefore, in this paper, the

degradation state estimation of IGBT based on apparent junction temperature is proposed.

4.1 Apparent junction temperature model based on voltage rise time

It can be found that the voltage rise time in the turn-off process of IGBT is closely related to the junction temperature, and the junction temperature can be represented by the collector current and the voltage rise time, according to (7)–(15).

The healthy IGBT module is calibrated first and then the t_{rv}—I_c curve model is established, and can be expressed as:

$$T_j = f\left(I_c^2, I_c, \frac{1}{t_{rv}}\right) = \alpha_1 I_c^2 + \alpha_2 I_c + \beta \frac{1}{t_{rv}} + \eta \quad (24)$$

α_1, α_2, β, and η are constants which are related to the device itself. The curve is the "original" model of the corresponding power electronic device, reflecting the relationship between t_{rv}, I_c, and T_j.

For the device to be tested, it is only necessary to input the corresponding collector current and voltage rise time into the "original" model, and the output is the apparent junction temperature T_{js}. Although this junction temperature is not the real junction temperature, it (i.e., T_{js}) can be used to express the degradation state of the IGBT. In general, when $T_{js} > T_{jmax}$ (the maximum junction temperature allowed by the chip), it can be determined that the IGBT is degraded and needs to be replaced. The process is shown in Fig. 10.

4.2 Measurement feasibility of voltage rise time during turn-off

Based on high-frequency pulsed signals (coherent with t_{rv}) induced on inductive elements in power electronic circuits, an online detection method of voltage rise time based on a high-frequency pulse signal is developed in this paper, and the accurate extraction of voltage rise time is realized.

In real converter systems (e.g., non-isolated DC/DC BOOST and BUCK circuits, motor drive systems, etc.), when the power electronic devices are turned off, the voltage at both ends of the devices will be mutated, resulting in the voltage mutation of inductor components or motor windings. It has been proved that the voltage mutation process, namely the voltage rise time, is closely related to the degree of junction temperature and degradation.

Based on the above situation, an online detection method of voltage rise time is proposed based on the transient high-frequency model of the switching process. In fact, the high-frequency model is composed of a high-frequency differential-mode model and a high-frequency
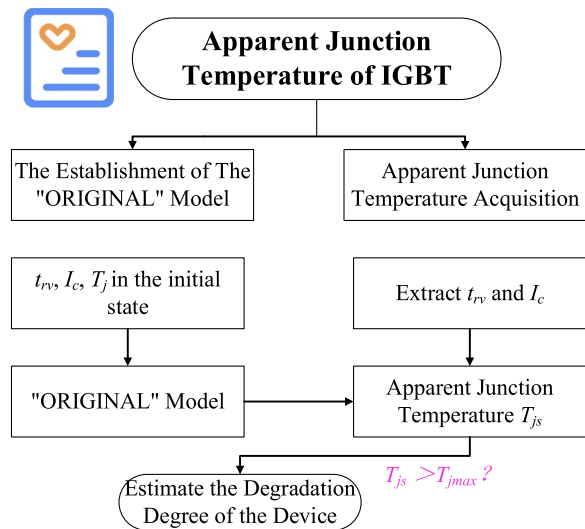

Fig. 10 Degradation estimation flow of IGBT devices based on apparent junction temperature

common-mode model. However, according to our research, the start and end points of the high-frequency pulse are not affected by the high-frequency common-mode model, so it can be neglected. Therefore, only the high-frequency differential-mode model is discussed below.

During the rapid turn-off process, a high-frequency pulse signal i_{HF} (t_{HF} corresponding to t_{rv}) will be generated on the inductance of the application circuit. Therefore, the detection of the voltage rise time can be replaced by the detection of the high-frequency pulse signal. This will greatly reduce the detection difficulty and cost.

Most power electronic conversion systems can be equivalent to the following three parts: ① equivalent voltage source $U_s(t)$; ② other circuit components; and ③ inductance equivalent circuit.

The equivalent voltage source is composed of the power supply and power electronic devices, the other circuit components are the remaining components, and the inductive equivalent circuit is the inductive load in the circuit.

At high frequency, the inductance equivalent circuit can be represented by two branches in parallel. Branch 1 consists of an equivalent inductance L_2 and an equivalent resistance R_2 in series, while branch 2 consists of equivalent capacitance C_1 and equivalent resistance R_1 in series. The whole high-frequency equivalent circuit is shown in Figs. 11 and 12, taking the respective BOOST circuit and H-bridge inverter circuit as examples.

When the power device is turned off, the equivalent capacitance of branch 2 is charged by the high-frequency pulse current. From the calculation, the equivalent
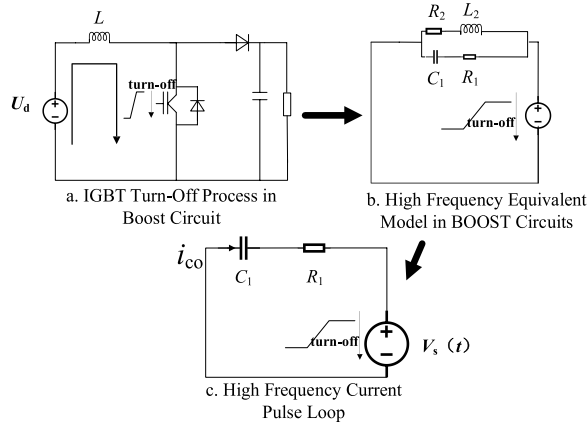
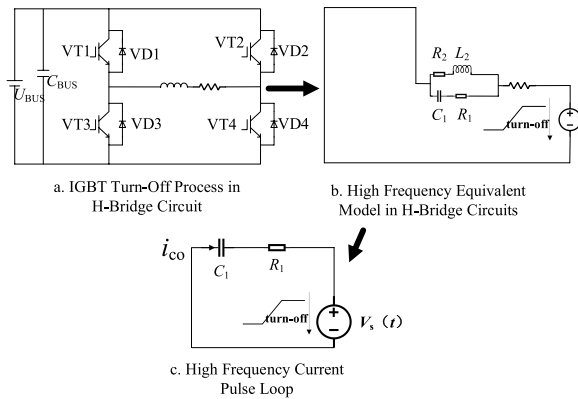**Fig. 11** High-frequency equivalent circuit model of BOOST circuit

Fig. 12 High-frequency equivalent circuit model of H-bridge circuit

voltage source voltage and high-frequency current are shown in Fig. 13. The voltage excitation is $\Delta U_{\mathrm{L}} = -V_{\mathrm{ce}}$, and the leading edge of the high-frequency pulse current during the turn-off process is expressed as:

$$i_{\mathrm{c}}(t) = (e^{-\frac{t}{RC}} - 1)\frac{CV_{\mathrm{cemax}}}{t_{\mathrm{HF}}} \tag{25}$$

The back edge of the high-frequency pulse current during the turn-off process is expressed as:

$$i_{\mathrm{c}}(t) = -\frac{U_{\mathrm{s}}(t_1)}{R_1}e^{\frac{t_{\mathrm{HF}}-t}{R_1 C_1}} \tag{26}$$

From the time difference between the leading edge and back edge of the entire high-frequency current pulse signal (differential method), the voltage rise time can be accurately extracted. The resulting signals are shown in Fig. 14, where the red, blue, and green curves represent the gate-emitter voltage, the collector-emitter voltage, and the high-frequency pulse current, respectively.
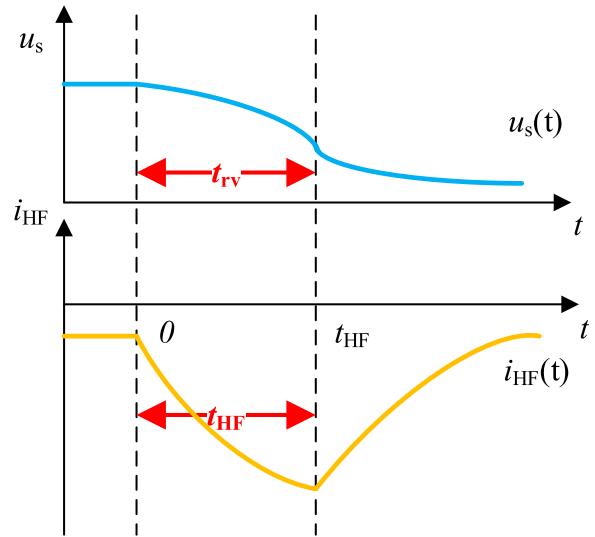
Fig. 13 The consistency of high-frequency pulse signal and voltage mutation during the turn-off process
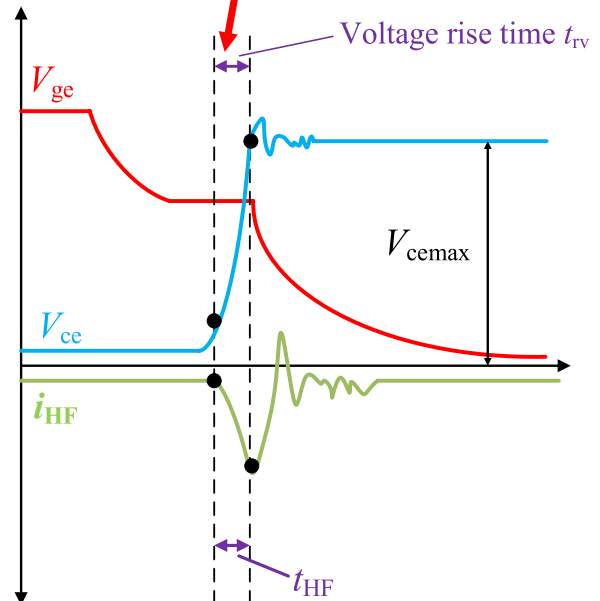

Fig. 14 Extraction and verification of voltage rise time based on high-frequency pulse current signal

It is also noted that the high-frequency isolation sensor used in the experimental platform for online extraction of voltage rise time is very cheap, and the high-frequency pulse current signal can be extracted by non-contact from the output current through the high-frequency isolation sensor. The sensor is mainly composed of three parts: a magnetic focusing ring, a low-frequency current detection unit, and a high-frequency electromagnetic coil.

The oscillation frequency of the high-frequency pulse current signal is in the MHz level, so the Rogowski coil is used. The Rogowski coil is composed of a magnetic ring and a high-frequency electromagnetic coil. Based on the principle of electromagnetic induction, the high-frequency magnetic field gathered in the magnetic ring is converted into voltage signals for output. It has the characteristics of high bandwidth, high signal-to-noise ratio, and low cost. The low-frequency current detection unit is realized by the Hall principle, and the low-frequency magnetic field gathered in the magnetic ring can be converted into a voltage signal for output.

As shown in Fig. 15, the high-frequency and low-frequency components pass through the virtual oscilloscope and data processor, and the voltage rise time t_{rv} is extracted in real time.

5 Experimental demonstration

In the IGBT turn-off process, the generated high-frequency pulse current signal is consistent with the voltage rise time, so the pulse signal can be used as the basis for the IGBT voltage rise time extraction.

Although the increase in voltage rise time can be caused by various types of device degradation, gate-oxide-layer degradation in chip degradation and bonding-wire degradation in packaging degradation are the key types in actual operation (they are more prone to failure).

To verify the sensitive relationship between the voltage rise time and degradation during the turn-off process of

the module, the apparent junction temperature based on the voltage rise time can be used to evaluate the degradation degree of the device, especially the degradation of the bonding-wire and the gate-oxide-layer. The theory is verified on the Saber simulation platform and the IGBT health state detection experimental platform in the laboratory.

5.1 Simulation

The circuit used for simulation is presented in Fig. 16a, and consists of four IGBTs, four diodes, a 1200 V DC power supply, an 8 mH inductor, and a 4.4 uF capacitor. To examine the turn-off process, voltage and current signals are extracted by employing a double-pulse test on the circuit. The double-pulse test is implemented with VT1 in the on-state, while VT2 and VT3 are in the off-state, and VT4 is triggered by two successive turn-on signals separated by an interval of 0.11 ms. The waveforms of the double-pulse test are presented in Fig. 16b, from which the voltage and current waveforms during the turn-off process are extracted.

5.1.1 Bonding-wire degradation

In this paper, the IGBT is modeled based on the fitted transfer characteristics, which are input into the Saber software. The modeling process is shown in Fig. 17.

In the study, the bonding-wire degradation is simulated by increasing the parasitic resistance between the IGBT gate and the auxiliary emitter (Corresponding to 1, 2, and 3 in Fig. 18). The double-pulse test is applied to the IGBT
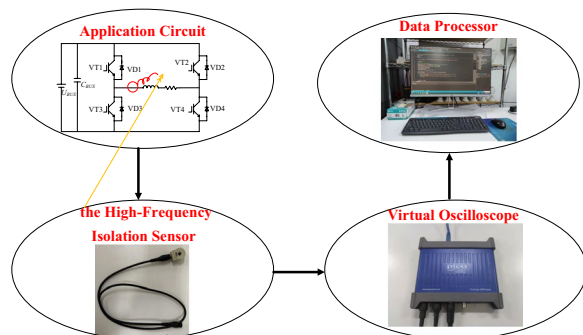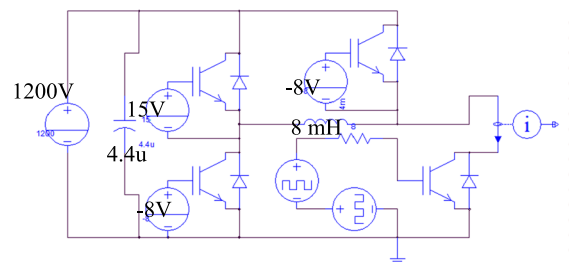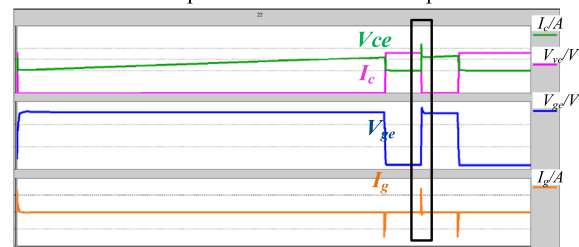

Fig. 15 Schematic diagram of online voltage rise time extraction

a. Simulation platform based on double pulse test

b. Electrical diagram of simulation

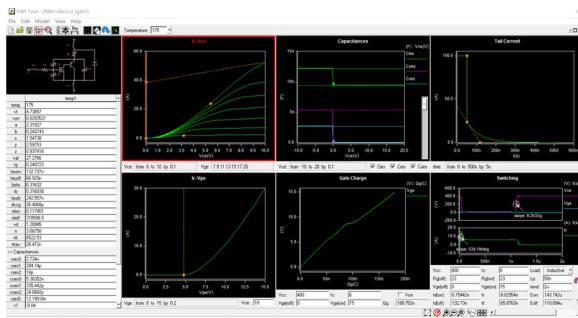**Fig. 16** Test circuit and electrical curves in the Saber Sketch
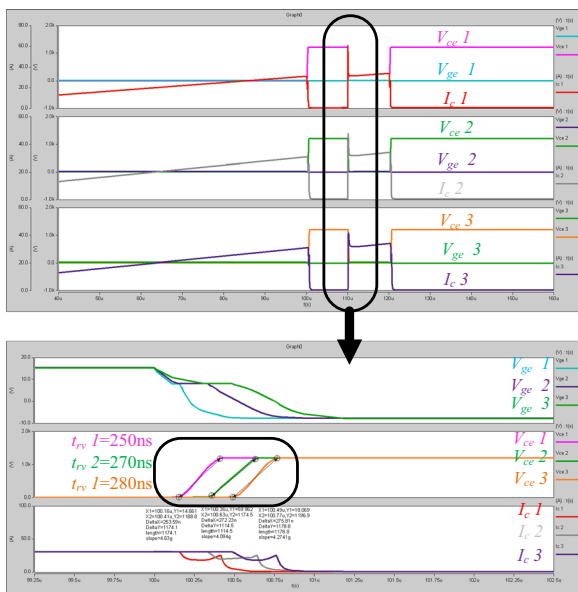
Fig. 17 The IGBT modeling process in Saber Sketch

Fig. 18 Voltage rise time under different bonding-wire degradation

Fig. 19 Voltage rise time under different gate-oxide-layer degradation

A. IGBT Health Status Detection Experiment Platform   B. Circuit Diagram of Experimental Platform

Fig. 20 Experimental platform and test circuit

module, and the results with different bonding-wire degradation degrees are shown in Fig. 18.

The results show that with the deterioration of the bonding-wire, the voltage rise time gradually increases. When the voltage rise time is input into the " original" model, the apparent junction temperature will exceed the maximum junction temperature T_{jmax}.

5.1.2 Gate-oxide-layer degradation

In the study, gate-oxide-layer degradation is simulated by increasing the Miller capacitance C_{gc} (corresponding to 1, 2, and 3 in Fig. 19). The double-pulse test is applied to the IGBT module, and the results with different gate-oxide-layer degradation degrees are shown in Fig. 19.

The results show that with the deterioration of the gate-oxide-layer, the voltage rise time increases significantly. When the voltage rise time is input into the "original"
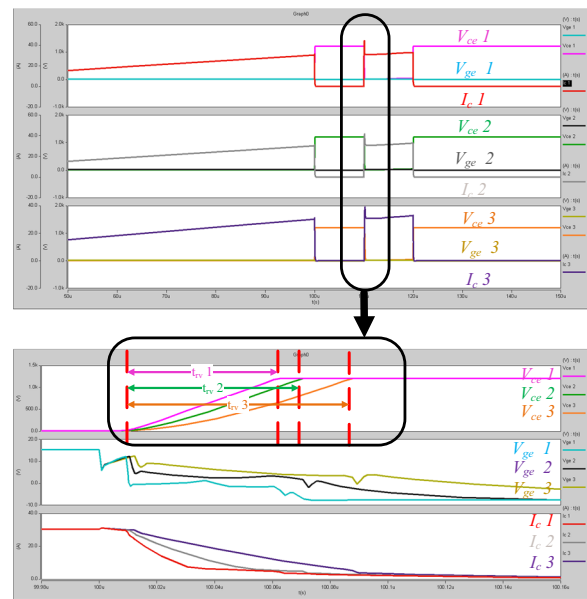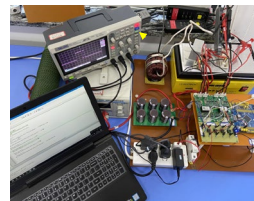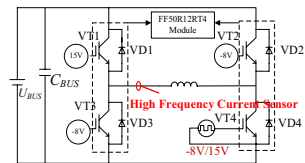
model, the apparent junction temperature will exceed the maximum junction temperature T_{jmax}.

5.2 Experimental

The IGBT health status detection experimental platform based on dual-pulse testing is built as shown in Fig. 20. The voltage rise time of the IGBT is obtained through the high-frequency current sensor, and the voltage rise time is input into the established apparent junction temperature model. Then, the degradation degree of the IGBT can be evaluated based on the apparent junction temperature overrun, while the apparent junction temperature model can be established according to (24) and the calibration experiment.

In the experimental platform, two intermittent gate signals are applied to the gate of the IGBT device (VT_4). Then the voltage and current waveforms in the turn-off and turn-on processes can be extracted (VD_1 remains on-state, VD_2 and VD_3 remain off-state.).

5.2.1 Bonding-wire degradation

In the experiment, the bonding-wire degradation is simulated by cutting the bonding-wire of the IGBT. The double-pulse test is performed on the IGBT module, and the results with different bonding-wire fracture conditions are shown in Fig. 21.

According to (24) and the experimental results, based on the multivariate linear fitting algorithm, the apparent junction temperature model (27)–(28) is established, and the key parameters in the model are per-unitized. The model is shown in (28), where the reference values are: $T_{jb} = 30$ °C, $I_{cb} = 20$ A, and $t_{rvb}^{-1} = 0.00330033$ /ns^{-1}. The fitting degree of the model is 94.3%, which is a reliable degree.

$$T_j = -0.017 I_C^2 + 3.786 I_C - 64893.759 t_{rv}^{-1} + 179.975 \tag{27}$$

$$\dot{T}_j = -0.222 \dot{I}_C^2 + 2.524 \dot{I}_C - 7.139 \dot{t}_{rv}^{-1} + 5.999 \tag{28}$$

According to the experimental results and the apparent junction temperature model, the apparent junction temperature variation based on voltage rise time is shown in Fig. 22.

The experimental results show that the voltage rise time increases gradually with the bonding-wire degradation. When the voltage rise time corresponding to the bonding-wire degradation is input into the "original" model, the apparent junction temperature will exceed the original maximum junction temperature $T_{jmax} = 130$ °C. At the same time, with the deepening of the bonding-wire degradation, the apparent junction temperature will further increase.
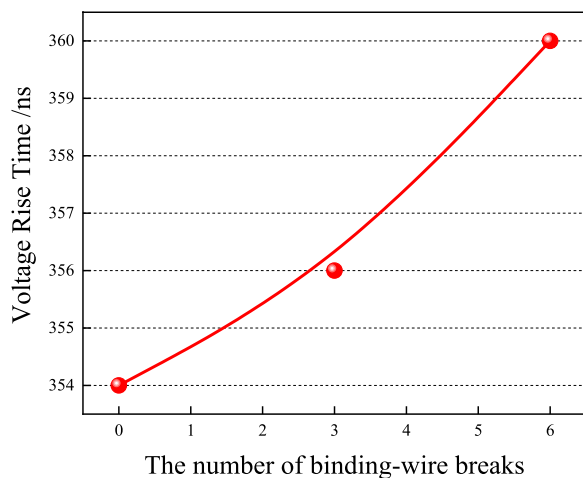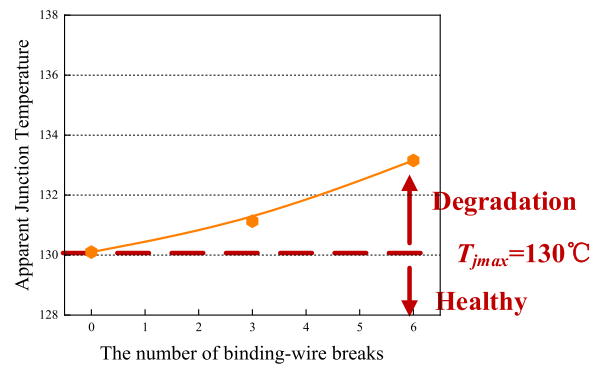

Fig. 22 Apparent junction temperature based on voltage rise time

5.2.2 Gate-oxide-layer degradation

In the experiment, the gate-oxide-layer degradation is accelerated by continuously applying a 75 V gate-emitter bias to the IGBT (with an interval of 3 h each time, and after 20 h of accelerated deterioration, the device is completely failed). The IGBT module is tested with double pulses at different collector currents and accelerated aging times, and the results are shown in Fig. 23.

From the experimental results and apparent junction temperature model (26)-(27), the variations of apparent junction temperature based on voltage rise time with different degradation states are shown in Fig. 24.

The experimental results show that, with the gate-oxide-layer degradation, the voltage rise time gradually increases. When the voltage rise time is input into the "original" model, it can be found that the apparent junction temperature will exceed the maximum junction temperature $T_{jmax} = 130$ °C. At the same time, the apparent junction temperature deviates more and more from the maximum junction temperature with the deepening of gate-oxide-layer degradation.
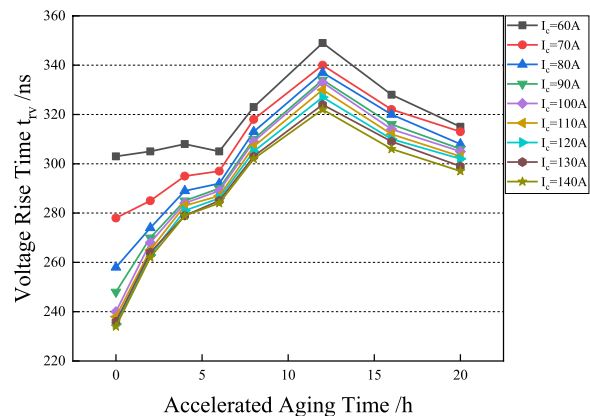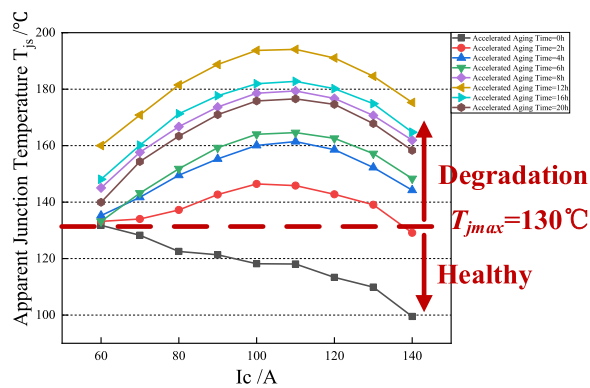

Fig. 21 Voltage rise time of IGBT with different numbers of bonding-wire breaks (130 °C and 100 A)

Fig. 23 Relationship between voltage rise time and gate-oxide-layer degradation

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Fig. 24 Relationship between apparent junction temperature and gate-oxide-layer degradation

To sum up, when the IGBT is degraded, the voltage rise time will be much longer than that of the IGBT in a healthy state, and all forms of degradation can be characterized by the apparent junction temperature overrun.

6 Conclusion

In this paper, the failure types and mechanisms of IGBT modules are discussed, and combined with the temperature dependence of the key characteristic parameter (e.g., voltage rise time) during the turn-off process, the degradation state analysis based on apparent junction temperature is proposed. For the most common chip degradation (gate-oxide-layer degradation) and packaging degradation (bonding-wire degradation), Saber simulation and IGBT health status detection experiments are carried out. The simulation and experimental results show that the method proposed is valuable, and in particular:

(1) Universality. The relationship between the voltage rise time of the IGBT and various types of degradation has been revealed and proved. More importantly, the apparent junction temperature based on the voltage rise time can be directly used to predict the IGBT degradation state.

(2) Non-contact online detection. The principle of high-frequency pulse current caused by the voltage mutation at both ends of the device during the turn-off process is discovered, and the detection of voltage rise time is replaced by the detection of the high-frequency current pulse.

In summary, the IGBT degradation state estimation technique based on apparent junction temperature proposed in this paper can be applied to power electronic devices' health state estimation in industrial production. This can effectively avoid catastrophic accidents caused by sudden device failures.

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