ORIGINAL RESEARCH

Comparative study of semiconductor power losses between CSI-based STATCOM and VSI-based STATCOM, both used for unbalance compensation

Anas Benslimane[1]* , Jamal Bouchnaif[2], Mohammed Essoufi[1], Bekkay Hajji[1] and Loukmane el Idrissi[2]

Abstract

In this paper, we present a detailed procedure to determine the semiconductor losses for both structures of a shunt STATCOM (Static Compensator), STATCOM based on Current Source Inverter (CSI) and STATCOM based on Voltage Source Inverter (VSI), both used for voltage unbalance compensation. As a first step, we study the VSI-based STATCOM and the CSI-based STATCOM used in high speed railway substations. Then we analyze the design and the sizing of the unbalance compensator in order to obtain an unbalance factor that does not exceed the limits imposed by the standards or by the energy provider. Following that, we compare the performances obtained with both structures VSI-STATCOM and CSI-STATCOM, after calculating the semiconductor power losses in the STATCOM converters. Finally, we validate our approach by simulation over real data of unbalance compensation caused by the new high-speed railway in Morocco. We use the tools MATLAB / Simulink/Simpowersys for performing our simulations.

Keywords: Power losses, VSI, CSI, STATCOM, Unbalance compensation, Railway

1 Introduction

The flexible alternative current transmission system (FACTS) is used in the power grid in order to improve the quality of energy. In particular, the static shunt compensators with voltage source inverters are installed in high-speed railway substations to compensate the unbalance [1–3].

The railway operator is mainly interested in reducing the compensator size, cost, and the converter losses; this is from where comes our idea to propose a replacement of the voltage source inverter structure by the current source inverter structure. To validate this proposition, we show the performances obtained by a CSI-based STATCOM used in the unbalance compensation. The rest of this paper is organized as follows:

In the second section, we give an overview of the principle of electric power supply system for high-speed railways (HSR). The third section presents the analysis of voltage unbalance generated by the railway substation. In the fourth section, we present the STATCOM structure used for unbalance compensation. While in the fifth section, we present our sizing methodology and our control strategy, for both STATCOM structure VSI and CSI. The sixth section, we show the detailed calculation of the semiconductor power losses in the converters. Then in the seventh section, we compare and discuss the obtained results for both structures (VSI-based STATCOM and CSI- based STATCOM) using data coming from railway operator in Morocco about the HSR substation.

2 Principle of electrification of high-speed railway

The HSR are electrified by a tow-phases system 2*25KV – 50 Hz (Fig. 1), where the single-phase transformer of the substation is connected between two phases of the HV power grid.

* Correspondence: anas.benslimane@gmail.com
[1]Laboratory Renewable energy, embedded system and information processing, National School of Applied Sciences, University of Mohammed I, Oujda, Morocco
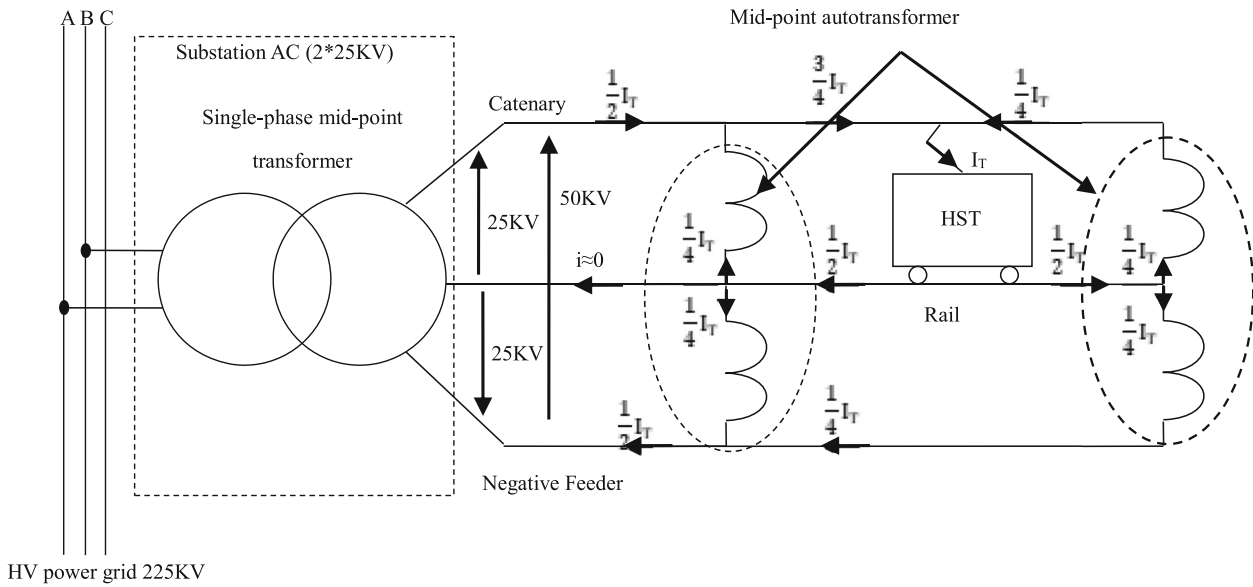Full list of author information is available at the end of the article

Fig. 1 Power circuit of supply AC system (2*25KV-50 Hz) of the HSR substation

This system transmits the energy at 50 kV between the catenary and a complementary cable, called the "negative feeder". A voltage of 25 kV between the catenary and the railis, is obtained by means of Mid-point autotransformer connected between the catenary, the rail, and the negative feeder. The first implementation of this solution was in 1981 on the HST South-East line in France [2].

3 Analysis of the unbalance caused by HSR

A three-phase system is balanced if the three currents or voltages have the same amplitude, the same frequency, as well as the difference between their phases is equal to 120°; otherwise the system is unbalanced. The HSR substations generate a significant unbalance in the high voltage lines with low short-circuit power (S_{cc}), because they are more sensitive to the disruptions. Figure 2 shows the supply schema of a HSR substation by a three-phase line with line impedance (Z_{cc}) [2].

The apparent power and the unbalance factor for HSR substations:

$$T_{iV}(\%) \approx 100 \frac{S_{ss}}{S_{CC}} \tag{1}$$

$$S_{ss} = U \cdot I_{SS} \tag{2}$$

4 Compensation of the unbalance by STATCOM
4.1 Principle of the STATCOM

The static compensator (as shown in Fig. 3) is a three-phase sinusoidal AC current source that injects the negative sequence of currents to compensate the unbalance at the PCC point. This injection of current is made by the STATCOM which is based on power electronics converters [2–4, 5, 6].

The STATCOM must be sized to control the unbalance around $T_{iv.max}$ in the limit imposed by the energy
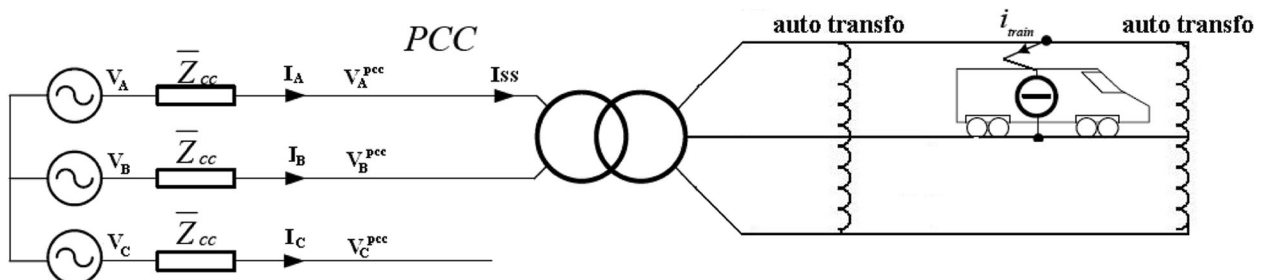

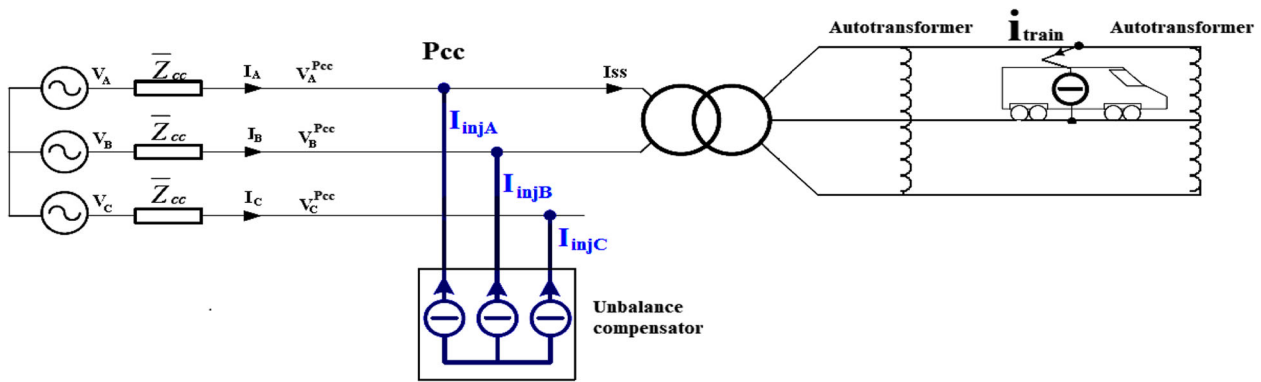**Fig. 2** A power schema of a substation connection [2]

Fig. 3 Diagram of an unbalance compensator

provider. The currents injected at PCC have a negative sequence [7] (see Table 1).

– For total compensation:

$$\overline{I_{inj}^-} = \frac{\sqrt{3}}{3}\overline{I_{SS}}e^{j\frac{\pi}{6}} \tag{3}$$

The apparent power of STATCOM used for unbalance total compensation is: [7].

$$S_{C.Total} = \sqrt{3}U I_{inj}^- = \sqrt{3}U \frac{\sqrt{3}}{3} I_{SS} = U I_{SS} = S_{SS} \tag{4}$$

– For partial compensation:

In order to size the STATCOM, in first step, it is necessary to determine the percentage of the limit RMS value of the current negative component to be injected:

$$I_{inj}^-(\%) = T_{iV.\ max}(\%) \cdot \frac{S_{CC}}{\sqrt{3}U} \cdot \frac{1}{100} \tag{5}$$

The apparent power of STATCOM used for unbalance partial compensation is given by:

$$S_{C.partial} = \frac{I_{inj}^-(\%)}{100} \cdot S_{ss} \tag{6}$$

4.2 Voltage source inverter based STATCOM (VSI-STATCOM)

A compensator STATCOM based on a VSI (see Fig. 4) is composed of several compensation cells coupled in parallel with the secondary of the three-phase transformer with Yy0 connection. Each cell contains an AC filter inductor (L), a VSI converter with sine-triangle PWM control, and a DC side voltage source made by a capacitor (C_{dc}). The VSI-STATCOM and the HSR substation (unbalanced load) are connected to the PCC bus

In general, the apparent power of the compensator (S_c) is equal to the number of cells (N_{VSI}) multiplied by the power of each cell (S_{cel}):

Table 1 Expression & diagram of injected currents

Instant expression of injected currents	Diagram of injected currents
$\begin{bmatrix} I_{inj.A.}^-(t) \\ I_{inj.B.}^-(t) \\ I_{inj.C.}^-(t) \end{bmatrix} = \begin{bmatrix} \sqrt{2} \cdot I_{inj}^- \cdot \sin\left(\omega_r t + \frac{\pi}{3}\right) \\ \sqrt{2} \cdot I_{inj}^- \cdot \sin(\omega_r t + \pi) \\ \sqrt{2} \cdot I_{inj}^- \cdot \sin\left(\omega_r t + \frac{5\pi}{3}\right) \end{bmatrix}$	

Table 2 Expression of Peak, RMS, and AVG value of IGBT and antiparallel diode current and voltage (VSI cell)

	Peak current expression	RMS current expression	AVG current expression	DC Voltage expression
IGBT	$\sqrt{2}\cdot I_{inj}$	$I_{inj}(0, 18r_{max} + 0, 5)$	$I_{inj}(0, 18r_{max} + 0, 22)$	$V_{DC.\ ref}$
Anti-parallel diode	$\sqrt{2}\cdot I_{inj}$	$I_{inj}(0, 5 - 0, 3r_{max})$	$I_{inj}(0, 22 - 0, 18r_{max})$	$V_{DC.\ ref}$

$$S_C = N_{VSI}\cdot S_{cel} \qquad (7)$$

$$S_C = N_{CSI}\cdot S_{cel} \qquad (8)$$

4.3 Current source inverter based STATCOM

A CSI-STATCOM (see Fig. 5) is composed of several compensation cells coupled in parallel to the secondary of the three-phase transformer with Yy0 connection. Each cell contains an AC LC filter, a CSI converter with sine-triangle PWM control, and a DC side current source realized by an inductor (L_{dc}). The CSI-STATCOM and the HSR substation (unbalanced load) are connected to the PCC bus.

In general, the apparent power of compensator (S_c.) is equal to the number of cells (N_{CSI}) multiplied by the power of each cell (S_{cel}):

5 Sizing and control strategy of STATCOM

5.1 Sizing of VSI-STATCOM cell

The power circuit of the VSI-STATCOM cell is composed of a six bidirectional current switch (IGBT with anti-parallel diode), a capacitive storage source in a DC side inverter, and a three-phase inductor filter connected between the AC side inverter (a',b',c') and the transformer secondary (a,b,c). The IGBT switch is controlled by the PWM signal (see Fig. 6).

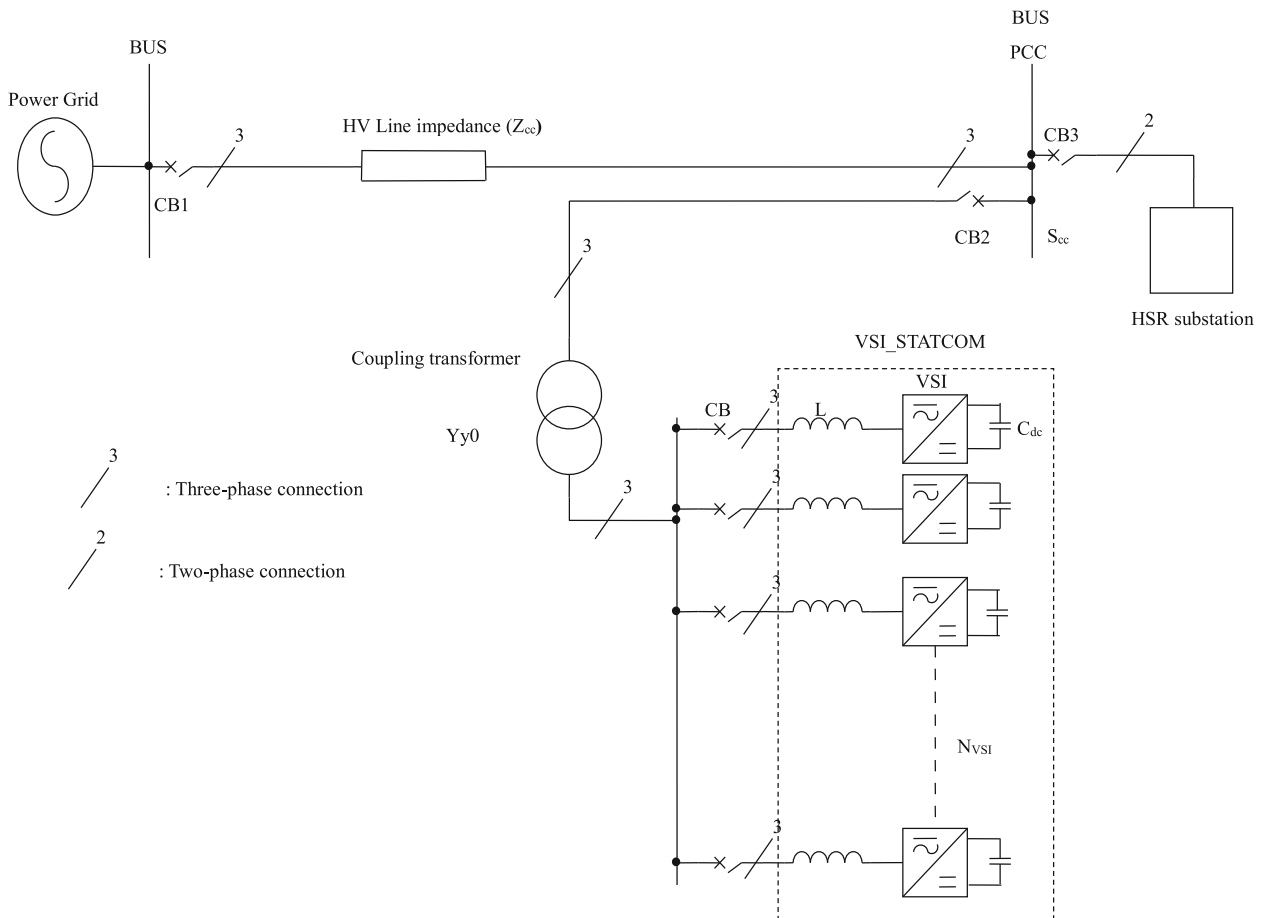The DC capacitor and the filter inductor are given by the flowing expressions [8–10]:
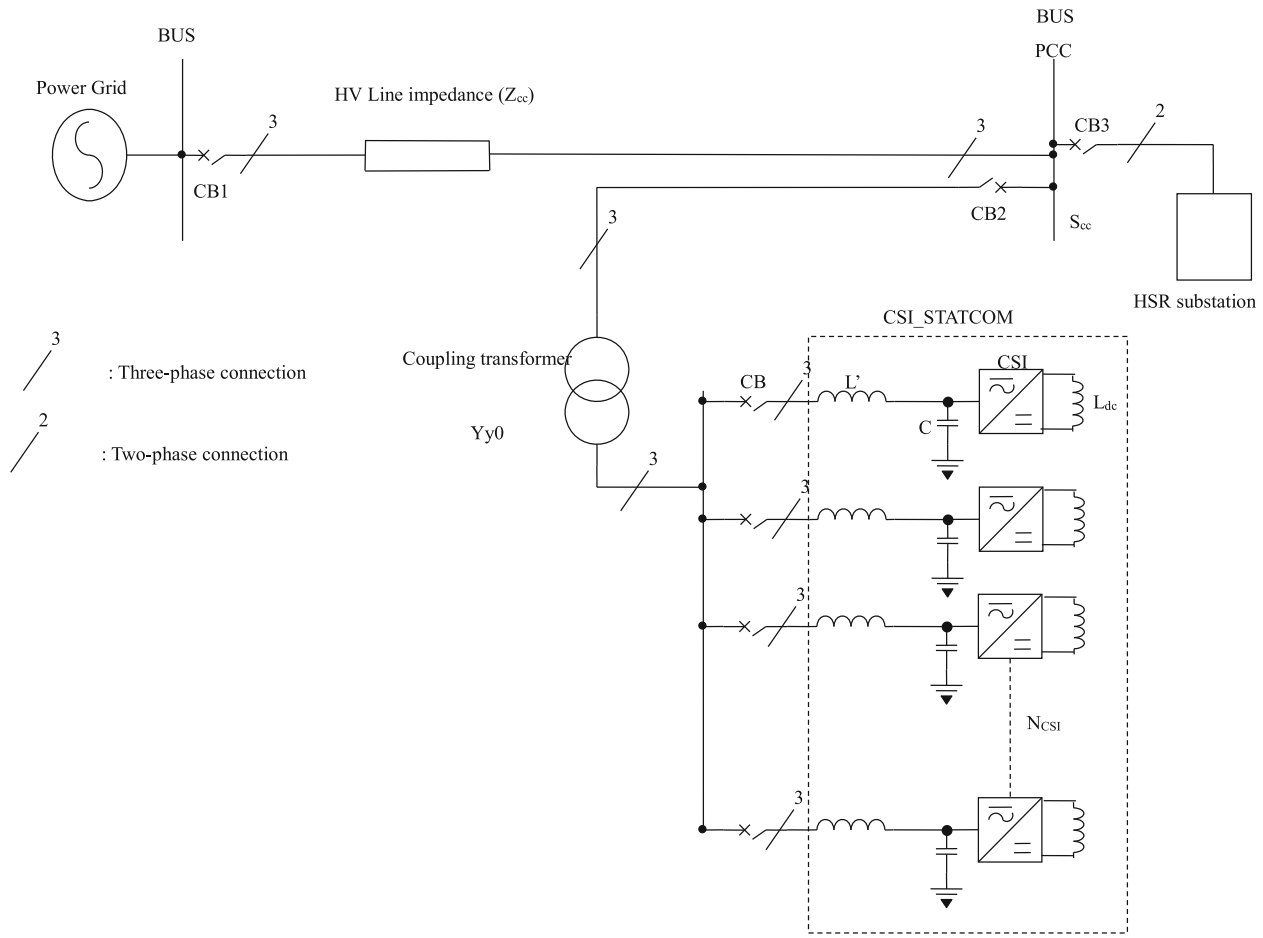

Fig. 4 One-Line Diagram of VSI-STATCOM

Fig. 5 One-Line Diagram of CSI-STATCOM

$$C_{dc} = \frac{\sqrt{2} \cdot S_{cel}}{V_{DC.ref} \cdot \Delta V_{DC}(max) \cdot \omega_r} \qquad (9)$$

$$L = \frac{V_{DC.ref}}{12 \cdot f_d \cdot \Delta I_{inj}} \qquad (10)$$

The voltage and current supported by IGBT are given by the flowing expressions [11]:

Fig. 6 Power circuit of VSI-STATCOM cell

$$I_{sw} \geq \sqrt{2} \cdot I_{inj} \qquad (11)$$

$$V_{sw} \geq V_{DC.ref} \qquad (12)$$

The VSI_STATCOM cell apparent power is given by:

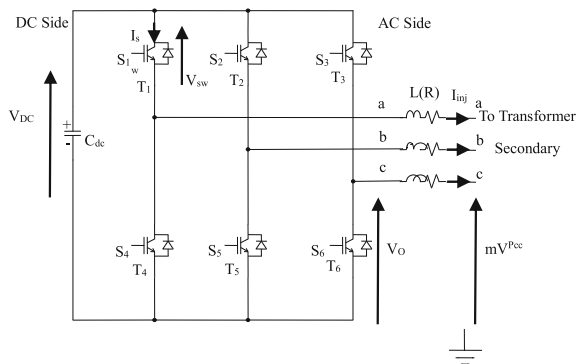$$S_{cel} = 3 \cdot m V^{pcc} \cdot I_{inj} \qquad (13)$$

5.2 Sizing of the CSI-STATCOM cell

The power circuit of the CSI-STATCOM cell is composed of six unidirectional current switches (only IGBT or IGBT with anti-parallel diode and diode in series), an inductor storage source in the DC side inverter, and a three-phase L'C filter connected between the AC side inverter (a',b',c') and the transformer secondary (a,b,c). The IGBT switches are controlled by the PWM signal (see Fig. 7).

The DC inductor and the L'C filter are given by the flowing expressions: [12].

$$L_{dc} = \frac{\sqrt{2} \cdot S_{cel}(1 - (2 \cdot C \cdot \omega_r^2 \cdot L'))}{I_{DC.ref} \cdot \Delta I_{DC}(max) \cdot \omega_r} \qquad (14)$$
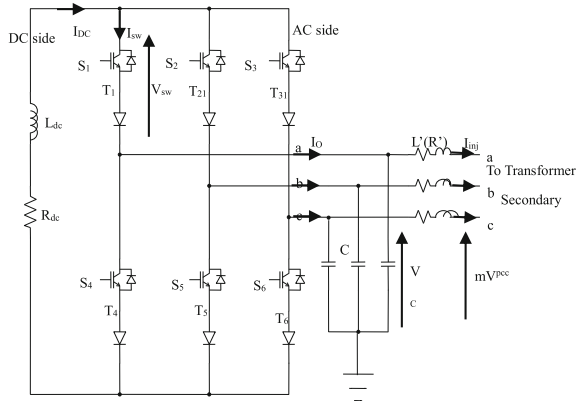
Fig. 7 Power circuit of CSI_STATCOM cell

$$L' = \frac{(mV^{pcc})^2}{3 \cdot S_{cel} \cdot \omega_r} \tag{15}$$

$$C = \frac{1}{L' \cdot \omega_0{}^2} \tag{16}$$

The voltage and current supported by IGBT are given by the flowing expressions: [11].

$$I_{sw} \geq I_{DC.ref} \tag{17}$$

$$V_{sw} \geq \sqrt{2} \cdot V_C(\ max) \tag{18}$$

The CSI-STATCOM cell apparent power is given by:

$$S_{cel} = 3 \cdot mV^{pcc} \cdot I_{inj} \tag{19}$$

The fundamental component of the AC side current (I_O) is given by: [12].

$$I_{DC.re'f = \sqrt{2} \cdot I_O(\ max)} \tag{20}$$

$$\overline{I_O} = \overline{I_{inj}}\left(1 - C.L'.\omega_r{}^2\right) + j.C.\omega_r.m\overline{V^{pcc}} \tag{21}$$

5.3 Control of VSI_STATCOM cell
The shunt STATCOM must inject the negative sequence of the current consumed by the single-phase load (High speed railway substation) in the transformer's secondary. According to equations of Table 1, the block diagram for the set-point generation of the injected currents is shown in Fig. 8 [9, 13].

The VSI-STATCOM cell is controlled by two loops: The first loop controls the injected current (I_{inj}) in the d-q plan (park transformation) with PI controller $R_I(p)$ (see Fig. 9), the second loop regulates the DC bus voltage (V_{dc}) around its reference value with a proportional delay controller $R_u(p)$ (see Fig. 10). The generation of three-phase PWM control signals from the corrected sinusoidal modulating signals (sine) is shown in Fig. 11.
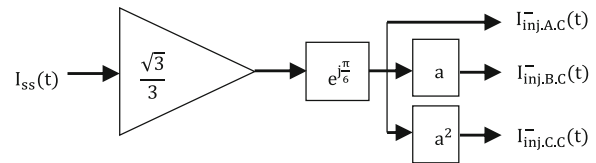

Fig. 8 Obtaining the set-point currents to be injected

The transfer functions of controllers used in the control part are given by [9]:

$$R_u(p) = \frac{K_v}{1 + \tau_v p} \tag{22}$$

$$R_I(p) = K_I \frac{1 + \tau_I p}{\tau_I p} \tag{23}$$

The transformation matrices (Park & Clark) are given by:

$$C = \frac{1}{\sqrt{3}}\begin{bmatrix} 0 & \frac{\sqrt{3}}{\sqrt{2}} & \frac{-\sqrt{3}}{\sqrt{2}} \\ \sqrt{2} & \frac{-1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \end{bmatrix} And\ C'$$

$$= \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \tag{24}$$

$$\begin{cases} P_k^- = \frac{1}{3}\begin{bmatrix} 2\ sin(-\theta) & 2\ sin\left(-\theta - \frac{2\pi}{3}\right) & 2\ sin\left(-\theta + \frac{2\pi}{3}\right) \\ 2\ cos(-\theta) & 2\ cos\left(-\theta - \frac{2\pi}{3}\right) & 2\ cos\left(-\theta + \frac{2\pi}{3}\right) \\ 1 & 1 & 1 \end{bmatrix} \\ \qquad\qquad\qquad \theta = \omega_r \cdot t \end{cases} \tag{25}$$

5.4 Control of CSI-STATCOM cell
The CSI-STATCOM cell is controlled by two loops: The first loop controls the injected current (I_{inj}) in the d-q plan (park transformation) with PID controller $R_{I1}(p)$ (see Fig. 12); the second loop regulates the DC bus current (I_{DC}) around its reference value with a proportional delay controller $R_{I2}(p)$ (Fig. 13). We use the same block diagrams (Figs. 8 and 11) for the injection of set-point currents and the generation of three-phases PWM signals,

The transfer functions of controllers used in the control part are given by [12]:

$$R_{I1}(p) = K_I' \frac{1 + \tau_I' p + \tau_I' \tau_d p^2}{\tau_I' p} \tag{26}$$

$$R_{I2}(p) = \frac{K_{IDC}}{1 + \tau_{IDC} s} \tag{27}$$
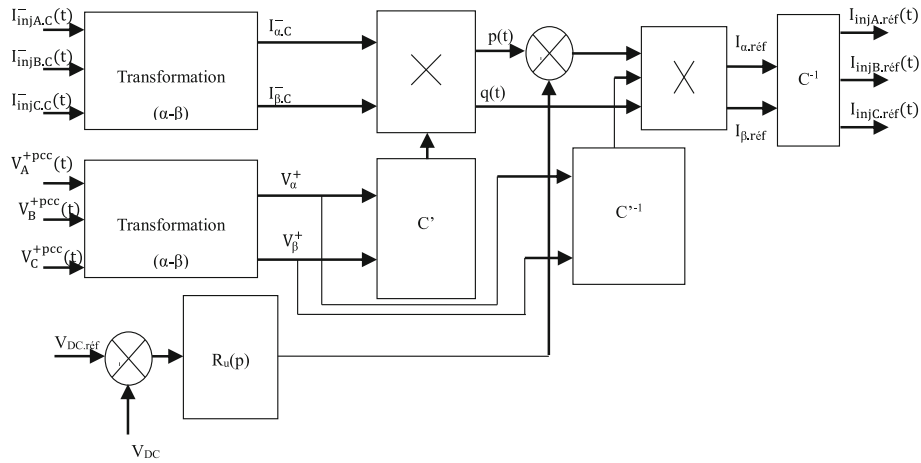
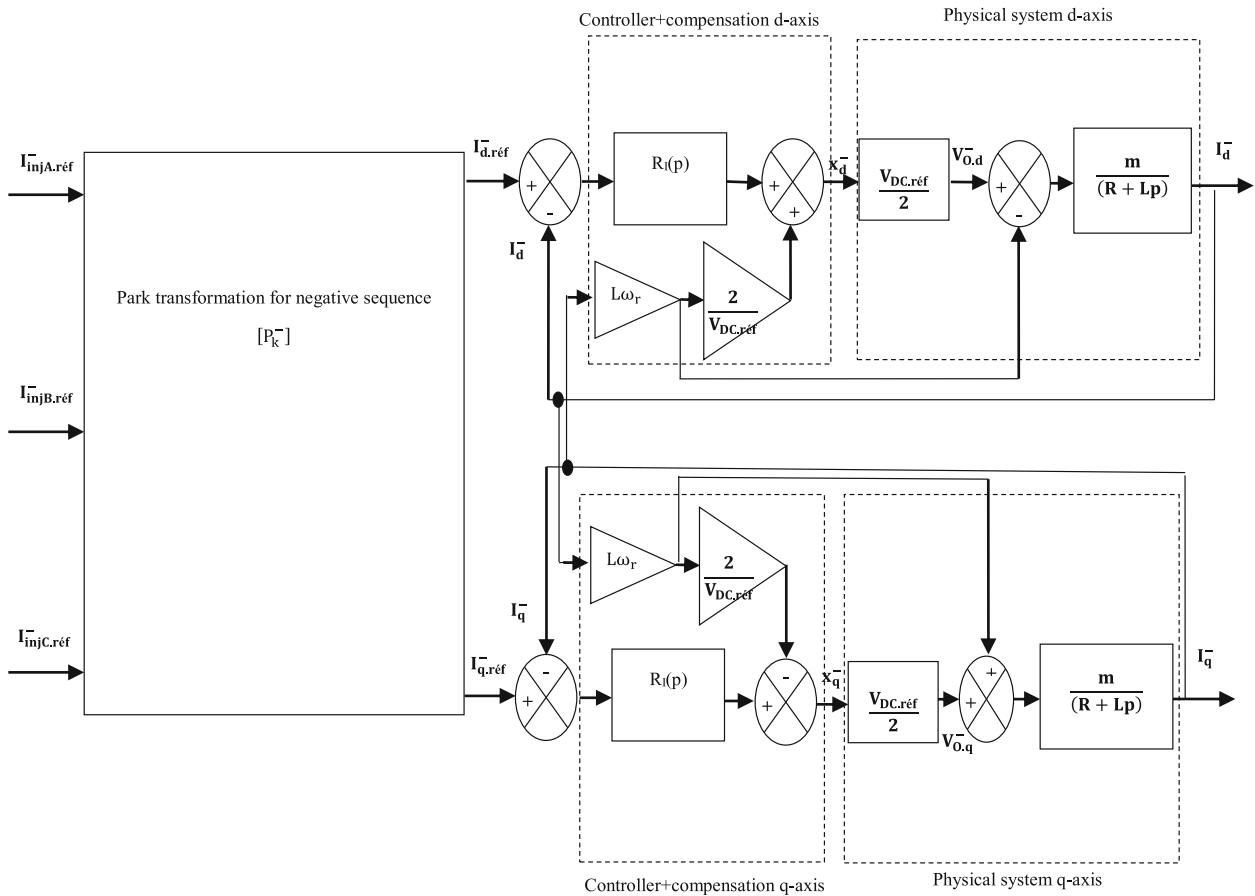**Fig. 9** Diagram control blocks of the voltage V_{DC}

Fig. 10 Diagram control blocks of the injected current negative sequence for VSI cell

The transfer functions of the physical system for CSI-STATCOM in dq plan are given by [12]:

$$H_1(p) = \frac{\dfrac{m}{1-\dfrac{\omega_r{}^2}{\omega_0{}^2}}}{\left(1 + \dfrac{\dfrac{R'}{L'}}{\omega_0{}^2-\omega_r{}^2}p + \dfrac{1}{\omega_0{}^2-\omega_r{}^2}p^2\right)} \qquad (28)$$

$$H_2(p) = \frac{(R'C\omega_r + (L'C \cdot 2\omega_r p))\dfrac{1}{1-\dfrac{\omega_r{}^2}{\omega_0{}^2}}}{\left(1 + \dfrac{\dfrac{R'}{L'}}{\omega_0{}^2-\omega_r{}^2}p + \dfrac{1}{\omega_0{}^2-\omega_r{}^2}p^2\right)} \qquad (29)$$

6 Calculation of power losses in semiconductors

6.1 Analytical expressions of power losses in semiconductors

The IGBT module is a bidirectional current switching device. It is composed of a bipolar transistor with an insulated gate and an anti-parallel diode which allows bidirectional current (VSI cell case) (Fig. 14 (a)). The IGBT combines the advantages of a bipolar transistor (high voltage, high intensity) and a MOSFET (fast switching).

The diode module added in series with the IGBT module ensures the unidirectional current circulation (CSI cell case) (Fig. 14 (b)).

6.1.1 Conduction losses

The equivalent model of an IGBT transistor (Fig. 15 (a)) and the diode (Fig. 15 (b)) during conduction is presented in the following figure:

The analytical expression of the conduction losses can also be expressed in an alternative way in the case when the transistor is in conduction: [2, 14, 15].

$$P_{cond.IGBT} = (V_{CE.sat} \cdot I_{C.AVG}) \\ + \left(r_{on.IGBT} \cdot I_{C.rms}{}^2\right) \qquad (30)$$

In the same way, the conduction diode losses are expressed as follows: [2, 14, 15].

$$P_{cond.D} = (V_F \cdot I_{FAV.AVG}) + \left(r_{on.D} \cdot I_{FAV.rms}{}^2\right) \qquad (31)$$

6.1.2 Switching losses:

The analytical expressions of the switching losses for IGBT are expressed by [2, 14, 15]:

$$P_{comm.IGBT} = f_d \cdot \frac{V_{CE}}{V_{CE.r}} \cdot \left((a_{on} + a_{off})\frac{I_{C.peak}{}^2}{4} + (b_{on} + b_{off})\frac{I_{C.peak}}{\pi} + (c_{on} + c_{off})\frac{1}{2}\right) \qquad (32)$$

In the same way, the switching losses of the diode are expressed by: [2, 14, 15].

– Anti-parallel diode:

$$P_{comm.D} = f_d \cdot \frac{V_{RRM}}{V_{RRM.r}} \cdot \left(a_{rec}\frac{I_{FAV.peak}{}^2}{4} + b_{rec}\frac{I_{FAV.peak}}{\pi} + c_{rec}\frac{1}{2}\right) \qquad (33)$$

– Serial diode (for CSI):

$$P_{comm.D} = f_d \cdot V_r \cdot Q_{rr} \qquad (34)$$

6.2 Power losses calculation for VSI cell

If we take a single-phase AC side of the VSI cell as an example, the both power switches (IGBT module) in the arm (TOP and BOTTOM), switches in a complementary way, and they have the same losses. The Fig. 16 shows the waveform of the current in the IGBT transistor and its anti-parallel diode.

The modulating signal and the injected current for one phase in the VSI cell are expressed as follows:

$$r_{a'}(t) = r_{a', max} \cdot sin(\omega_r t) \qquad (35)$$

With **a'** is a phase reference.
The collector current of IGBT is:

$$I_C(t) = I_{inj}(t) = \sqrt{2} \cdot I_{inj} \cdot sin(\omega_r t + \phi) \qquad (36)$$

The IGBT transistor is conducting in the interval [φ; φ + π], while the antiparallel diode is conducting in the interval [φ + π; φ + 2π]. Therefore, the expressions of the peak, RMS, and AVG values of the IGBT currents and the ant parallel diode current are [11] (see Table 2):

6.3 Power losses calculation for the CSI cell

In the same way as for the VSI cell, expressions of the peak, RMS, and AVG values of the IGBT currents and the series diode current for CSI cell are illustrated in Table 3 [11]:

7 Application and simulation (case study)

The simulation has been performed with the real parameters of the IGBT module of the manufacturer ABB ($V_{CE.r}$ = 4.5KV / $I_{C.r}$ = 1.2KA, ref.: 5SNA1200G450300) and the diode module of the manufacturer SEMIKRON ($V_{RRM.r}$ = 2.2KV /
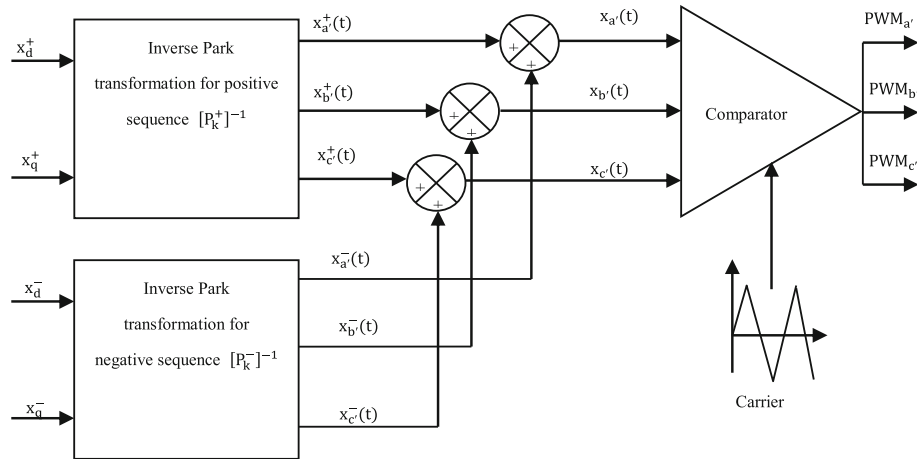
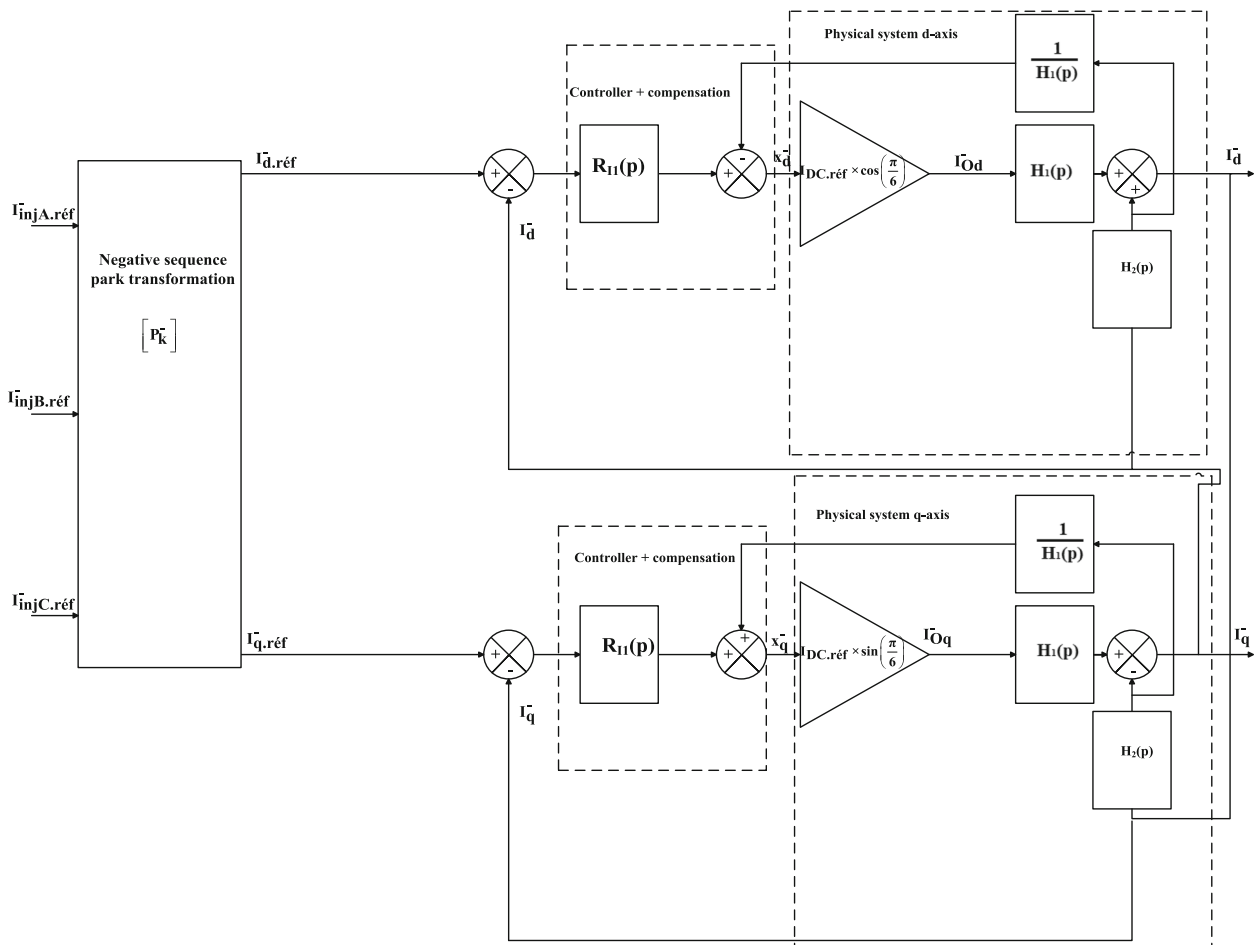**Fig. 11** Generation of three-phase PWM signal

Fig. 12 Diagram control blocks of the injected current negative sequence for CSI cell
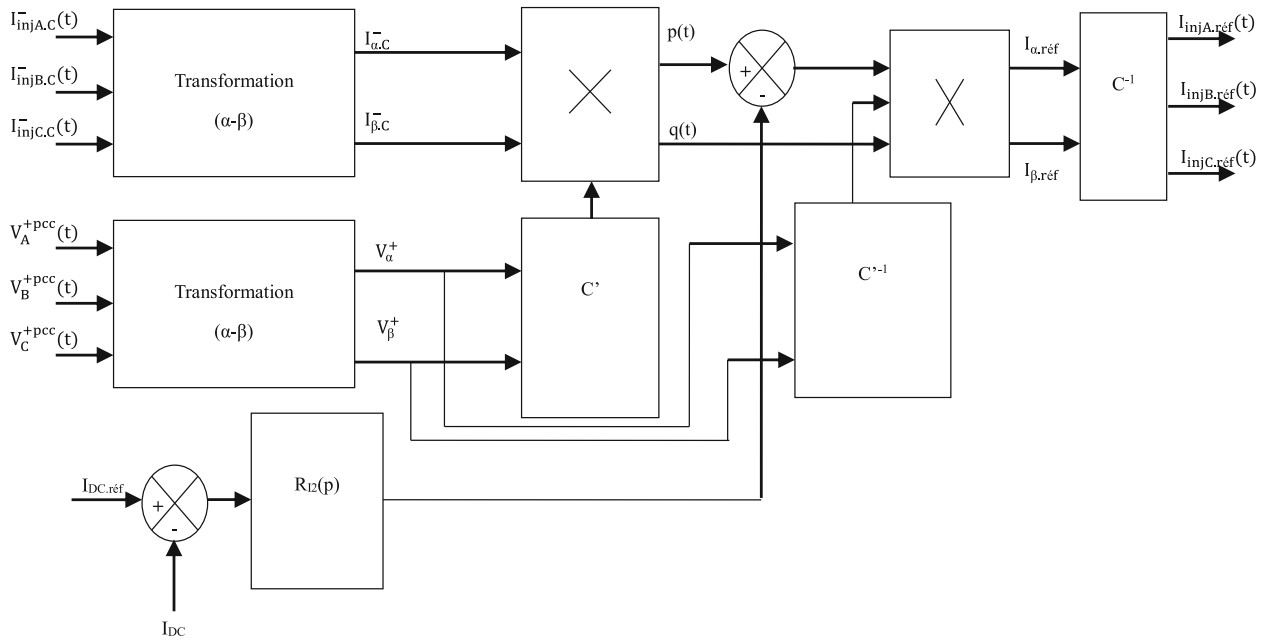
Fig. 13 Diagram control blocks of the voltage I_{DC}

$I_{FAV.r}$ = 1.37KA, ref.: SKKE 1200/22 H4). The Table 4 presents the characteristics of these semiconductors.

We choose one substation among others of the new Moroccan HSR as a study case (see Fig. 17). This substation has the following characteristics (see Table 5) [16]. The unbalance (see Fig. 18) caused by this substation exceeds the limit of 2% imposed by the standard NF EN50160 [17]. Soit is interesting to install an unbalance compensator in this substation.

7.1 Sizing of the unbalance compensators substation (PK100)
In this subsection, we calculate the compensator power with a total unbalance compensation for each type of the converter (VSI and CSI). The calculation results are presented in the Table 6.
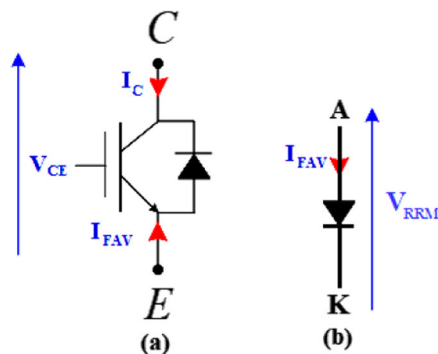
Table 7 shows the values of the parameters calculated for the power circuit of each cell (VSI and CSI):

Table 8 depicts the values of the controller parameters used for control of each cell (VSI and CSI):

7.2 Simulation of unbalance compensation
Figures 19 and 20 show the simulation results of the unbalance factor obtained using static compensators (VSI and CSI):

7.3 Calculating of power losses in full load
The Table 9 presents the conduction and switching power losses for each structure of STATCOM (VSI and CSI):

If considering the active power losses in the AC side filters, and in the DC side storage circuit, the Table 10 presents the global power losses for STATCOM:
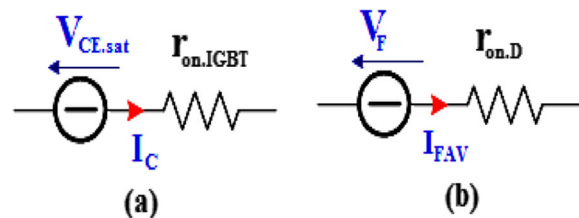

Fig. 14 a The module of an IGBT with anti-parallel diode. **b** The module of the diode in series used in CSI case

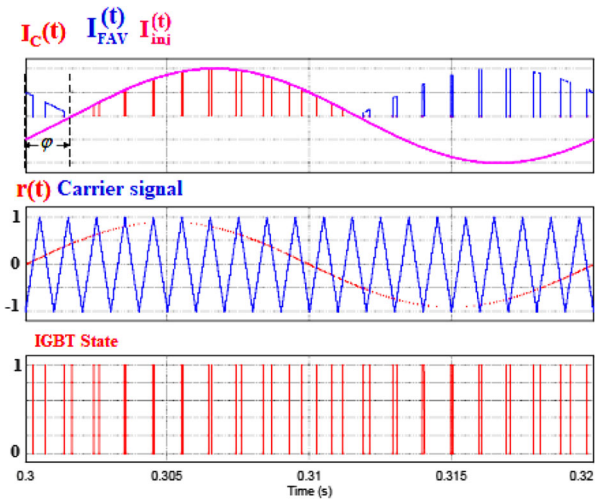**Fig. 15 a** IGBT model in conduction. **b** Diode model in conduction

Fig. 16 IGBT and anti-parallel diode currents waveform with sine-triangle PWM modulation
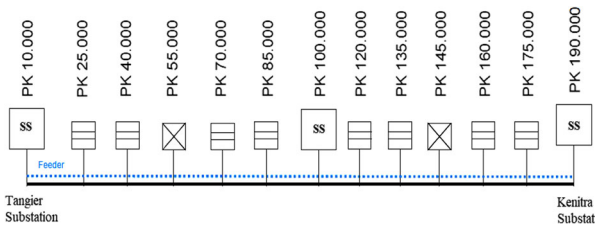
Fig. 17 Distribution schematic of HSR

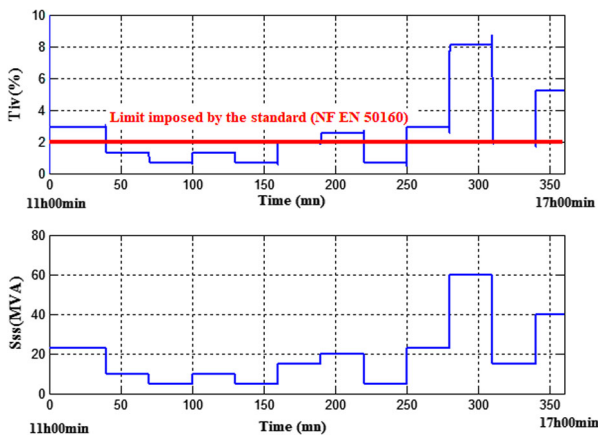**Fig. 18** Unbalance factor and substation power in function of daily railway traffic without STATCOM [16]
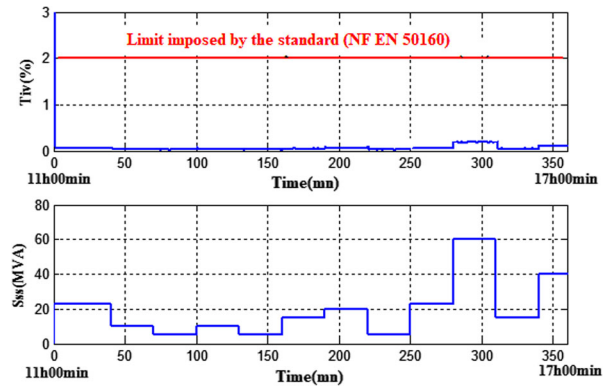

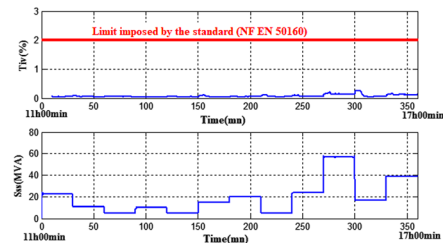**Fig. 19** Unbalance factor in function of daily railway traffic caused by substation Pk100 with VSI_STATCOM

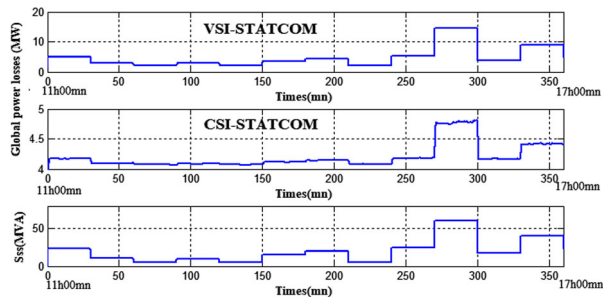**Fig. 20** Unbalance factor in function of daily railway traffic caused by substation Pk100 with CSI-STATCOM

Fig. 21 Global power losses in function of daily railway traffic

Table 3 Expressions of Peak, RMS, and AVG value of IGBT and antiparallel diode current and voltage (CSI cell)

	Peak current expression	RMS current expression	AVG current expression	DC Voltage expression
IGBT	$I_{DC.r}e'f$	$\dfrac{I_{DC.r}e'f}{\sqrt{3}}$	$\dfrac{I_{DC.r}e'f}{3}$	$\dfrac{\sqrt{2}\cdot V_C}{3}$
Series diode	$I_{DC.r}e'f$	$\dfrac{I_{DC.r}e'f}{\sqrt{3}}$	$\dfrac{I_{DC.r}e'f}{3}$	$\dfrac{2\cdot\sqrt{2}\cdot V_C}{3}$

Table 4 STATCOM Semiconductors characteristics

Semiconductor	Parameters	Value
Transistor (IGBT module)	$V_{CE.\,sat}$	3,2 V
	$r_{on.\,IGBT}$	2,94 mΩ
	$V_{CE.\,r}$	4500 V
	$I_{C.r}$	1200 A
	$(a_{on} + a_{off})$	1,2. 10−6
	$(b_{on} + b_{off})$	6,1. 10−3
	$(c_{on} + c_{off})$	1,08
Anti-parallel Diode (IGBT module)	V_F	3,25 V
	$r_{on.\,D}$	2,98 mΩ
	$V_{RRM.\,r}$	4500 V
	$I_{FAV.r}$	1200 A
	a_{rec}	-5,25. 10−7
	b_{rec}	2,61. 10−3
	c_{rec}	375. 10−3
Series Diode (Diode module)	V_F	0,82 V
	$r_{on.\,D}$	0,858 mΩ
	Q_{rr}	700 μC
	V_r	100 V
	$V_{RRM.\,r}$	2200 V
	$I_{FAV.r}$	1370 A

Table 5 Substation characteristics of study case

Characteristics	Value
Transformer rated power	60 MVA
Transformer primary rated voltage	225KV
Transformer secondary rated voltage	2*25KV-50 Hz
Connection	Tow-phases
secondary situation	Mid-point
Kilometric point of substation	Pk100 (100 km)
Distribution schematic of High speed substations	Figure 17
Unbalance factor in function of daily railway traffic between 11h00mn and 17h00mn	Figure 18
Power grid High voltage line (225KV)	Short-circuit power: S_{cc} = 800MVA, Line parameters: $R_{line}(\Omega/Km)$ = 0.129 and L_{line} (mH/Km) = 1.366

7.4 Simulation of power losses in dynamic power variation

Figure 21 shows the dynamic evolution of the global power losses according to the variation of the power consumed by the substation during railway traffic.

7.5 Discussion and evaluation of the results

In sizing terms, the calculation results in Table 10 show that the unbalance compensator with a voltage source inverter (VSI) needs up to 24 converter cells, but the one with a current source inverter (CSI) needs only up to 9 converter cells. This is the advantage of STATCOM with CSI cells; which is the congestion in the railway substation, and the reduced costs.

Figures 19 and 20 show that the STATCOM with VSI cell or CSI cell allow to control the unbalance factor according to the standards ($T_{iv} < 2\%$).

In terms of power losses and efficiency, the calculation results in (Table 10) show that, the compensator based on CSI (4.75 MW, 92.56%) is more optimal than the one based on VSI (14.52 MW, 80.51%), in steady state with full load condition. In addition, Fig. 21 demonstrates that the STATCOM with CSI cells has less loss than the one with VSI in dynamic daily railway traffic. Thus, we conclude that the unbalance compensation with CSI cells is an optimal solution for railway operator.

8 Conclusion

According to the sizing procedure described in this paper, the use of STATCOM compensator is much more required when daily railway traffic reaches a certain value, especially in rush hours. This compensator implies a big investment for the railway operator. For this reason, the designer engineering office tries to choose the optimal solution in terms of cost and efficiency. The obtained results show that the VSI-STATCOM has lower efficiency then the CSI-STATCOM (80,51% VS 92,65%) with full load (rated conditions). The CSI-STATCOM presents a reduced number of converter cells compared to the VSI-STATCOM which reduces the size and the cost of the compensator while keeping the unbalance factor lower than the limit of **2%** imposed by the standard. We conclude so that the STATCOM based on CSI is an optimal solution in high power compensation.

The experimental validation for this comparative study makes the objective of a second paper.

Table 6 Sizing results for unbalance compensator

	Compensation power S_c	Cell power S_{cel}	Number of cell
VSI_STATCOM	60MVA	2544MVA	24
CSI_STATCOM	60MVA	7,24MVA	9

Table 7 STATCOM power circuit parameters

	AC filter	DC circuit	Transformer ratio
VSI cell	$L = 2$ mH($R = 0,12\ \Omega$)	$C_{dc} = 11,31$mF $V_{dc} = 4,5$KV	$m = 8153 \cdot 10{-3}$
CSI cell	$L' = 1$ mH($R' = 6$mΩ), $C = 827\ \mu$F	$L_{dc} = 0.378$H ($R_{dc} = 0,27\ \Omega$) $I_{dc} = 1,2$KA	$m = 20,092 \cdot 10{-3}$

Table 8 Controller parameters

	Injected current controller	DC circuit controller	Switching frequency
VSI cell	$\tau_I = 0,1$ s, $K_I = 7359 \cdot 103$	$\tau_v = 14,14$ ms, $K_v = 1,8 \cdot 103$	10 Khz
CSI cell	$\tau_{I'} = 5,4\ \mu$s, $\tau d = 0,16$ s $K_{I'} = 7,4$	$\tau_{IDC} = 14,14$ ms, $K_{IDC} = 16,03 \cdot 103$	10 Khz

Table 9 Power losses converter STATCOM

STATCOM Converter	Conduction Power losses (MW)	switching Power losses (MW)	Total Power losses in converter (MW)	Efficiency (%)
24 VSI cell	0,417	8414	8832	87,168
9 CSI cell	0,179	0,95	1129	98,15

Table 10 Global power losses for STATCOM

	Active power losses in the filter, AC and DC side (MW)	Power losses converter (MW)	Global Power losses (MW)	Global Efficiency (%)
VSI_STATCOM	5691	8832	14,523	80,512
CSI_STATCOM	3629	1129	4758	92,652

9 Nomenclatures

a, b, c phase indexes

+, −positive and negative sequence indexes

S_cCompensator apparent power

S_{cc}Short-circuit apparent power

S_{ss}Apparent power consumed by substation

$Sc._{total}$Apparent power for total compensation

$Sc._{partial}$Apparent power for partial compensation

S_{cell}converter cell apparent power

P_{cond}Conduction losses

P_{comm}Switching losses

V HVline-ground rated voltages

V^{pcc}HV line-ground voltages in PCC

UHV line-line RMS voltage

$V_{DC.ref}$DC voltage set-point for VSI

ΔV_{DC}voltage ripple in DC side for VSI

V_{CE}IGBT collector-emitter voltage

V_FDiode forward voltage

VLine-ground in filter capacity for CSI

I_{sw} and V_{sw}current and voltage of the semiconductor switch

I_TCurrent consumed by train

iReturn current to substation

I_{ss}Current consumed by substation

IHV line phase current

I_{inj}injected current by compensator

I_CIGBT collector current

I_{FAV}diode current

ΔI_{inj}injected current ripple in AC side inverter for VSI

T_{iv}voltage unbalance factor

mtransformer ratio

N_{VSI}number of voltage source inverter cell

N_{CSI}number of current source inverter cell

$f_d$switching frequency

ω_0Natural frequency of RLC filter for CSI

$\omega_r$power grid pulsation

Z_{cc}Line impedance in PCC

r_{on}dynamic resistance diode

Authors' contributions
AB, and JB performed the detailed design of the compensator cell sizing (VSI and CSI), as well as the calculation of the semiconductors power losses. ME, BH, and LE corresponding, engaged in modifying the paper and submitted it to the PCMP. SM, MT and YM checked the grammar and writing of the paper. All authors read and approved the final manuscript.

Availability of data and materials
Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

Author details
[1]Laboratory Renewable energy, embedded system and information processing, National School of Applied Sciences, University of Mohammed I, Oujda, Morocco. [2]Laboratory of Electrical Engineering and Maintenance, Higher School of Technology, University of Mohammed I, Oujda, Morocco.

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