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LETTER

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Low-temperature smoothing method of scalloped DRIE trench by post-dry etching process based on SF_6 plasma

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Abstract

Deep reactive-ion etching (DRIE) is commonly used for high aspect ratio silicon micromachining. However, scalloping, which is the result of the alternating Bosch process of DRIE, can cause many problems in the subsequent process and degrade device performance. In this work, we propose a simple and effective method to smoothen the scalloping of DRIE trenches. The proposed method utilizes sidewall dry etching by reactive-ion etching (RIE) based sulfur hexafluoride (SF_6) plasmas, following the DRIE process. To investigate the effect of the etch parameter on the scallop smoothing effect, the radio frequency (RF) power and gas flow are controlled. After the RIE treatment, the scallop smoothing effects were evaluated by measuring the average scallop depth under each condition. The scallop depth was reduced by 91% after implementing the scallop smoothing technique using RIE. Thus, our smoothening method based on SF_6 plasmas would provide broad availabilities and applicability in silicon micromachining with the simple low-temperature process.

Keywords: Deep reactive-ion etching, Reactive-ion etching, SF_6 plasma, Scallop smoothing, Silicon micromachining

Introduction

Deep reactive-ion etching (DRIE) is the most popular dry etching process used to create deep trenches and holes for various applications such as micromachining of micro-electromechanical systems (MEMS) and through-silicon via (TSV) for three-dimensional (3D) packaging [1]. The DRIE process is known as the Bosch process steps that are pulsed and time-multiplexed etching. In the Bosch process, the etching and passivation steps are alternating to achieve vertical trenches [2]. However, the repeated etch/deposit steps in DRIE essentially create scalloped sidewalls in trenches, and this degrades the performance of MEMS devices. For example, the scalloped sidewall of silicon can cause degrade the performance of silicon diodes by introducing interface charge and undesired capacitance [3]. In addition, the scalloping of silicon sidewalls causes light scattering and reduces the signal-to-noise ratio (SNR) in optical applications such as micromirrors, silicon waveguide, and optical switches [4–6].

To address these problems, many studies have developed strategies to fabricate scallop-free silicon structures in micromachining. The initial studies focused on the direct modification of the DRIE processes. Voss et al. modified the DRIE processes by introducing C_4F_8 and O_2 gases during the etching process [3]. The incorporation of C_4F_8 in each etching step resulted in smooth profiles; however, the etch rate of silicon was low. Chen et al. increased the ion flux density using a higher coil power during the etching to reduce the passivation removal time [7]. The decrease in the switching time between the etch and passivation steps reduced the scalloping. Another strategy to fabricate scallop-free trenches is incorporating

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other etch systems. Fu et al. employed reactive-ion etching (RIE) as the DRIE assistant based on aspect ratio dependent scalloping attenuation (ARDSA) effect in the Bosch process [8]. RIE and the subsequent deposition of a thick passivation layer preceded the DRIE process to avoid the scalloped sidewall at the top of the trenches while using DRIE at increasing trench depth. Compared with the conventional DRIE process, the RIE-combined DRIE process could reduce the scalloped sidewall roughness by approximately 60%. However, chipmakers cannot directly modify DRIE systems in many cases because the DRIE process is often optimized for other production purposes. Besides, incorporating other etching systems to DRIE can complicate the overall etching process for vertical trench fabrications complicated.

Alternatively, other researchers have explored strategies to smoothen the scalloped DRIE sidewalls via postprocessing, without modifying the DRIE process. Focused ion beam (FIB) milling techniques for optical MEMS devices were investigated by Song et al. [9]. The FIB milling technique effectively reduced the RMS value of the sidewall roughness below 10 nm. However, FIB milling is not suitable for mass production because trenches are treated one at a time, making it time-consuming. Zishan et al. developed a DRIE roughness reduction method based on alternating oxidation and oxide removal steps [10]. This method is based on the fact that the oxidation rate of the sharp silicon tip of scalloped sidewalls is higher than that of other regions. Repeated oxidation and oxide removal cycles can reduce the scallop depth of trenches from 410 nm to 80 nm. However, high-temperature oxidation at 965 °C can cause heat-related problems such as severing the metal connection of integrated circuits (ICs) in direct fabrication of MEMS devices on the substrate with ICs.

In this study, we proposed a simple and effective scallop smoothing method using dry etching, RIE. The RIE with single SF_6 gas flow smoothens the scalloped DRIE trenches. This smoothening effect can be controlled by selecting the physical and chemical etching conditions of the SF_6 plasmas. The proposed method employs low-temperature (< 200 °C) dry etching. Also, the use of the single SF_6 gas, rather than a mixture gas, can reduce the complexity of etching, thereby reducing the cost of the process during mass production.

Materials and methods

Silicon cylindrical trenches with a diameter of 70 μm and a height of 230 μm were the target structures to investigate the proposed scallop smoothing method. Figure 1

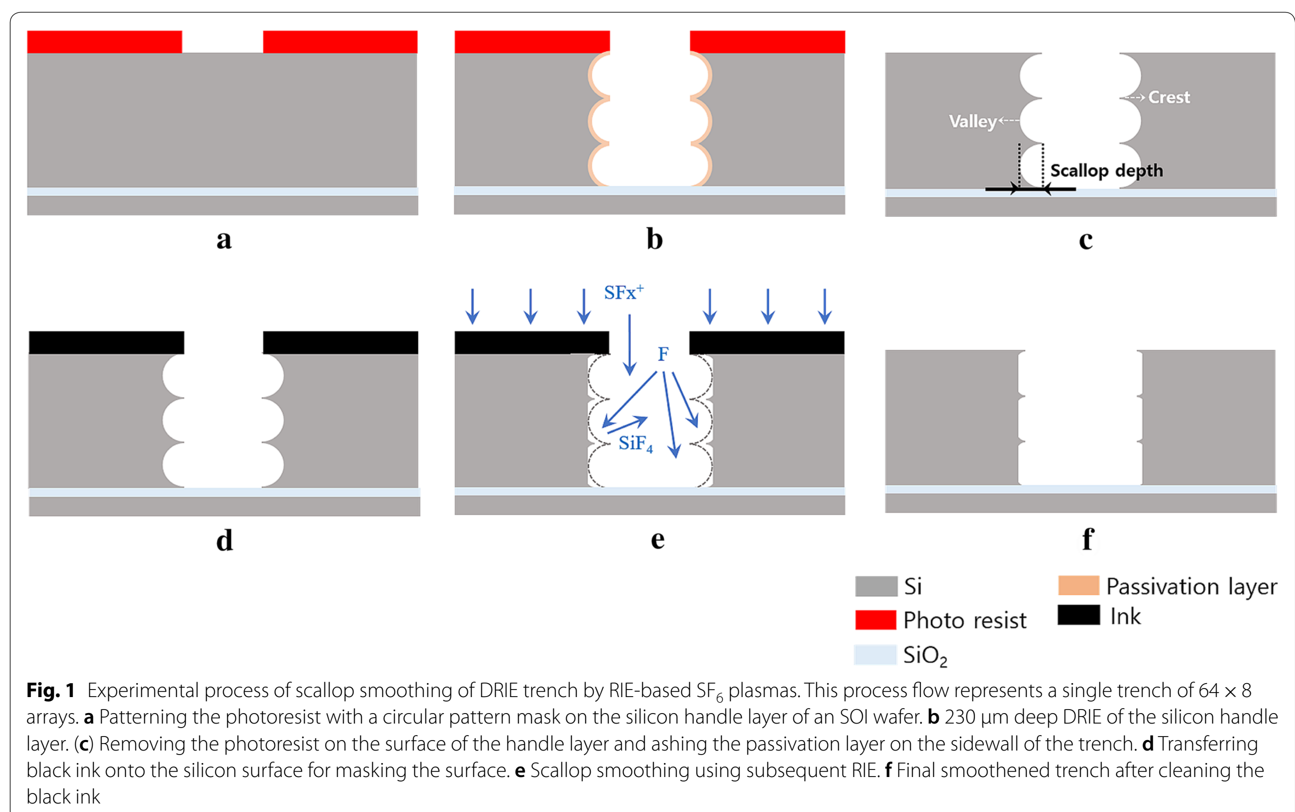

Fig. 1 Experimental process of scallop smoothing of DRIE trench by RIE-based SF_6 plasmas. This process flow represents a single trench of 64 × 8 arrays. **a** Patterning the photoresist with a circular pattern mask on the silicon handle layer of an SOI wafer. **b** 230 μm deep DRIE of the silicon handle layer. (**c**) Removing the photoresist on the surface of the handle layer and ashing the passivation layer on the sidewall of the trench. **d** Transferring black ink onto the silicon surface for masking the surface. **e** Scallop smoothing using subsequent RIE. **f** Final smoothened trench after cleaning the black ink

shows a schematic diagram of the overall experimental processes. First, the circular 64 × 8 arrays were patterned on the silicon handle layer of a silicon on insulator (SOI) wafer (Buysemi, Seoul, Republic of Korea) via standard photolithography (Fig. 1a). The thicknesses of the silicon device layer and the silicon handle layer of the SOI wafer were 5 µm and 230 µm, respectively. The buried oxide (BOX) layer, which acts as the DRIE etch stopper, had a thickness of 1 µm thick. Negative photoresist, DNR-L-300-40 (Dongjin Semichem Co., Ltd., Seoul, Republic of Korea), was spin-coated on the SOI handle layer with a thickness of 5.4 µm, providing sufficient hard mask during the DRIE of 230 µm. After patterning the circular arrays with the negative photoresist using an MA6 mask aligner (Suss Microtec SE, Garching, Germany), we used an Omega® LPX-DSi Etch system (SPTS Technologies Ltd., Newport, United Kingdom) to etch the handle silicon by the cyclic Bosch process (Fig. 1b). The etched trenches had an aspect ratio of approximately 3:1. Before the subsequent RIE for scallop smoothing, the patterned photoresist and sidewall passivation layer formed during the deposition steps of DRIE were removed using O_2 plasma asher, Mini-Plasma Station (Plasmart Corp., Daejeon, Republic of Korea) (Fig. 1c). The ashing process was performed for 10 min at RF power of 350 W under 100 sccm O_2 gas flow.

After ashing, the average scallop depths of the DRIE trenches were measured before scallop smoothing using RIE. Because the sample has a circular 64 × 8 array pattern, we diagonally cleaved the sample along the array pattern to view the cross-section of the trench using scanning electron microscopy (SEM). Two different locations, where the one is near the top area and the other is at the bottom of the trench, were selected to compare the smoothening effects statistically. Since the cleaving process can chip the weak top opening area, the scallops at approximately 50 µm away from the top opening area were selected. We defined the scallop depth as the distance from the tangential line of the midpoint valley to the line passing in-between two adjacent crests (Fig. 1c). Every 5 ripples of the scallops were selected at each location in one dice sample, which means a total of 10 data points in the sample. We also collected the measured data with different 5–6 samples selected in random locations across the wafer.

One another wafer was selected from the DRIE wafer samples to apply the scallop smoothing RIE technique. This is to maintain a consistent exposed area and reduce the sample variation during the scallop smoothing RIE process. We covered and re-patterned the circular arrays with black ink transferred via a soft lithographic method to protect the surface of the wafer. A custom-made 2 cm × 2 cm square PDMS sheet was soaked into alcohol-based ink (Monami, Yong-in, Republic of Korea). After the PDMS sheet has sufficiently swelled, the ink was transferred to the wafer surface through contact with the PDMS sheet. We perfomed the hard bake procedure of the ink at 90 °C for 1 min 30 s. Finally, the RIE process for scallop smoothing was performed (Fig. 1e) using a plasma etching system (PlasmaPro 800 Plus, Oxford Instruments Plasma Technology, Bristol, United Kingdom). The proposed scallop smoothing method utilizes SF_6 plasmas. The process temperature was approximately 10 °C, which can be beneficially applied to the fabrication process with a low thermal budget. The silicon crests have a higher probability of reacting with the incident SF_x ions and fluorine (F) radicals than the silicon valleys. The etch rate of the crest is higher than that of the valley, resulting in smooth sidewalls. After completing all the etch processes, the patterned black ink was removed by dipping in acetone and isopropyl alcohol (Fig. 1f). To achieve the most effective scallop smoothing of DRIE trenches, the etch parameters, RF power and SF_6 flows, were mainly controlled. These variables regulate physical etching by ions and chemical etching by radicals in the plasma etching system [11]. By precisely tuning these parameters, we obtained the optimal etching condition for the proposed method to achieve scallop-free trenches.

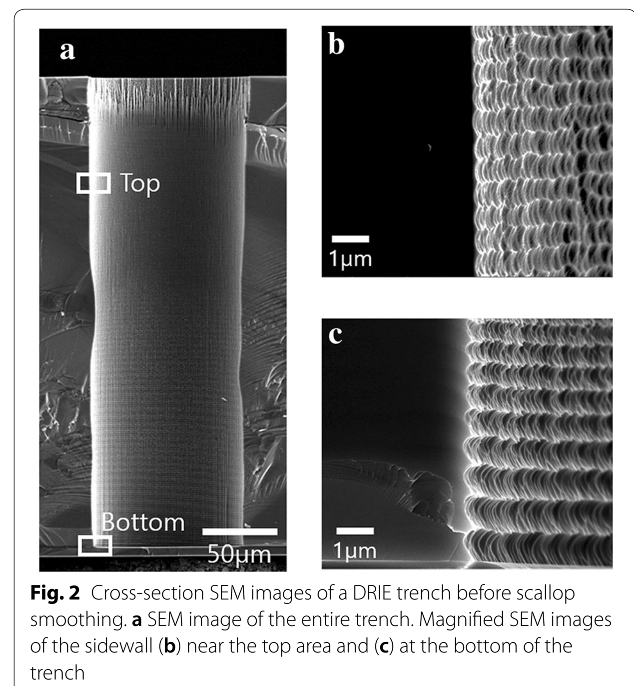

Fig. 2 Cross-section SEM images of a DRIE trench before scallop smoothing. **a** SEM image of the entire trench. Magnified SEM images of the sidewall (**b**) near the top area and (**c**) at the bottom of the trench

Results and discussion

Figure 2 shows the cross-section SEM image of a typical DRIE trench. From Fig. 2b, c, it can be seen that the sidewall of the DRIE trench shows scalloping. The initial average scallop depths before scallop smoothing were 130 nm at the top and 230 nm at the bottom of the trench. The influence of the RF power on sidewall etching for scallop smoothing was investigated. We increased the RF power from 100 W to 250 W at intervals of 50 W and fixed other etch parameters such as pressure (2 mTorr), SF_6 flow (10 sccm), and process time (10 min). Figure 3a shows the measured average scallop depths under each RF power condition. The scallop depth at the top of the trench decreased with an increase in the RF power. As noted by Tzeng, increasing the RF power considerably increases the concentrations of both F radicals and ions [12]. The increased physical and chemical reaction by the radicals and ions etched the silicon crests more quickly than the valleys of the sidewalls; therefore, smoother sidewalls can be achieved (Fig. 3b). However, at the bottom of the trench, the average scallop depth increased slightly at 150 W. It can be observed from Fig. 3c that an angled sidewall profile was formed when the RF power increased above 150 W. The slope of the scalloped sidewall formed an angle of ~ 64° with the surface plane (Fig. 4a), and this morphology is related to the crystal orientation. The angled sidewall profiles were formed by secondary etching of the reflected ions during

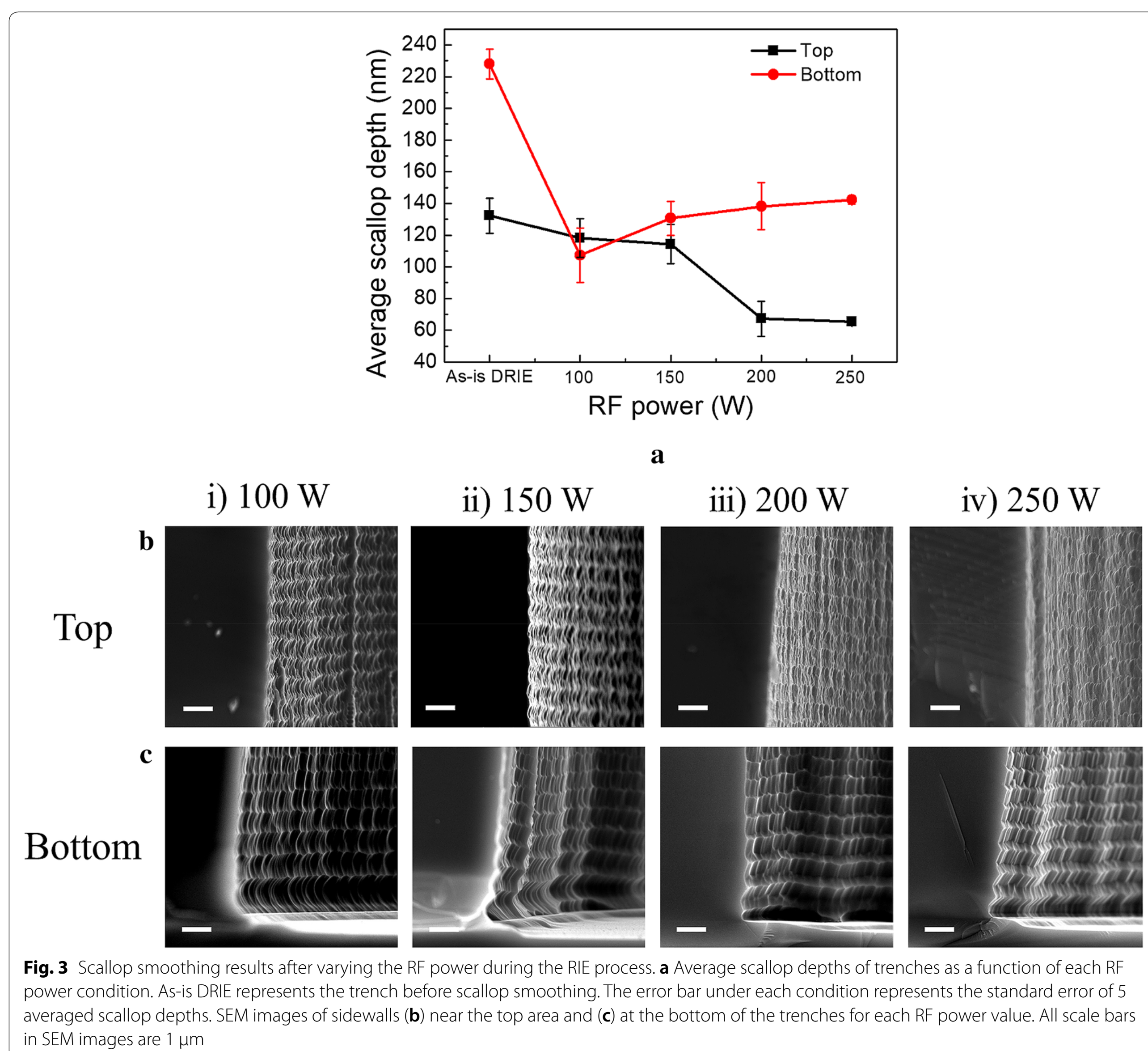

Fig. 3 Scallop smoothing results after varying the RF power during the RIE process. **a** Average scallop depths of trenches as a function of each RF power condition. As-is DRIE represents the trench before scallop smoothing. The error bar under each condition represents the standard error of 5 averaged scallop depths. SEM images of sidewalls (**b**) near the top area and (**c**) at the bottom of the trenches for each RF power value. All scale bars in SEM images are 1 μm

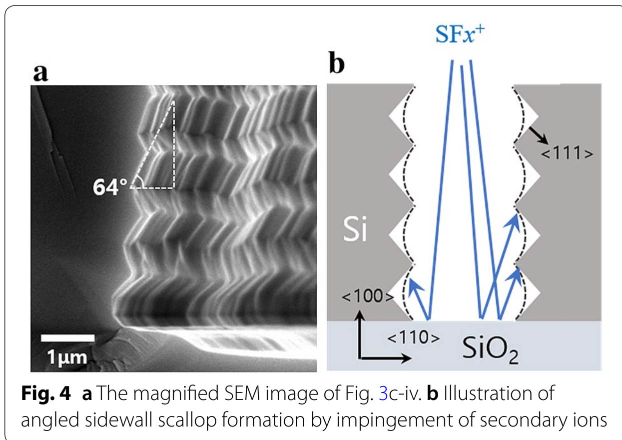

Fig. 4 **a** The magnified SEM image of Fig. 3c-iv. **b** Illustration of angled sidewall scallop formation by impingement of secondary ions

silicon plasma etching. The difference in the etch rates in a different direction in silicon results in the appearance of <111> crystal planes; the sidewall profiles form angles of 50–70° with the surface plane [13]. As the RF power increased, the increase in the self-bias voltage accelerated more SF_x ions to the bottom surface of the trenches, forming more angled sidewall profiles [11]. These excited SF_x ions bounced back to further distances from the surface of the BOX layer. The impingement of the reflected ions etched the sidewall anisotropically, resulting in angled and sharp scalloped sidewalls (Fig. 4b). Varying the RF power did not produce the desired scallop smoothing effect on the bottom side to reduce the average scallop depth of the entire trenches, owing to the formation of angled sidewalls.

In order to investigate the influence of SF_6 gas flow on sidewall smoothing, the SF_6 flow rate was increased from 10 sccm to 50 sccm. Other conditions, excluding RF power, were identical to those in the RF power variation. The RF power was fixed at 100 W, where the scallop

Fig. 5 Influence of the SF_6 gas flows in the scallop smooting RIE process. **a** Average scallop depths of trenches as a function of each SF_6 flow condition. As-is DRIE represents the trench before scallop smoothing. The error bar under each condition represents the standard error of 5 averaged scallop depths. SEM images of sidewalls (**b**) near the top area and (**c**) at the bottom of the trenches under each SF_6 flow condition. All scale bars in SEM images are 1 µm

depth was reduced most effectively without the formation of an angled sidewall profile at the bottom of the trench. As shown in Fig. 5a, the average scallop depth at the top of the trench decreased with an increase in the gas flow rate. A higher SF_6 flow increased the F radical concentration. This accelerated the chemical etching of the silicon crest, resulting in more smoothened profiles of sidewalls (Fig. 5b). At SF_6 gas flow of 30 sccm, the scallop depth near the top area decreased by 70 nm from 130 nm to 60 nm. On the other hand, the scallop depth at the bottom decreased by 160 nm from 230 nm to 70 nm. This is because the higher vertex or larger exposed area of the scallop crest has a higher possible contact with the F radical in order to etch away faster, which increases the etch rate. However, at the bottom, the average scallop depths increased when the SF_6 flow was greater than 30 sccm. Irregular dented patterns were observed at the sidewalls at 40 sccm and 50 sccm (Fig. 5c-iv and c-v). The factors responsible for these phenomena are not fully understood, but we assumed that a byproduct of etching is deposited irregularly during sidewall scallop smoothing. The chemical reaction between the F atoms and the SiO_2 bottom surface can produce SiO_xF_y, and this byproduct was deposited on the sidewall of trenches, inhibiting uniform sidewall scallop smoothing. According to previous studies, the inhibition by re-deposition of this byproduct increases the surface roughness or formation of silicon micro grass [14, 15]. Further research is necessary to correctly identify the factors responsible for these phenomena, which we believed to be due to the reaction mechanism between SiO_2 and F radicals.

To avoid etching of the sidewall with dented patterns, the SF_6 flow rate was fixed at 30 sccm, where the most significant scallop smoothing effects were observed without dented patterns. The RF power and pressure conditions were set to 100 W and 2 mTorr, respectively. Increasing the etching time to 30 min resulted in smoother sidewalls of DRIE trenches. Figure 6 shows the cross-sectional SEM images of the trench smoothened at SF_6 30 sccm for 30 min. No scallops were visible on the sidewall near the top of the trench. The average value of the scallop depth decreased below 20 nm (91% reduction from 230 nm), without any dented patterns or angled sidewall scalloping at the bottom of the trench (Fig. 6b). Since the long etching time of the scallop smoothing RIE process can widen the circular trench, it is necessary to investigate the opening diameters of the trench before and after performing the smoothening technique. As shown in Fig. 7a, b, the diameter of the top area slightly increased from 70.17 μm to 72.68 μm (a 1.25 μm increase in the radius) after 30 min of scallop smoothing RIE. Since an excessive number of cycles in the DRIE process etched the BOX layer of the SOI wafer, size expansion at the bottom can be measured by inspecting the annular residual pattern, as shown in Fig. 7d. A subsequent RIE etching process, in which the selectivity between silicon and silicon oxide is very high, removed only the sidewall of the silicon, resulting in the horizontal expansion of the annular borderline of the silicon. This residue of the buried oxide layer was shown as an annular pattern at the edge of the trench. The width of the annular pattern was 1.49 μm, indicating an increment in the radius at the bottom of the trench.

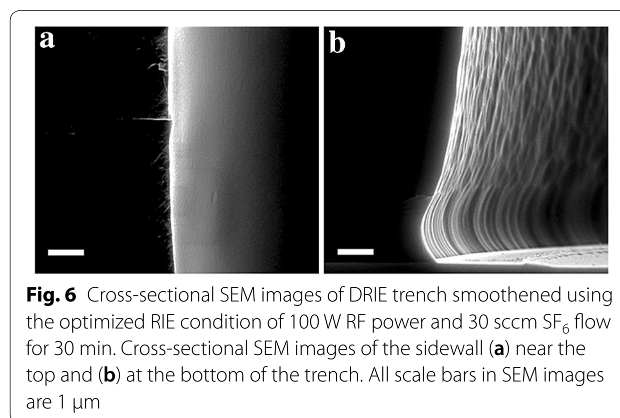

Fig. 6 Cross-sectional SEM images of DRIE trench smoothened using the optimized RIE condition of 100 W RF power and 30 sccm SF_6 flow for 30 min. Cross-sectional SEM images of the sidewall (**a**) near the top and (**b**) at the bottom of the trench. All scale bars in SEM images are 1 μm

Conclusion

In this study, we proposed a simple and effective smoothing method of scalloped DRIE trenches using dry etching. There were no heat-related problems and risk of damaging the IC in the substrate as the method employs low-temperature dry etching. Furthermore, the use of SF_6 single gas reduced the complexity of the etching system and the cost. By moderately controlling SF_6 gas flows, the average scallop depth was reduced by 91% from 230 nm to 20 nm at the bottom of the trenches, resulting in smooth profiles of the sidewall trench. This method is expected to be useful for the manufacture of various MEMS devices that require smooth silicon trenches.

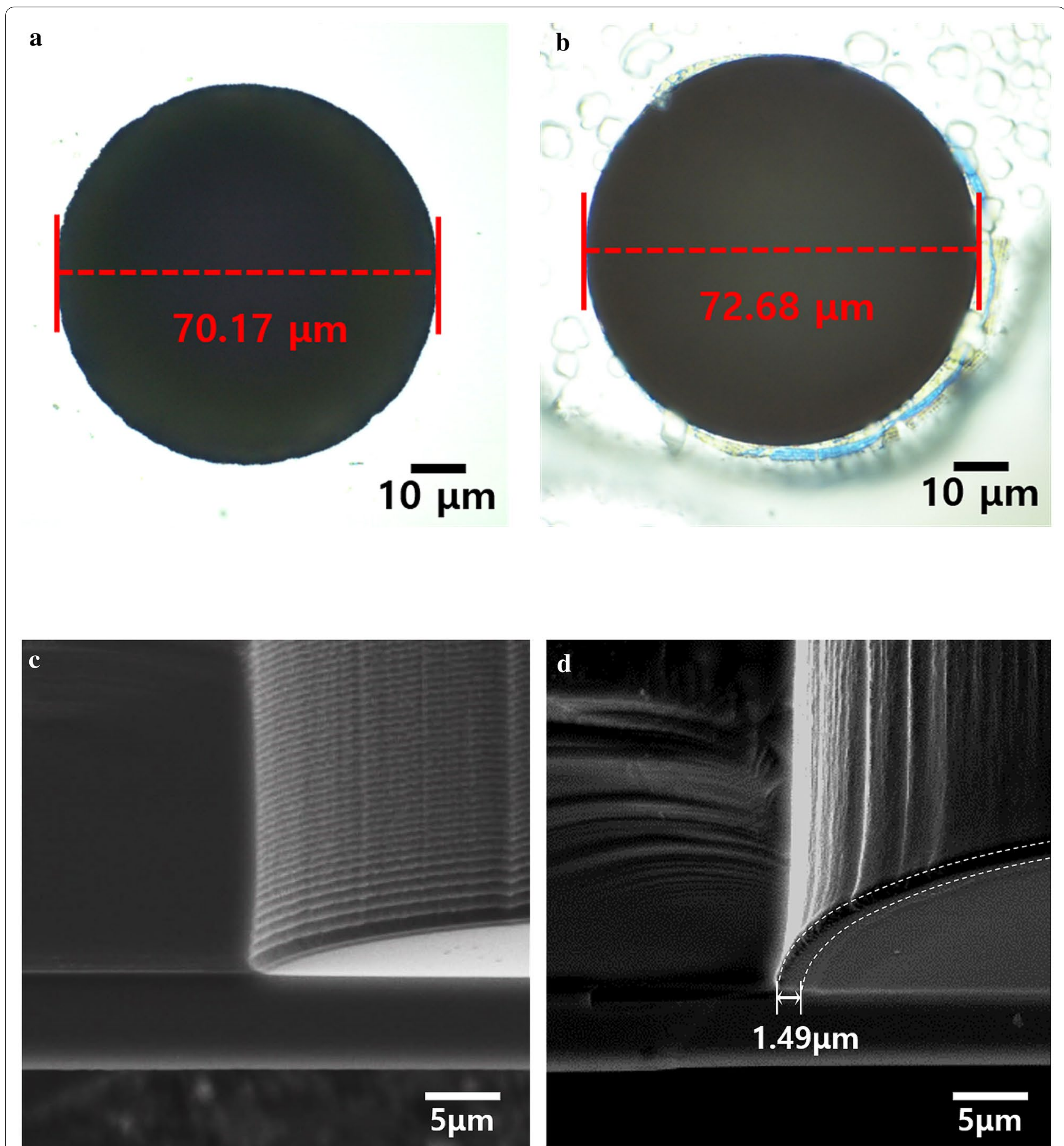

Fig. 7 Optical top view images of the opening trenches (**a**) before and (**b**) after the scallop smoothing RIE. Cross-sectional SEM images at the bottom of the trenches (**c**) before and (**d**) after scallop smoothing RIE for 30 min

Abbreviations

DRIE: Deep reactive-ion etching; RIE: Reactive-ion etching; SF_6: Sulfur hexafluoride; RF: Radio frequency; MEMS: Micro-electromechanical system; TSV: Through silicon via; SNR: Signal to noise ratio; ARDSA: Aspect ratio dependent scalloping attenuation; FIB: Focused ion beam; ICs: Integrated circuits; SEM: Scanning electron microscopy; F: Fluorine.

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Authors' contributions

JSP, S-HB and BCL devised the idea and designed the experimental processes. D-HK and SMK performed the DRIE process for the fabrication of silicon trenches. JSP and D-HK performed RIE for scallop smoothing that is the primary process of this project. TSK, S-HB, and BCL supervised the project. JSP, JHP, TGK, and BCL analyzed the etching results of RIE for scallop smoothing. The first draft of the manuscript was written by JSP. All authors read and approved the final manuscript.

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Availability of data and materials

The datasets supporting the conclusions of this article are included within the article.

Competing interests

The authors declare that they have no competing interests.

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