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CMOS compatible 2T pixel for on-wafer in-situ EUV detection

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Abstract

A novel 2-transistor (2T) pixel EUV detector is proposed and demonstrated by advanced CMOS technology. The proposed 2T detector also exhibits high spectral range (< 267 nm) and spatial resolution (67 μm) with high stability and CMOS Compatibility. The compact 2T EUV detector pixels arranged in a test array are capable of on-wafer recording the 2D EUV flux distribution without any external power. The compact 2T EUV detector pixels arranged in a test array are capable of on-wafer recording the 2D EUV flux distribution without any external power. Through proper initialization process, EUV induced discharging mechanism is fully investigated and an EUV induced electron emission efficiency model is established. Finally, a 2D array for in-situ EUV detection is demonstrated to precisely reflect the pattern projected on the chip/wafer surface.

Introduction

In recent years, Extreme Ultraviolet (EUV, 10–100 nm or 13.5 nm) radiation has become one of the core technologies in modern semiconductor manufacturing industry. According to Moore's law, it has been projected that the total number of transistors on a single chip will double every a few years [1, 2]. By scaling down the critical dimensions (CD) in ICs, the semiconductor industry continuously pushed the circuit performance and its complexity to the next stages [3, 4]. In the past decade, the mainstream lithography system adopts Deep Ultraviolet (DUV) light of wavelength from 300 to 193 nm with sources from krypton-fluoride (KrF) lasers and argon-fluoride (ArF) excimer lasers [5, 6]. Limited by its wavelength, DUV systems is unable to further reduced CD as one enters 7 nm technology node [7]. To break through this bottleneck, EUV based lithography system is proposed, enabling the transfer of patterns reliability for IV production of advanced technology node. Applying EUV (13.5 nm) light source [8, 9], the semiconductor industry is capable of mass-produce sub-10 nm integrated circuits (IC) and optimizing their overall operational speed, power consumption and circuit density aggressively. Monitoring the EUV light in the scanner chamber has become one of the key challenges to ensure the high uniformity, accuracy and stability in modern nanoelectronics manufacturing [10].

✉ Wei-Hwa Lin, whlin.starlab@gapp.nthu.edu.tw | [1]Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan. [2]College of Semiconductor Research, National Tsing Hua University, Hsinchu, Taiwan. [3]National Synchrotron Radiation Research Center, Hsinchu, Taiwan.

Table 1 Performance parameters of Different Sensors

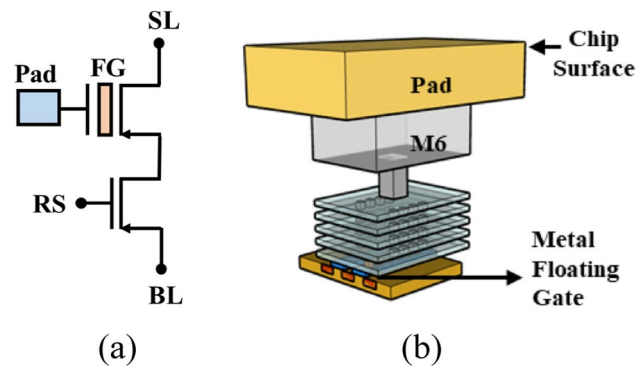| Detector	Spectral range	Spatial resolution	Detection power	Stability	CMOS compatibility
2T Detector	< 267 nm	67 μm	No need	Good	Fully compatible
Photodiode [26]	120 nm–250 nm	> 1 cm	High	Not stable	Not compatible
Photodiode [27]	< 220 nm	3.7 mm	High	Good	Not compatible
APS [28]	5 nm-1 μm	10 μm	Medium	Not stable	Highly compatible

Fig. 1 The **a** circuit schematic and **b** 3D structure of the proposed EUV detector, including 2 PMOS in series. Row select (RS) transistor is used for pixel selection, while EUV detection and data storage are achieved by the floating gate (FG) transistor in series to the select transistor

Previous studies [11, 12] have reported that EUV will be absorbed by air and thin films used in semiconductor ICs, including Cu (metal line) and SiO_2 (Inter Layer Dielectric, ILD), the most common materials in back-end-of-line process. In addition to ensure there is no outgassing in a vacuum environment, EUV monitoring generally requires specially designed detectors. Typically, silicon-based photodiode including Schottky photodiode are used in EUV lithography system, and the EUV responsivity is obtained by measuring the photocurrent [13–15]. However, continuous degradation of EUV detectors is reported on silicon-based photodiodes [13] which cannot endure long-term bombardment of high-energy photons. Besides, most EUV photodetectors require customized fabrication process [16], increasing the complexity of integrating the EUV photodiodes with read-out circuits, essential to building sizable pixel arrays.

Conventional CMOS compatible detectors, such as Active Pixel Sensor (APS) can be applied to EUV detection [17]. APS arrays with backside illumination can maintain some EUV sensitivity. Nevertheless, they still subject to degradation after long term exposure [17]. Also, external power supply is required on these conventional arrays to operation, which makes them less approachable for the environments in lithography chambers, such as high vacuum level or under liquid immersion [18–20].

In this work, an on-wafer, in-situ 2T pixel array for EUV sensing is proposed and demonstrated. 2T pixel array with buried sensing pad is proposed and demonstrated for detecting other sources in lithography system including DUV and electron beam. In this work, the proposed detector has been modified to be applied to in EUV detection [21–23]. Featuring CMOS logic process compatibility, the proposed 2T EUV detectors are directly made on Si-wafer, and can be placed in EUV scanner directly. Unlike traditional detectors with Si-based sensing layer [24], the proposed EUV detector uses metal sensing pads. The current generated through the photoelectric effect is immune to degradation after EUV bombardment. By in-line EUV detection and off-line reading, the compact 2T EUV detector can reflect the projected light intensity without any external power module, making it safe and accessible in processing chambers without any contamination concerns [25]. By analyzing EUV induced discharging on the proposed p-channel floating gate detector, an electron emission efficiency model is established. The proposed 2T pixel is capable of precisely reflecting the 2-dimensional EUV patterns, making it a promising solution of providing on-wafer light detection, feedback module for advanced lithography system. The performance parameters of the proposed sensor and other sensors are summarized in Table 1.

Pixel circuit and operation principles

The circuit schematic of the proposed 2T pixel for EUV sensing is shown in Fig. 1a. Two p-channel Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) are placed in series to construct a single pixel. Unlike traditional floating-gate-based device, there is no extra coupling structure to control the FG potential, EUV data read-out is completed by measuring the channel current affected by the FG potential. The row-select (RS) transistor is used for pixel selection during initialization step and data read-out, while EUV detection and data storage made possible by the floating gate (FG) transistor.

Previous studies have reported that EUV is well absorbed by dozens of materials [11, 12]; to collect the projected photons, the floating gate of the detectors are extended from metal gate to the surface pad, leading to a surface sensing node. The 3D structure of the proposed 2T EUV detector is illustrated in Fig. 1b. During EUV exposure, the high energy photons are directly projected onto the surface sensing pad (SSP) and excite the electrons stored in the FG transistor. The excited electrons with high energy will then overcome the energy barrier and escape from the floating gate, which lowers the floating gate potential. The Transmission Electron Microscope (TEM) photograph of the proposed EUV detector structure is in Fig. 2a and the cross-sectional view of the SSP is shown in Fig. 2b. During EUV exposure, the stored electrons are excited by 92 eV photons and leave the floating gate to the surface. The amount of charge-lost can reflect the EUV dosage, i.e., intensity × exposure time, as illustrated in Fig. 3a.

The relation between floating gate charge (Q_{FG}) and EUV induced electron discharging is crucial to the following analysis. The amount of excited Q_{FG} can precisely reflect the EUV flux intensity. Consequently, Q_{FG} extraction is the first step. Here, a specially-designed dummy cell, where the FG terminal can be directly probed and measured. In addition, the gate potential can be specified, therefore, the change in channel current with respect to FG potential, V_{FG}, can be directly observed. Based on measured BL current characteristics, three different regions can be identified as floating gate potential moves from 0 to more negative direction. In off region, the floating gate potential is lower than the threshold voltage (V_{th}). BL current is dominated by noise when floating gate potential is lower than the threshold voltage, therefore the amount of Q_{FG} cannot be determined [29, 30]. If V_{FG} is larger than V_{max}, FG cannot effectively retain stored charge. Therefore, this region is not suitable for EUV sensing. In the saturation region, the current is limited by RS transistor. Hence, measured the current is less sensitive to the floating gate potential in this circumstance, causing poor response toward EUV exposure. When floating gate transistor operates in the linear region, there is a linear dependency between channel current and floating gate potential, see Fig. 3b. When the proposed 2T EUV detector operates in the linear region, the detector holds the better sensitivity and is capable of reflecting the Q_{FG} level, hence it becomes the most desirable operation region. Before EUV exposure, it is best to raise
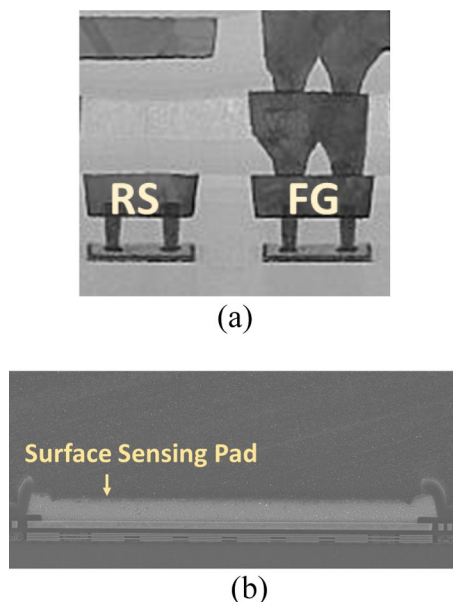

(a)

(b)

Fig. 2 The TEM photograph of **a** the propose EUV detector and **b** SSP. The detector samples are fabricated by 28 nm CMOS logic process
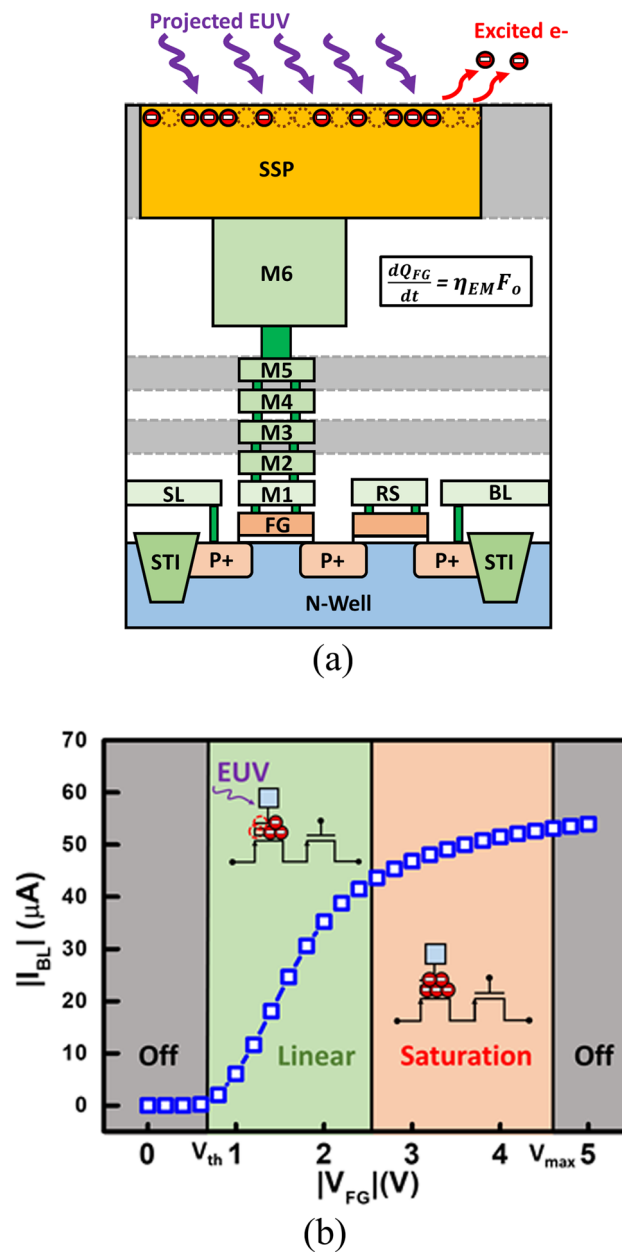
(a)

(b)

Fig. 3 **a** Illustration of the basic operation principle of this detector **b** The corresponding FG potential at different measured BL current. The three different detector's regions are proposed and shown in the insets

the floating gate potential to the boundary between linear and saturation region by hot-hole induced hot electron injection (HHIHEI) [31, 32] to achieve optimal response and large sensing window.

As the measurement data in Figs. 4 and 5 reveals, the EUV discharging behavior is demonstrated under EUV exposure, and the amount of stored Q_{FG} will gradually change as the exposure time increases. Based on the previous discussion, the V_{FG} can be extracted by fitting the measurement date with that from a dummy cell where its gate voltage can be directly applied. Then, the floating gate charge can be obtained as follow:

$$Q_{FG} = \left(V_{FG} - \alpha_D V_D\right) \times C_{FG}$$

where C_{FG} is the total capacitance from FG terminal, and V_D and α_D are the potential and coupling ratio from the drain side of FG transistor.
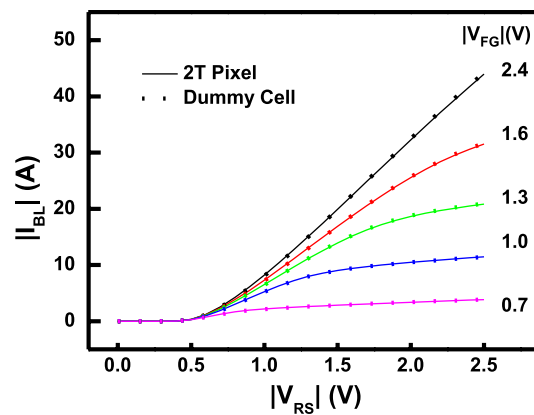
Fig. 4 The measurement of dummy cell (symbol) and floating-gate-based 2T pixel (line) is proposed, indicating that dummy cell fitting is reliable to extract the floating gate potential
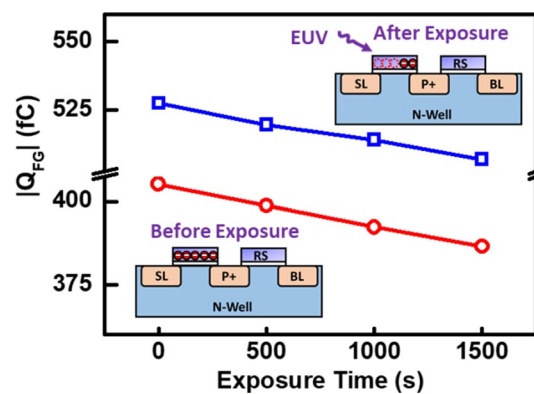

Fig. 5 EUV discharging characteristics are compared from demonstrated two different initial states set by initialization. FG charge excited by projected photons is lost, so the total number of stored electrons will gradually decrease

From the multiplication of floating gate potential (V_{FG}) and floating gate capacitance (C_{FG}), the Q_{FG} can be obtained and the discharging rates are summarized in Fig. 5, on detectors of two distinct initial states. During EUV exposure, the EUV photons will reach the SSP and excite the stored Q_{FG}. Subsequently, the floating gate potential and Q_{FG} will gradually decrease as the exposure time increases. The charge loss rate can be reflected by the measured BL current over time. Levels of ΔQ_{FG} is proportional to different flux intensities directly when exposure time are kept constant.

Experimental results and discussion

EUV discharging characteristic is collected from an EUV detector array, as shown on the circuit schematic of 4×4 pixel array in Fig. 6a, pixels are placed in a 2D array, where each pixel can be independently read on BLs sequentially [33, 34]. The top view of the 4×4 array from optical microscope (OM) is in Fig. 6b, where each white squares represents a surface sensing pads (SSP) with a pixel pith of 67 μm.

The measured I-V characteristics of the proposed 2T EUV detector are compared in Fig. 7, where the initialization step can place different amount of Q_{FG}, leading to different V_{FG}, as indicated. For a pixel in its fresh state, due to the absence of electrons in floating gate, floating gate transistor cannot be fully turned on, and thus the EUV 2T detector is typically stay in the off-state. By channel hot carrier injection, hot electrons are injected into the floating gate, which raising V_{FG}. By tuning the injection condition, the floating gate potential can be moved and positioned to the ideal levels, forcing the 2T detector to start at the linear/saturation region boundary, see Fig. 3b.

To investigate the discharging characteristics at different potential level, the floating gate potential of detectors on each row is initialized to different initial states ranging from 1.1 to 2.1 V. As the measured data in Fig. 8a shows, each
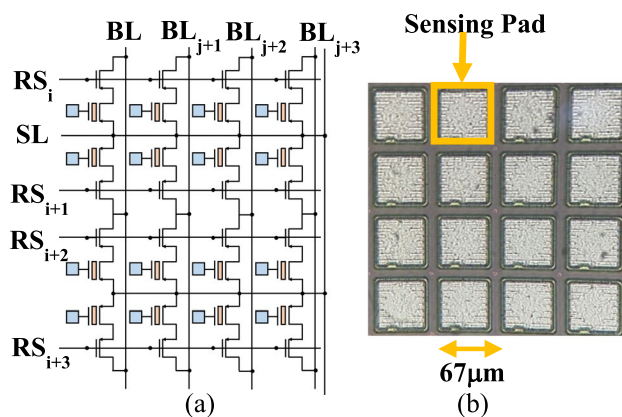
Fig. 6 **a** The circuit schematic of 4×4 2T pixel array and **b** the top view photograph from optical microscope, where the white square is sensing pad used for photon collection
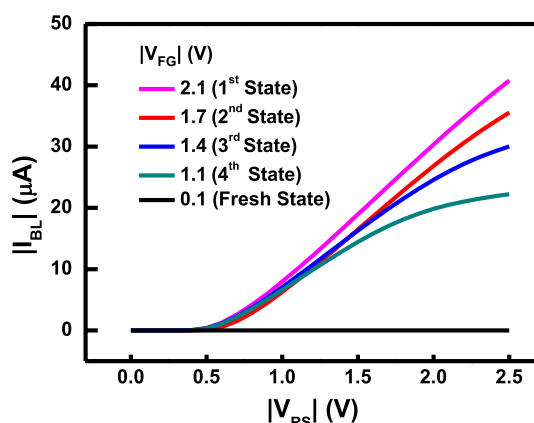

Fig. 7 Before EUV exposure, the floating gate potential of a 4×4 detector array is initialized to 4 initial states by different amount of hot electron injection

row is programed to one initial state to verify the relation between initial V_{FG} and its corresponding sensitivity. After 4.2 µW/cm^2 13.5 nm-EUV light exposure, the resulting V_{FG} and the shift of Q_{FG} are arranged in Fig. 8b and c respectively. As expected, V_{FG} becomes lower than initial state, indicate substantial amount of the electrons stored in floating gate has been excited by 13.5 nm photons and escaped from SSP. Furthermore, data in Fig. 8c reveals that under the same EUV exposure, pixels with higher initial V_{FG} are more responsive, namely, that more stored electrons are lost.

Here, the sensitivities of individual detectors evaluated and compared in Fig. 9, indicates a positive correlation between initial floating gate potential and responsivity. Under fixed EUV flux intensity (F_o), a linear dependency between the electric field across the gate oxide (E_{ox}) and the emission efficiency (η_{EM}) is found as follow [21]:

$$\eta_{EM}(E_{ox}) = AE_{ox} + B$$

where the fitted parameters are found to be $A = 0.1617$ (cm/MV), $B = 7.18 \times 10^{-4}$ (a.u.). Data also suggests that higher V_{FG} and E_{ox} result in higher emission efficiency and hence sensitivity, so the floating gate potential of the proposed EUV sensor is programmed to the edge between linear and saturation region, as indicated in Fig. 3, the best sensitivity and the largest sensing window can be obtained. According to Fig. 8c, a non-uniform mapping of Q_{FG} shift is found under uniform EUV light. Considering the E_{ox}-dependent emission model, the EUV distribution in the light field of 258 µm × 258 µm intensity can be more truthfully reflected, as shown in Fig. 10.
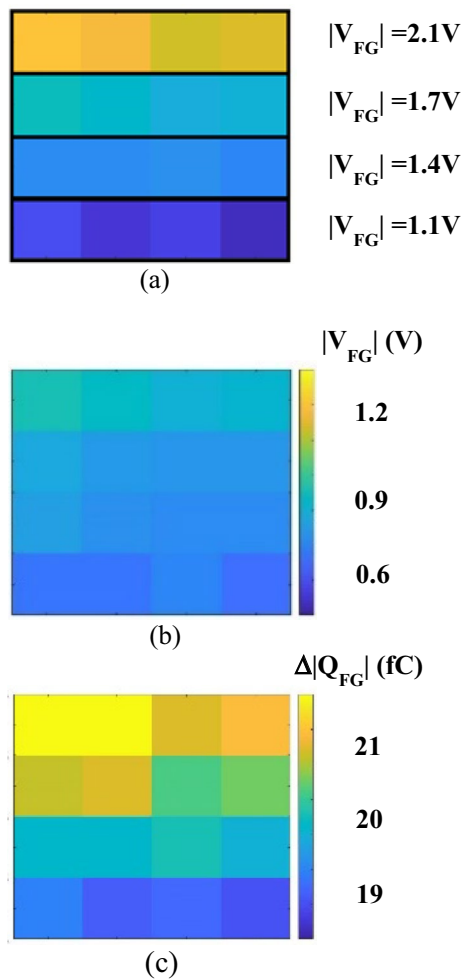
Fig. 8 The response of 4×4 sensor array mapping including the FG potential **a** before, **b** after EUV exposure are demonstrated, each row is placed to different initial state; the floating gate charge shift is in **c**
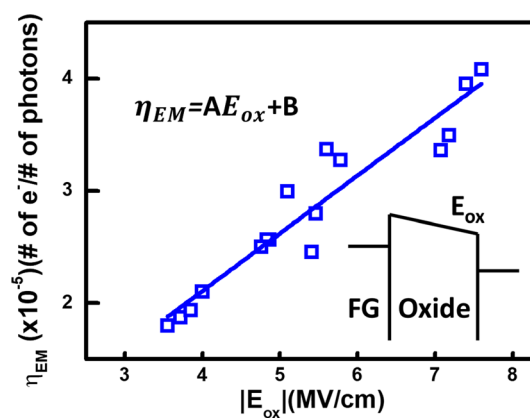

Fig. 9 The sensitivity of the proposed 2T pixel detector can be observed, indicating a positive correlation between initial FG potential and EUV sensitivity
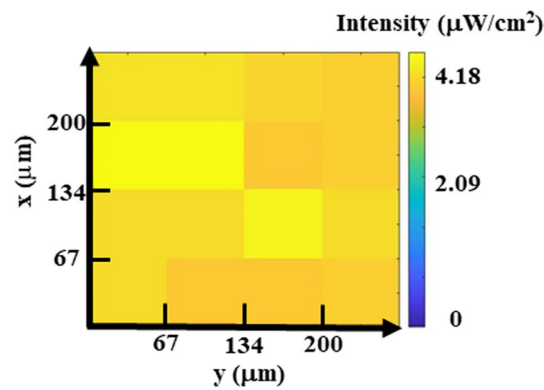
Fig. 10 After calibration, a uniform mapping of EUV flux distribution is obtained, proving that the proposed calibration model is a promising solution for EUV detection. This data suggests that through the η_{EM} model, one can obtain 2D EUV distribution on a 2T pixel array

Conclusions

In this study, a novel in-line EUV 2T detector featuring fully CMOS logic process compatibility, non-volatile data storage and high stability is proposed. The proposed 2T detector also exhibits high spectral range (< 267 nm) and spatial resolution (67 μm). Detection through proposed EUV induced discharging characteristic has also been studied comprehensively. With novel emission efficiency model, the proposed EUV 2T detector can accurately reflect the projected EUV flux intensity on the chip/wafer surface, for application in advanced lithography systems.

Data availability Not applicable.

Declarations

Competing interests The authors declare that they have no competing interests.

Ethics approval and consent to participate Not applicable.

Consent for publication The authors provide consent to publish.

References

1. DeBenedictis EP. It's time to redefine Moore's law again. Computer. 2017;50(2):72–5.
2. Thylen L. A Moores law for photonics. In: 2006 international symposium on biophotonics, nanophotonics and metamaterials, 2006. pp. 256–63.
3. Acharya K, et al. Monolithic 3D IC design: power, performance, and area impact at 7nm. In: 2016 17th international symposium on quality electronic design (ISQED), 2016.
4. Cheng S, et al. Optical critical dimension measurement for 16/14 nm FinFET. In: 2016 China semiconductor technology international conference (CSTIC), 2016. pp. 1–3
5. Razhev AM, et al. Highly efficient electric-discharge ArF and KrF excimer lasers with He as a buffer gas. In: Technical digest. CLEO/Pacific Rim 2001. 4th Pacific rim conference on lasers and electro-optics (Cat. No.01TH8557), 2001. p. II.
6. Watson T. Excimer lasers for DUV lithography. In: Technical digest. Summaries of papers presented at the conference on lasers and electro-optics. Conference edition. 1998 technical digest series, Vol. 6 (IEEE Cat. No.98CH36178); 1998. p. 122.
7. Yen A, et al. Enabling manufacturing of sub-10nm generations of integrated circuits with EUV lithography. In: 2019 electron devices technology and manufacturing conference (EDTM), 2019. pp. 475–7.
8. Wu Q, et al. A study of image contrast, stochastic defectivity, and optical proximity effect in EUV photolithographic process under typical 5 nm logic design rules. In: 2020 China semiconductor technology international conference (CSTIC), 2020. pp. 1–7.
9. Yeric G. IC design after Moore's Law. In: 2019 IEEE custom integrated circuits conference (CICC), 2019. pp. 1–150.
10. Shi L, et al. High performance silicon-based extreme ultraviolet (EUV) radiation detector for industrial application. In: 2009 35th annual conference of IEEE industrial electronics, 2009. pp. 1877–82.
11. Li Y, et al. A simulation study for typical design rule patterns and stochastic printing failures in a 5 nm logic process with EUV lithography. In: 2020 China semiconductor technology international conference (CSTIC), 2020. pp. 1–7.
12. Wang C-P, et al. On-wafer FinFET-based EUV/eBeam detector arrays for advanced lithography processes. IEEE Trans Electron Devices. 2020;67(6):2406–13.
13. Hu J, et al. 1 x 16 Pt/4H-SiC Schottky photodiode array for low-level EUV and UV spectroscopic detection. IEEE Photon Technol Lett. 2008;20(24):2030–2.
14. Shi L, et al. Electrical performance stability characterization of high-sensitivity Si-based EUV photodiodes in a harsh industrial application. In: IECON 2012 - 38th annual conference on IEEE industrial electronics society, 2012. pp. 3952–7.
15. Xia S, et al. Response time of silicon photodiodes for DUV/EUV radiation. In: 2008 IEEE instrumentation and measurement technology conference, 2008. pp. 1956–9.
16. Mohammadi V, et al. Stability characterization of high-performance PureB Si-photodiodes under aggressive cleaning treatments in industrial applications. In: 2015 IEEE international conference on industrial technology (ICIT), 2015. pp. 3370–6.
17. Stern RA, Shing L, Waltham N, Mapson-Menard H, Harris A, Pool P. EUV and soft X-Ray quantum efficiency measurements of a thinned back-illuminated CMOS active pixel sensor. IEEE Electron Device Lett. 2011;32(3):354–6.
18. Watanabe T. Current status and prospect for EUV lithography. In: 2017 7th international conference on integrated circuits, design, and verification (ICDV), 2017. pp. 2–7.
19. Suganuma T, et al. Laser produced plasma light source for next generation lithography. In: The 30th international conference on plasma science, 2003. ICOPS 2003. IEEE conference record - abstracts, 2003. p. 392.
20. Fujimori T. Negative-tone imaging (NTI) process for ArF immersion and EUV lithography to improve 'chemical stochastic'. In: 2021 international workshop on advanced patterning solutions (IWAPS), 2021. pp. 1–3.
21. Lin WH, et al. 2T-pixel sensors array for on-wafer in-chamber DUV sensing. In: 2022 international symposium on VLSI technology, systems and applications (VLSI-TSA), 2022. pp. 1–2.
22. Wang CP, et al. On-wafer electronic layer detectors array (ELDA) for e-beam imaging in advanced lithographic systems. In: 2021 international symposium on VLSI technology, systems and applications (VLSI-TSA), 2021. pp. 1–2.
23. Wang CP, et al. Detectors array for in situ electron beam imaging by 16-nm FinFET CMOS technology. Nanos Res Lett. 2021;16:93.
24. Okigawa M, Ishikawa Y, Samukawa S. "Reduction of ultraviolet-radiation damage in SiO_2 using pulse-time-modulated plasma and its application to charge coupled 44 device image sensor processes. J Vacuum Sci Technol B Microelectr Nanometer Struct Process Measur Phenom. 2003;21(6):2448.
25. Chuang J, et al. The construction of coherence microscope for extreme ultraviolet mask defect inspection in synchrotron facility. In: 2017 IEEE/SICE international symposium on system integration (SII), 2017. pp. 440–3.
26. BenMoussa A, Gissot S, Giordanengo B, Meynants G, Wang X, Wolfs B, Bogaerts J, Schuhle U, Berger G, Gottwald A, Laubis C, Kroth U, Scholze F, Soltani A, Saito T. Irradiation damage tests on backside-illuminated CMOS APS prototypes for the extreme ultraviolet imager on-board solar orbiter. IEEE Trans Nucl Sci. 2013;60(5):3907–14.
27. Kuschnerus P, Rabus H, Richter M, Scholze F, Werner L, Ulm G. Characterization of photodiodes as transfer detector standards in the 120 nm to 600 nm spectral range. Metrologia. 2003;35:355.
28. Lis K. Silicon photodiodes for low penetration depth beams such as DUV/VUV/EUV light and low-energy electrons. In: Betta G-FD, editor. Advances in photodiodes. InTech; 2011. https://doi.org/10.5772/15396.
29. Panda S, et al. Power, delay and noise optimization of a SRAM cell using a different threshold voltages and high performance output noise reduction circuit. In: 2009 4th international conference on computers and devices for communication (CODEC), 2009. pp. 1–4

30. Kuroda T, et al. Substrate noise influence on circuit performance in variable threshold-voltage scheme. In: Proceedings of 1996 international symposium on low power electronics and design, 1996. pp. 309–12.
31. Franco J, et al. Hot electron and hot hole induced degradation of SiGe p-FinFETs studied by degradation maps in the entire bias space. In: 2018 IEEE international reliability physics symposium (IRPS), 2018. p. 5A.
32. Lin FR, Hsu CC. New divided-source structure to eliminate instability of threshold voltage in p-channel flash memory using channel hot-hole-induced-hot-electron programming. In: 1999 International symposium on VLSI technology, systems, and applications. Proceedings of technical papers. (Cat. No.99TH8453), 1999. pp. 203–6.
33. Mekala VR. Methodology for characterization of NOR-NOR programmable logic array. In: 2008 Second Asia international conference on modelling & simulation (AMS), 2008. pp. 1025–8.
34. Malavena G, et al. Implementing spike-timing-dependent plasticity and unsupervised learning in a mainstream NOR flash memory array. In: 2018 IEEE international electron devices meeting (IEDM), 2018. p. 2.3.1–4.