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A complementary low-Schottky-barrier S/D-based nanoscale dopingless bidirectional reconfigurable field effect transistor with an improved forward current

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Abstract

In this paper, a nanoscale dopingless bidirectional RFET (BRFET) is proposed. Unlike conventional BRFETs, the proposed BRFET uses two different metal materials to form two different types of Schottky barriers on the interface between the S/D and silicon. For one of the two metal forms, the Schottky barrier height between the conduction band of the semiconductor and one of the two metal materials is lower than half of the energy band gap. The Schottky barrier height between the valence band of the semiconductor and the other kind of the two metal materials is lower than half of the energy band gap of the semiconductor. Therefore, a complementary low Schottky barrier (CLSB) is formed. Therefore, more carriers from the source electrode can easily flow into the semiconductor region through thermionic emission in both n-mode and p-mode compared to conventional BRFET operation, which generates carriers through the band-to-band tunneling effect. Therefore, a larger forward current can be achieved by the proposed CLSB-BRFET. The performance of the CLSB-BRFET is investigated by device simulation and compared with that of the BRFET. The working principle is interpreted through an analysis based on energy band theory. The output characteristics and reconfigurable function are also investigated and verified.

Keywords Schottky barrier height · Reconfigurable · Forward current · Field effect transistor

Abbreviations

RFET	The reconfigurable field effect transistor
BRFET	Bidirectional RFET
CMOS	Complementary metal oxide semiconductor
PG	Program gate
BTBT	Band-to-band tunneling
MOSFET	Metal oxide semiconductor field effect transistor
SB-MOSFET	Schottky barrier MOSFET
ϕ_{bp}	The height of the Schottky barrier for holes in the valence band
ϕ_{bn}	The height of the Schottky barrier for electrons in the conduction band

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S\D	Source/drain
CLSB-BRFET	Complementary low Schottky barrier source/drain (S/D)-based nanoscale dopingless bidirectional RFET
NiSi	Nickel silicide
PtSi	Platinum silicide
ErSi	Erbium silicide
L_{si}	The length of the semiconductor (silicon)
L_{CG}	The length of the control gate
L_{PG}	The length of the program gate
L_{sp}	The length of the spacer
t_{ox}	The HfO_2 oxide layer thickness
t_{si}	The thickness of the semiconductor (silicon)
W_{si}	The width of semiconductor (silicon)
ε_{HfO2}	The relative permittivity of HfO_2
ε_{spacer}	The relative permittivity of the spacer
$q\phi_{bn1}$	The barrier height between the ErSi S/D electrodes and the conduction band of the silicon
$q\phi_{bp1}$	The barrier height between the ErSi S/D electrodes and the valence band of the silicon
$q\phi_{bn2}$	The barrier height between the PtSi S/D electrodes and the conduction band of the silicon
$q\phi_{bp2}$	The barrier height between the PtSi S/D electrodes and the valence band of the silicon
$q\phi_{bn0}$	The barrier height between the NiSi S/D electrodes and the conduction band of the silicon
$q\phi_{bp0}$	The barrier height between the NiSi S/D electrodes and the valence band of the silicon
V_{DS}	The drain-to-source voltage
V_{GS}	The control gate to source voltage
V_{PG}	The program gate voltage
E_{FMS}	The Fermi energy level of the source electrode
E_{FMD}	The Fermi energy level of the source electrode
n	The electron concentration
n_s	The surface electron concentration
p	The hole concentration
p_s	The surface hole concentration
E_{FN}	The electron quasi-Fermi level
E_{FP}	The hole quasi-Fermi level
N_C	The effective density of states of the conduction band
N_V	The effective density of states of the conduction band
E_C	The band energy of the bottom of the conduction band
E_V	The band energy of the top of the valence band
V_{TH}	Threshold voltage
I_{on}/I_{off}	The on-state and off-state current ratio
SS	The subthreshold swing

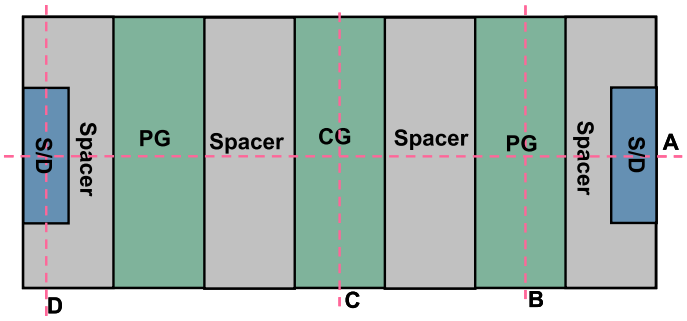
Introduction

Today, the minimum size of planar complementary metal oxide semiconductor (CMOS) integrated technology is about to reach the physical limit. Therefore, when the physical density of the circuit can no longer depend on the primary strategy of reducing the device size, it is necessary to find new, secondary ways to improve the functional density of the circuit. This means that the designers should use fewer devices to achieve richer functions through circuit design or develop new devices with richer functions through device design to reduce the dependence on the number of devices. Related research has become a hot issue in recent years. The reconfigurable field effect transistor (RFET) and bidirectional RFET (BRFET) have been proposed. As a single field effect transistor, the conduction mode can be configured as n-type or p-type by resetting the voltage applied on the program gate (PG) during operation [1, 2]. The RFET offers an advantage in logic arrays and enables various logic gates with fewer transistors than metal oxide semiconductor field effect transistor (MOSFET)-based CMOS technology [3–7]. To realize the reconfigurable function, the RFET needs to form a high Schottky barrier on the source side between the metal source and the conduction band of the semiconductor and the valence

band of the semiconductor at the same time. Thereafter, nickel silicide (NiSi) is usually adopted to form a Schottky barrier in RFETs. The Schottky barrier height formed between NiSi and the semiconductor conduction band $q\phi_{bn0}$ is similar to that formed between NiSi and the semiconductor valence band $q\phi_{bp0}$ [8]. This is appropriate for reconfiguration operation. The PG is used to generate a strong field effect on the source side to overcome the Schottky barrier, which prevents the carriers flowing from the source electrode into the conduction band or valence band of the semiconductor region. Through the strong field effect, band bending is generated in the semiconductor near the source side, and the band-to-band tunneling (BTBT) effect occurs and generates electron–hole pairs. If the voltage applied on the PG (V_{PG}) is positive, electrons accumulate in the semiconductor region near the source electrode, and the device works in n-mode, while if V_{PG} is negative, holes accumulate, and the device works in p-mode. Therefore, the magnitude of the PG voltage determines the intensity of band bending and the corresponding number of carriers generated by BTBT, and the polarity of the PG voltage determines the type of carriers that the source can provide and determines the conduction type of the RFET. However, because the number of carriers generated by the tunneling effect is limited, the forward conduction current of the conventional BRFET is much smaller than that of the MOSFET, which is a fundamental disadvantage of the unique Schottky barrier-based RFET. Moreover, the Schottky barrier MOSFET (SB-MOSFET) is also a type of device that forms metallic source/drain (S/D) junctions instead of the p–n junctions formed in the MOSFET [9–11]. In addition, the metallic S/D architecture holds the advantage of relaxing the severe constraints imposed on the conventional implanted S/D of MOSFETs. Taking p-type SB MOSFETs as an example, the height of the Schottky barrier for holes in the valence band ϕ_{bp} is much smaller than that for electrons in the conduction band ϕ_{bn}. Therefore, unlike the RFET, the SB-MOSFET uses metal materials with smaller ϕ_{bn} (n-type) or ϕ_{bp} (p-type) to reduce the height of the Schottky barrier as much as possible. This makes it unnecessary for carriers to flow into semiconductors through the BTBT effect, but they can directly flow into silicon in massive quantities through thermionic emissions. The forward current can be largely enhanced by reducing the height of the Schottky barrier. However, like the RFET, the SB-MOSFET is also a device with a unique metal silicide S/D based on a hologenetic S/D Schottky barrier. Because the sum of $q\phi_{bn}$ and $q\phi_{bp}$ equals the energy band gap of the semiconductor, if a material achieves a lower $q\phi_{bn}$, then $q\phi_{bp}$ is large. Therefore, for example, even if a conventional BRFET adopts a low $q\phi_{bn}$ material to form the source electrode, only the forward current in n-mode can be effectively enhanced, and the carriers that are supplied in p-mode still depend on BTBT. Based on the above analysis, we found that if we use a material that forms a high Schottky barrier for both the conduction band and the valence band, the forward conduction current is low in both p-mode and n-mode. If we use a material that forms a low Schottky barrier for either the conduction band or for the valence band, the forward current can be improved only in one mode, while the forward current cannot readily be improved in the other mode. Therefore, to improve the forward current of the BRFET in both modes, in this paper, we propose a complementary low-Schottky-barrier S/D-based nanoscale dopingless bidirectional RFET (CLSB-BRFET). Unlike devices that adopt only one type of metal material to form the S/D electrodes, such as the conventional BRFET or SB MOSFET, the proposed CLSB-BRFET utilizes two different metal materials to form two different types of Schottky barriers on the interface between the S/D and silicon. This means that both a low ϕ_{bn} and a low ϕ_{bp} Schottky barrier can be achieved simultaneously. A low ϕ_{bn} Schottky barrier can be formed on the interface between ErSi and silicon with $\phi_{bn} \sim 0.25$ V [12], and a low ϕ_{bp} Schottky barrier can be formed on the interface between platinum silicide (PtSi) and silicon with $\phi_{bp} \sim 0.25$ V [13, 14]. Therefore, when the PG is exposed to a positive voltage, the material that forms the lower ϕ_{bn} becomes dominant. The electrons from the source electrode can easily flow into the semiconductor region mainly through the lower-ϕ_{bn} Schottky barrier due to thermionic emission but not through the other material, which forms a higher ϕ_{bn} due to BTBT. When the PG is exposed to a negative voltage, the holes from the semiconductor can easily flow into the source electrode through the lower-ϕ_{bp} Schottky barrier due to thermionic emission but not through the other material, which forms a higher ϕ_{bp} due to BTBT. In this work, the characteristics of the proposed CLSB-BRFET are compared with those of the conventional BRFET, and the working principle is interpreted through an analysis based on energy band theory. Compared to the conventional BRFET, the proposed CLSB-BRFET can achieve a much higher on-state current and much lower static power consumption.

Methods

Figure 1a shows the top view of the proposed CLSB-BRFET, and Fig. 1b–e show the cross-sectional views along cut line A, cut line B, cut line C, and cut line D of Fig. 1a, respectively. Figure 1f shows the cross-sectional view along cut line A of Fig. 1b. Figure 1g shows a cross-sectional view of a conventional unique Schottky-barrier-based BRFET. L_{si} is the length of the silicon, L_{CG} is the length of the CG, L_{PG} is the length of the PG on either the source or side, L_{sp} is the length of the



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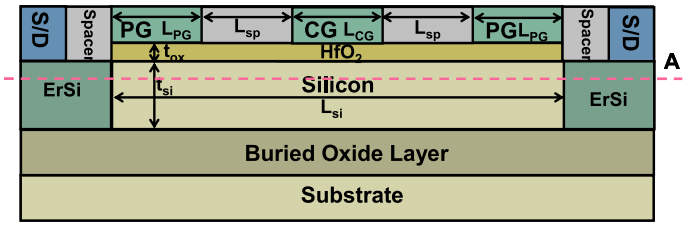

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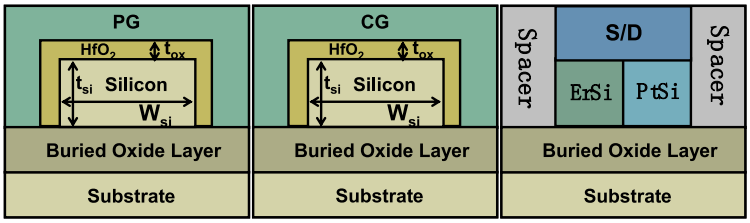
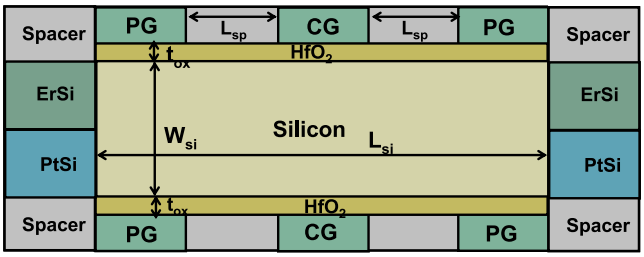


(c) (d) (e)



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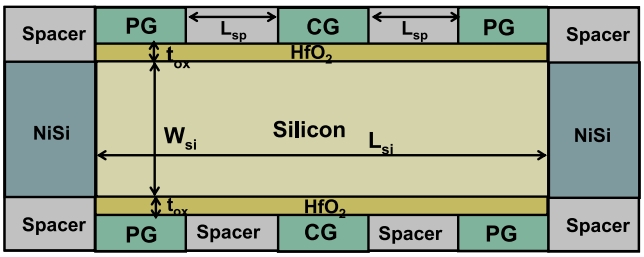


(g)

Fig. 1 **a** The top view of the proposed CLSB-BRFET, **b** the cross-sectional views along cut line A of **a**, **c** the cross-sectional views along cut line B of **a**, **d** the cross-sectional views along cut line C of **a**, **e** the cross-sectional views along cut line D of **a**, **f** the cross-sectional view along cut line A of **b**, and **g** a cross-sectional view of a conventional unique Schottky barrier-based BRFET

spacer between the CG and the PG, t_{si} is the thickness of silicon, t_{ox} is the HfO_2 gate oxide thickness, W_{si} is the width of the silicon, ε_{HfO2} is the relative permittivity of HfO_2, ε_{spacer} is the relative permittivity of the spacer, $q\phi_{bn1}$ is the barrier height between the first kind of metal, erbium silicide (ErSi), of the S/D electrodes and the conduction band of silicon, $q\phi_{bp1}$ is the barrier height between the first kind of metal (ErSi) of the S/D electrodes and the valence band of the silicon, $q\phi_{bn2}$ is the barrier height between the second kind of metal (PtSi) of the S/D electrodes and the conduction band of the silicon, and $q\phi_{bp2}$ is the barrier height between the second kind of metal (PtSi) of the S/D electrodes and the valence band of the silicon. The parameter selection for the CLSB-BRFET is shown in Table 1. The parameters of the conventional BRFET are selected to be as consistent as possible with the parameters of the CLSB-BRFET. The device performances are verified through SILVACO Atlas tools [15]. The Atlas device simulation tool consists of a set of fundamental equations that link the electrostatic potential and the carrier densities. These equations, which are solved inside any general-purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the continuity equations, and the drift–diffusion transport equations. Poisson's equation relates variations in electrostatic potential to local charge densities. The continuity and transport equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes. The drift–diffusion transport model, Fermi–Dirac statistic model, Auger recombination model, FN tunnel model and BTBT model are all turned on in all simulation work.

Table 1 Parameter selection for the CLSB-BRFET and BRFET

Parameters	Values/Units
The length of the semiconductor (silicon) (L_{si});	30 nm
The length of the control gate (L_{CG});	6 nm
The length of the program gate (L_{PG});	6 nm
The length of the spacer (L_{sp})	6 nm
The HfO_2 oxide layer thickness (t_{ox});	1 nm
The thickness of the semiconductor (silicon) (t_{si});	5 nm
The width of the semiconductor (silicon) (W_{si});	5 nm
The relative permittivity of HfO_2 (ε_{HfO2});	21.976
The relative permittivity of the spacer (ε_{spacer});	3.89
The barrier height between the ErSi S/D electrodes and the conduction band of the silicon ($q\phi_{bn1}$);	0.25 eV
The barrier height between the ErSi S/D electrodes and the valence band of the silicon ($q\phi_{bp1}$);	0.83 eV
The barrier height between the PtSi S/D electrodes and the conduction band of the silicon ($q\phi_{bn2}$);	0.83 eV
The barrier height between the PtSi S/D electrodes and the valence band of the silicon ($q\phi_{bp2}$);	0.25 eV
The barrier height between the NiSi S/D electrodes and the conduction band of the silicon ($q\phi_{bn0}$);	0.56 eV
The barrier height between the NiSi S/D electrodes and the valence band of the silicon ($q\phi_{bp0}$);	0.52 eV
The drain to source voltage (V_{DS})	− 0.6 V–0.6 V
The control gate to source voltage (V_{GS})	− 0.6 V–0.6 V
The program gate voltage (V_{PG})	− 0.6 V–0.6 V
The Fermi level of the source electrode (E_{FMS})	0 eV
The Fermi level of the source electrode (E_{FMD})	− 0.4 eV
The electron concentration (n)	cm^{-3}
The surface electron concentration (n_s)	cm^{-3}
The hole concentration (p)	cm^{-3}
The surface hole concentration (p_s)	cm^{-3}
The electron quasi-Fermi level (E_{FN})	eV
The hole quasi-Fermi level (E_{FP})	eV
The effective density of states of the conduction band (N_C)	cm^{-3}
The effective density of states of the conduction band (N_V)	cm^{-3}
The band energy of the bottom of the conduction band (E_C)	eV
The band energy of the top of the valence band (E_V)	eV
The threshold voltage (V_{TH})	V
The on-state and off-state current ratio (I_{on}/I_{off})	
The subthreshold swing (SS)	mV/decade

There are two kinds of Schottky barriers formed between the S/D electrodes and the semiconductor (silicon). We take an n-mode operation as an example. Because $q\phi_{bn1}$ is much smaller than $q\phi_{bp1}$, the Schottky barrier between ErSi and the conduction band of the silicon is lower than the Schottky barrier between ErSi and the valence band of the silicon. Therefore, when the PG is positively biased, the electrons from the source metal material, ErSi, more easily flow into the conduction band of the silicon through the thermionic emission effect compared to operation of the conventional unique Schottky barrier-based BRFET.

Results and discussion

Figure 2a shows a comparison of the transfer characteristics between the CLSB-BRFET and the conventional BRFET with different S/D metal materials in n-mode. Figure 2b shows the comparison of transfer characteristics between the CLSB-BRFET and the conventional BRFET with different S/D metal materials in p-mode. It is obvious that the CLSB-BRFET is the only device of the group that can achieve a higher forward conduction current and better subthreshold characteristics in both n-mode and p-mode at the same time. As Fig. 2a shows, for the conventional BRFET with the ErSi S/D electrode, the Schottky barrier height between the S/D electrode and the conduction band of the semiconductor is smaller than

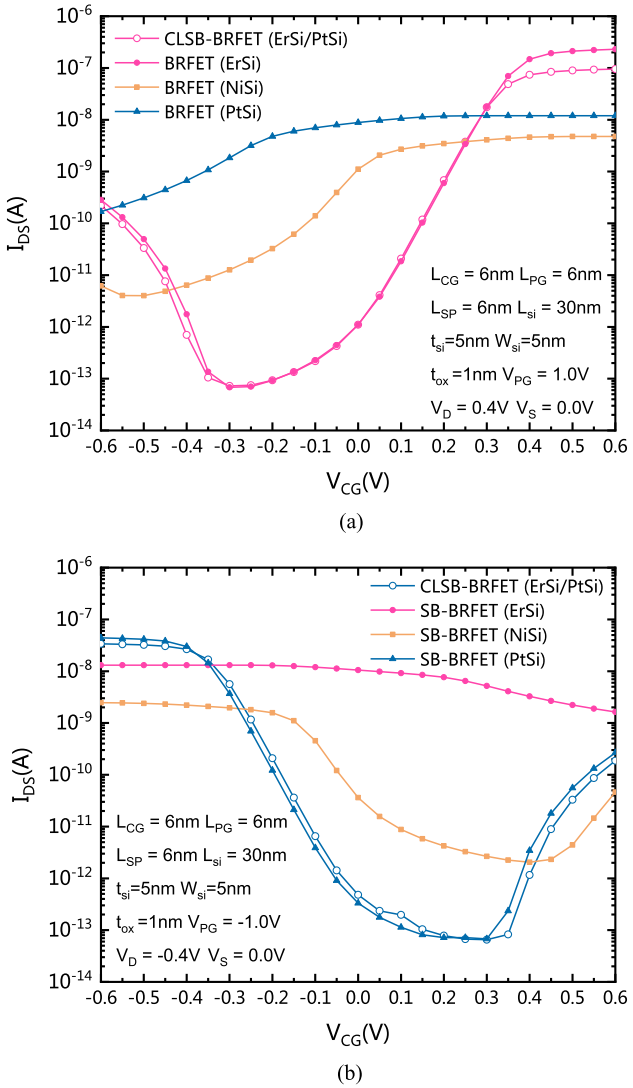


Fig. 2 **a** Comparison of transfer characteristics between the CLSB-BRFET and conventional BRFETs with different S/D materials in n-mode. **b** Comparison of transfer characteristics between the CLSB-BRFET and conventional BRFETs with different S/D materials in p-mode

in the other cases. Therefore, the forward current of the BRFET with ErSi S/D electrodes in n-mode is the largest. Because the CLSB-BRFET uses both ErSi and PtSi as the S/D metal materials, when the device works in n-mode, the forward current generated by thermionic emission through the ErSi in the conduction band is much larger than that generated by BTBT. In this case, the role of the ErSi becomes dominant. Similarly, as Fig. 2b shows, for the conventional BRFET with the PtSi S/D electrode, the Schottky barrier height between the S/D electrode and the valence band of the semiconductor is smaller than in the other cases. Therefore, the forward current of the BRFET with PtSi S/D electrodes in p-mode is the largest. For the CLSB-BRFET in p-mode, the forward current generated by thermionic emission through the PtSi in the valence band is also much larger than that generated by BTBT. In this case, the role of the PtSi is dominant.

Figure 3a shows the electron concentration of the CLSB-BRFET near the source side in n-mode and the hole concentration of the CLSB-BRFET near the source side in p-mode. Figure 3b shows the electron concentration of the BRFET with ErSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with ErSi S/D electrodes near the source side in p-mode. Figure 3c shows the electron concentration of the BRFET with NiSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with NiSi S/D electrodes near the source side in p-mode. Figure 3d shows the electron concentration of the BRFET with PtSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with PtSi S/D electrodes near the source side in p-mode. For the CLSB-BRFET, when the PG is positively biased, it works in n-mode, and the electrons flow into the semiconductor region through the ErSi part of the source electrode. The electron concentration can be expressed as

$$n = N_C \exp\left(\frac{E_{FN} - E_C}{kT}\right) \tag{1}$$

On the surface between the silicon and source electrode, the band energy difference between E_{FN} and E_C equals $-q\phi_{bn}$. Therefore, the surface electron concentration can be expressed as

$$n_s = N_C \exp\left(\frac{-q\varphi_{bn}}{kT}\right) \tag{2}$$

For ErSi, $q\phi_{bn1}$ is approximately 0.25 V, which is the smallest among ErSi, NiSi and PtSi; therefore, the surface electron concentration of ErSi is the largest. That is approximately 10^{15} cm^{-3}; for NiSi, n_s is approximately 10^{11} cm^{-3}, and for PtSi, n_s is approximately 10^6 cm^{-3}. Similarly, the hole concentration can be expressed as

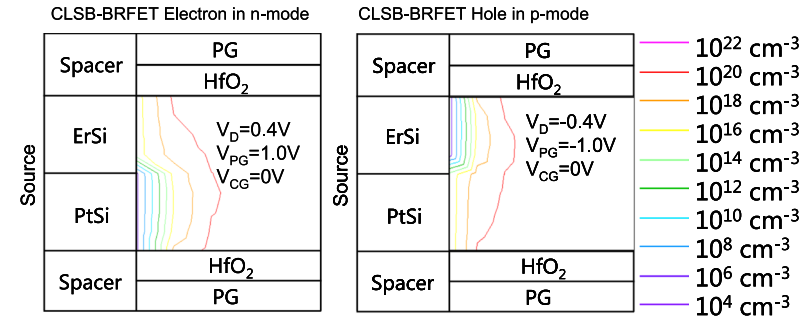
$$p = N_V \exp\left(\frac{E_V - E_{FP}}{kT}\right) \tag{3}$$

On the surface between the silicon and source electrode, the band energy difference between E_{FP} and E_V equals $-q\phi_{bp}$. Therefore, the surface hole concentration can be expressed as

$$p_s = N_V \exp\left(\frac{-q\varphi_{bp}}{kT}\right) \tag{4}$$

For ErSi, $q\phi_{bn1}$ is approximately 0.83 V, the largest value among ErSi, NiSi and PtSi; therefore, the surface hole concentration of ErSi is the smallest. That is approximately 10^6 cm^{-3}; for NiSi, p_s is approximately 10^{11} cm^{-3}, and for PtSi, p_s is approximately 10^{15} cm^{-3}.

Figure 4a and b show the comparison of band energy distributions and carrier concentration distributions between the CLSB-BRFET and the conventional BRFET in the forward biased state in n-mode, respectively. As Fig. 4a shows, the band energy is pulled down under the joint action of both the PG and the CG for all devices. However, because the Schottky barrier heights between the source and silicon are different, because electrons are the majority carrier, the surface electron concentrations of these devices are also different. Therefore, the source contact resistances are also different. For the proposed CLSB-BRFET in n-mode, the source contact resistance and the electron concentration distribution are dominated by the ErSi. Therefore, as Fig. 4b shows, the electron distribution of the CLSB-BRFET is also similar to that of the conventional BRFET with ErSi S/D electrodes. Note that even though the lowest electron concentrations of the BRFET with NiSi or PtSi S/D electrodes are larger than those of the BRFET with ErSi S/D electrodes, the forward on-state current of the BRFET with NiSi or PtSi S/D electrodes is still smaller than that of the BRFET with ErSi S/D electrodes. When the lowest electron concentration of the BRFET exceeds the surface electron concentration n_s, the resistance generated by



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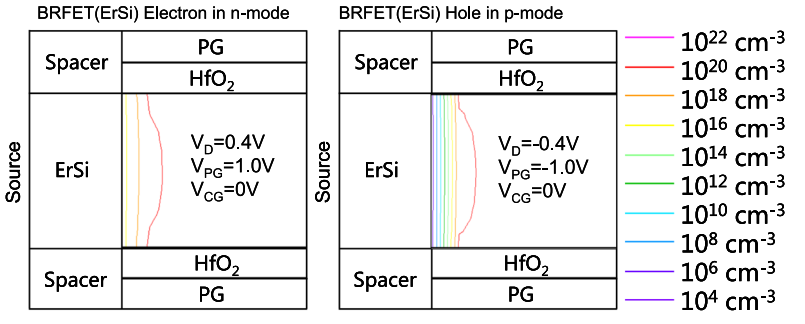

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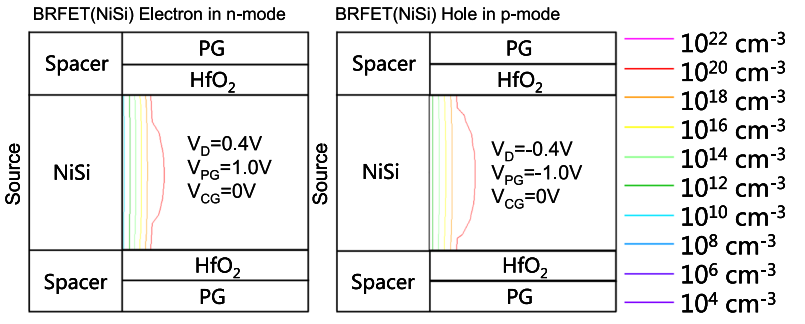

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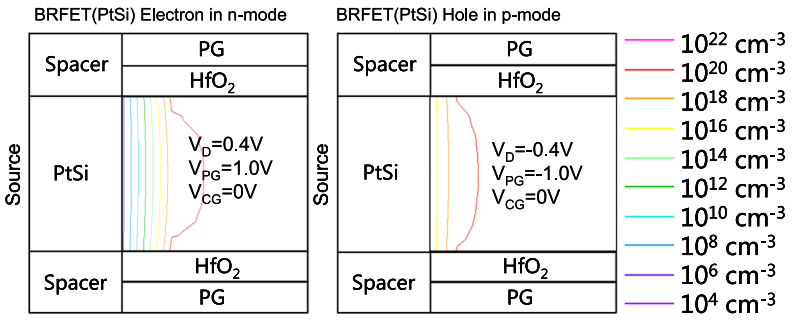


(d)

Fig. 3 **a** The electron concentration of the CLSB-BRFET near the source side in n-mode and hole concentration of the CLSB-BRFET near the source side in p-mode. **b** The electron concentration of the BRFET with ErSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with ErSi S/D electrodes near the source side in p-mode. **c** The electron concentration of the BRFET with NiSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with NiSi S/D electrodes near the source side in p-mode. **d** The electron concentration of the BRFET with PtSi S/D electrodes near the source side in n-mode and the hole concentration of the BRFET with PtSi S/D electrodes near the source side in p-mode

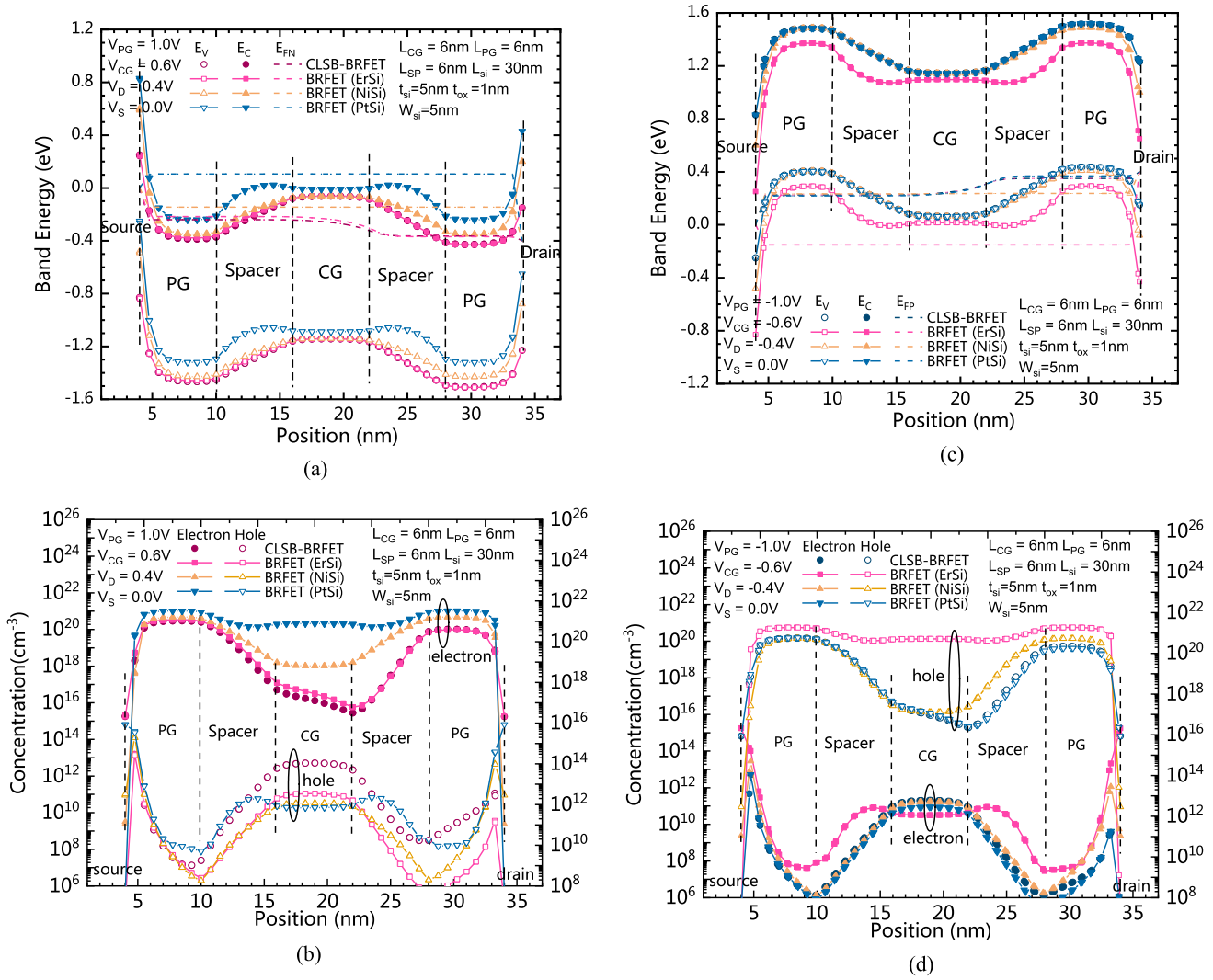


Fig. 4 **a** The comparison of the band energy distribution between the CLSB-BRFET and BRFETs with different S/D materials in the forward state of the n-mode. **b** The comparison of the carrier concentration distribution between the CLSB-BRFET and BRFETs with different S/D materials in the forward state of the n-mode. **c** The comparison of the band energy distribution between the CLSB-BRFET and BRFETs with different S/D materials in the forward state of the p-mode. **d** The comparison of the carrier concentration distribution between the CLSB-BRFET and BRFETs with different S/D materials in the forward state of the p-mode

the Schottky contact becomes dominant, and the forward current of the device cannot be further promoted by increasing V_G. This is also the reason that we use the material with the smallest possible $q\phi_{bn}$ in n-mode. Figure 4c and d show a comparison of the band energy distributions and carrier concentration distributions between the CLSB-BRFET and the conventional BRFET in the forward biased state in p-mode, respectively. As Fig. 4c shows, the band energy is pulled up under the joint action of both the PG and the CG for all devices. Because holes are the majority carrier, the surface hole concentrations of these devices are also different. Therefore, the source contact resistances in p-mode are also different. For the proposed CLSB-BRFET in p-mode, the source contact resistance and the hole concentration distribution are dominated by the PtSi. Therefore, as Fig. 4d shows, the hole distribution of the CLSB-BRFET is also similar to that of the conventional BRFET with PtSi S/D electrodes. Similar to the n-mode, when the smallest hole concentration of the BRFET exceeds the surface hole concentration n_s, the resistance generated by the Schottky contact becomes dominant, and the forward current of the device cannot be further promoted by decreasing V_G. The material with the smallest possible $q\phi_{bp}$ should be adopted in p-mode.

Figure 5a and b show the band energy distributions and carrier concentration distributions of both the CLSB-BRFET and the conventional BRFET in the static state of the n-mode, respectively. E_{FN} of the BRFET with PtSi in the central part is the highest among all devices. E_C in the central part of all devices is almost the same. Therefore, according to Formula

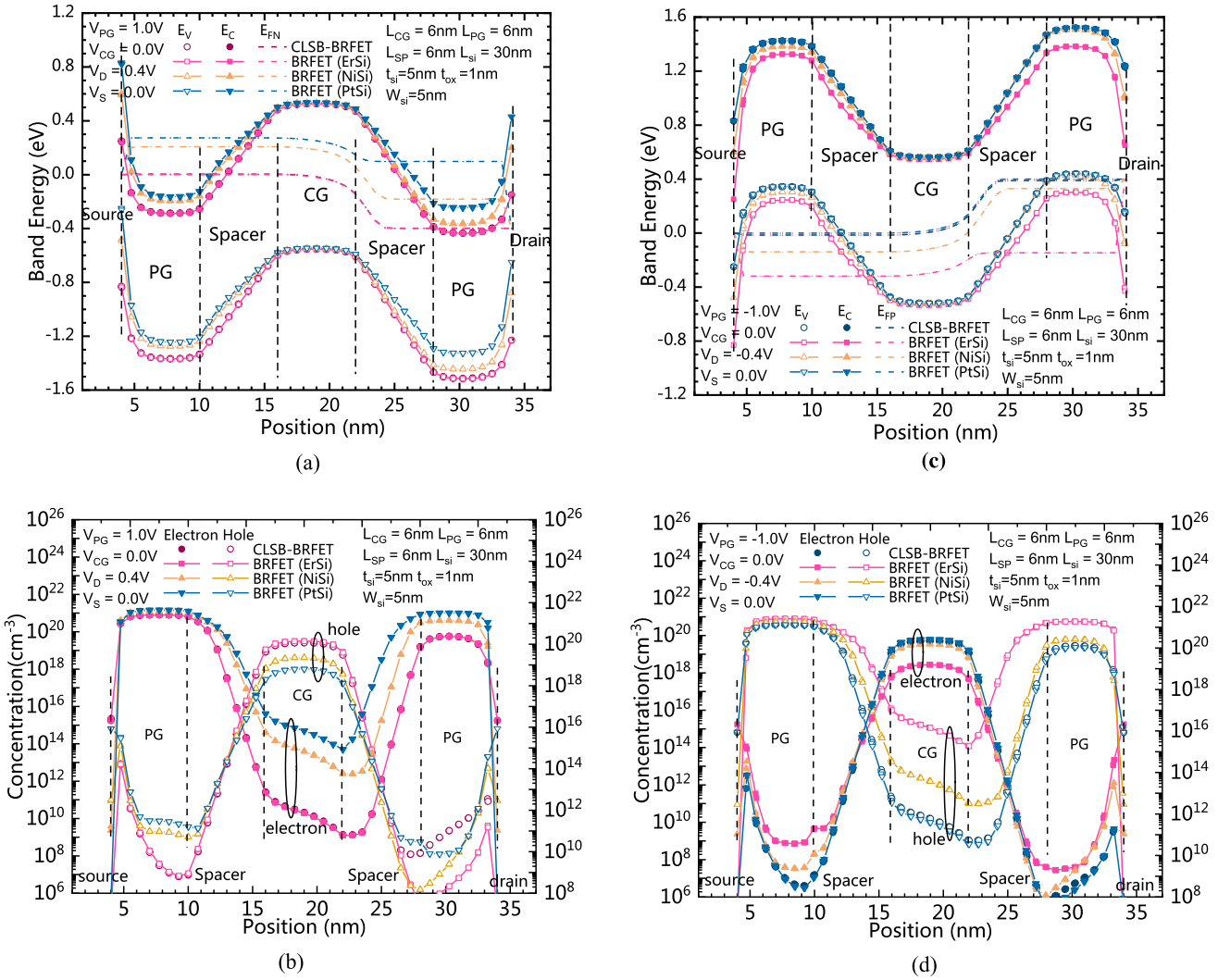


Fig. 5 **a** The comparison of the band energy distribution between the CLSB-BRFET and the conventional BRFETs in the static state of the n-mode. **b** The carrier concentration distributions between the CLSB-BRFET and the conventional BRFETs in the static state of the n-mode. **c** The comparison of band energy distribution between the CLSB-BRFET and the conventional BRFETs in the static state of the p-mode. **d** The carrier concentration distributions between the CLSB-BRFET and the conventional BRFETs in the static state of the p-mode

(1), as Fig. 5b shows, the electron concentration in the central part of the BRFET with PtSi S/D electrodes is the highest among these devices. Therefore, the static leakage current of the BRFET with PtSi S/D electrodes is the largest in n-mode. Because the ErSi is dominant for the proposed CLSB-BRFET in n-mode, as Fig. 2a shows, the static and subthreshold currents of the CLSB-BRFET are similar to those of the BRFET with ErSi S/D electrodes. Figure 5c and d show the band energy distribution and carrier concentration distributions of both the CLSB-BRFET and the conventional BRFET in the static state of the p-mode, respectively. E_{FP} of the BRFET with ErSi in the central part is the lowest among all devices. E_V in the central part of all devices is almost the same. Therefore, according to Formula (3), as Fig. 5d shows, the hole concentration in the central part of the BRFET with ErSi S/D electrodes is the highest among these devices. Therefore, the static leakage current of the BRFET with ErSi S/D electrodes is the largest in p-mode. Because PtSi is dominant for the proposed CLSB-BRFET in p-mode, as Fig. 2b shows, the static and subthreshold currents of the CLSB-BRFET are similar to those of the BRFET with PtSi S/D electrodes in p-mode.

Figure 6a and b show a comparison of band energy distributions and carrier concentration distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the n-mode, respectively. When the PG is positively biased and the CG is negatively biased, for both the CLSB-BRFET and the BRFETs, electrons are gathered in the semiconductor regions under the PG, while holes are gathered in the semiconductor region under the CG. As Fig. 6b shows, the semiconductor near the S/D sides is N-type, while the semiconductor at the central region is P-type. The p-type

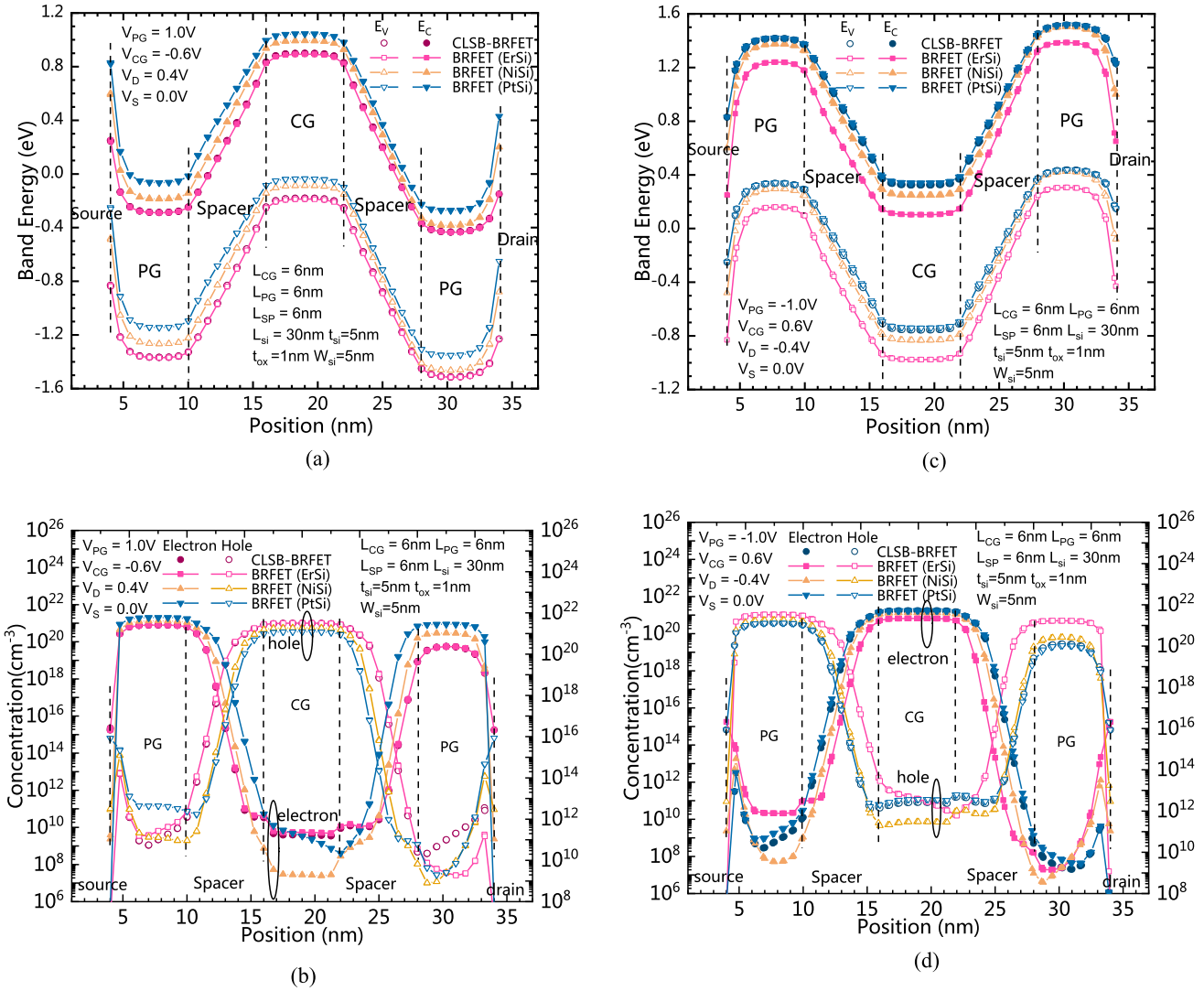


Fig. 6 **a** The comparison of band energy distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the n-mode. **b** The carrier concentration distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the n-mode. **c** The comparison of band energy distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the p-mode. **d** The carrier concentration distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the p-mode

semiconductor in the central region and the n-type semiconductor near the drain side form a reversely biased PN junction when V_D is positive. Therefore, all devices are in the reverse cutoff state. As Fig. 6a shows, there is strong energy band bending between the CG and PG, and the energy band bending degree of all devices is almost equal. Currently, BTBT is the dominant mechanism for generating reverse leakage current. However, as Fig. 2a shows, there are some differences in the leakage current generated by different devices. The difference in S/D contact mainly causes these differences. For the CLSB-BRFET and BRFET (ErSi), as Fig. 6a shows, the built-in potential generated in the semiconductor near the drain side is much smaller than that generated by BRFET (NiSi) and BRFET (PtSi). Therefore, the electrons produced by the BTBT effect caused by the energy band bending between the CG and PG are more likely to flow out from the drain electrode. For BRFET (NiSi), the built-in potential generated is smaller than that generated by the CLSB-BRFET and BRFET (ErSi), so the electrons do not easily flow out of the drain electrode under the effect of the built-in potential. For BRFET (PtSi), although its built-in potential is the largest, the energy band bending at the interface between the semiconductor and drain electrode is also the largest. Therefore, the strongest BTBT phenomenon occurs at this interface, so the leakage current generated by BRFET (PtSi) is also greater than that generated by BRFET (NiSi). However, from another point of view, for BRFET (PtSi) and BRFET (NiSi), the potential difference between the central semiconductor region under the CG

and the semiconductor region on the drain side is smaller than that of the CLSB-BRFET. Therefore, the reverse bias degree of different devices is also not the same. For BRFET (NiSi) and BRFET (PtSi), the potential differences between the center and the drain side are smaller than those of BRFET (ErSi) and the CLSB-BRFET. Therefore, compared with BRFET (ErSi) and the CLSB-BRFET, when V_{CG} equals − 0.6 V, for BRFET (NiSi) and BRFET (PtSi), their subthreshold states have just ended, while the reverse cutoff states have just begun, while for BRFET (ErSi) and the CLSB-BRFET, their subthreshold state ends earlier. In other words, BRFET (ErSi) and the CLSB-BRFET are in a deeper reverse bias state. Figure 6c shows a comparison of band energy distributions between the CLSB-BRFET and the conventional BRFETs in the reverse cutoff state of the p-mode. Figure 6d shows the carrier concentration distributions between the CLSB-BRFET and the conventional BRFET in the reverse cutoff state of the p-mode. For the p-mode, the situation of BRFET (ErSi) and BRFET (PtSi) is reversed. Similar to the forward and static states, the reverse leakage of the CLSB is also equivalent to that of BRFET(PtSi) in p-mode. Due to the high similarity between n-mode and p-mode, only the voltage applied by each electrode is reversed, so the analysis is not repeated here.

Figure 7a–c compare the I_{on}/I_{off} current ratio, the subthreshold swing (SS) and the threshold voltage (V_{TH}) between the CLSB-BRFET and the conventional BRFETs, respectively. As Fig. 7a shows, if V_{PG} is appropriately selected and large enough, V_D does not affect the I_{on}/I_{off} ratio. The I_{on}/I_{off} ratio of the CLSB-BRFET is much larger than that of the conventional BRFET with NiSi S/D electrodes. As Fig. 7b shows, if V_D is increased, the SS is slightly degraded. The SS of the CLSB-BRFET is much smaller than that of the NBRFET with NiSi S/D electrodes. The average SS of the proposed CLSB-BRFET is about 80 mV/dec, while the minimum SS of the NBRFET with NiSi S/D electrodes is larger than 100 mV/dec. As Fig. 7c shows, the V_{TH} is not obviously affected by V_D, the V_{TH} of the conventional NBRFET is approximately 0 V, and the V_{TH} of the proposed CLSB-NBRFET is approximately 0.22 eV, which is larger than 0 V; therefore, the proposed device is more suitable for use as a reconfigurable device.

Figure 8a shows the comparison of the transfer characteristics of the CLSB-BRFET with different V_{PG} in n-mode. Figure 8b shows the comparison of the transfer characteristics of the CLSB-BRFET with different V_{PG} in p-mode. Because two metal materials are used, one of which forms a low Schottky barrier on the interface between the metal and the conduction band and the other forms a low Schottky barrier on the interface between the corresponding metal and the valence band, it is necessary to apply sufficient voltage to the PG to determine the conduction mode. If V_{PG} is too low, it causes the opposite type of carriers to be much easier to pass through and generate a leakage current. The forward current can be improved by increasing V_{PG}. However, an excessively large V_{PG} causes an increase in the potential difference between the PG and CG, thus increasing the leakage current. Therefore, the subthreshold characteristics degrade. By considering the influence of V_{PG} on the reverse, static and forward properties, the optimized value of V_{PG} is approximately 1 V in n-mode, while the optimized value of V_{PG} is approximately − 1 V in p-mode.

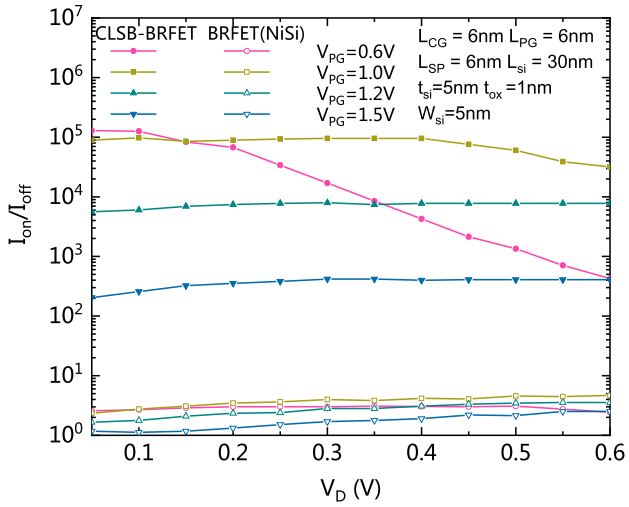
Figure 9a shows the output characteristics of the proposed CLSB-BRFET with different V_{CG} in n-mode. Figure 9b shows the output characteristics of the proposed CLSB-BRFET with different V_{CG} in p-mode. The forward-on-state saturation current is strictly restricted by V_{CG}. Thereafter, the proposed CLSB-BRFET has a good inhibition effect on the early effect. The output characteristic enters from the linear region into the saturation region as V_{DS} increases. The drain saturation current increases with increasing gate voltage.

Figure 10 shows the transfer characteristics of the proposed CLSB-BRFET with different L_{CG} and L_{PG}. The change in L_{CG} and L_{PG} has no obvious effect on the transfer characteristics unless L_{CG} and L_{PG} are reduced to 3 nm. This is similar to the short channel effect of conventional MOS devices. When L_{CG} and L_{PG} are changed, the curve translates slightly.

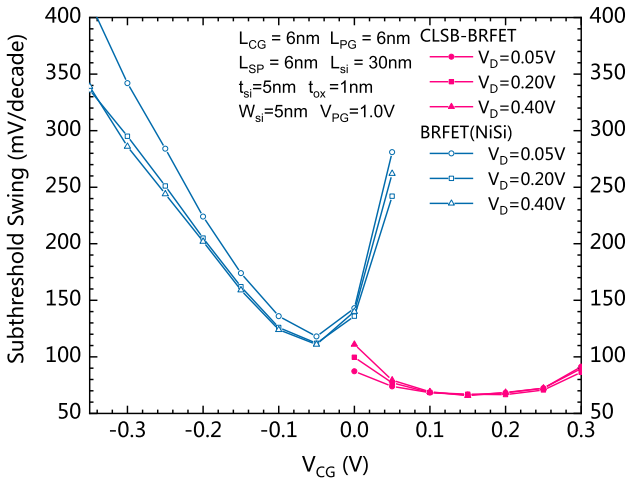
Figure 11 shows the reconfigurable characteristics of the CLSB-BRFET. V_{PG} determines the conduction mode. When the PG, the CG and the drain electrode are all positively biased, electrons flow from the ErSi source into the conduction band to form the forward current. The proposed CLSB-BRFET operates in the turn-on state of the n-mode. Similarly, when the PG, CG and the drain electrode are all negatively biased, the holes flow from the PtSi source into the valence band to form the forward current. The proposed CLSB-BRFET operates in the turn-on state of the p-mode. If V_D is increased in both modes, the forward on-state current is increased. Moreover, the reverse leakage current is also increased slightly. In both modes, the I_{on}/I_{off} ratio is approximately 10^5.

Conclusions

In this work, a complementary low-Schottky-barrier source/drain (S/D)-based nanoscale dopingless bidirectional RFET (CLSB-BRFET) is proposed. Two different metal materials are adopted to form two different types of Schottky barriers on the interface between the S/D and silicon. Both a low Schottky barrier for the conduction band and a low



(a)



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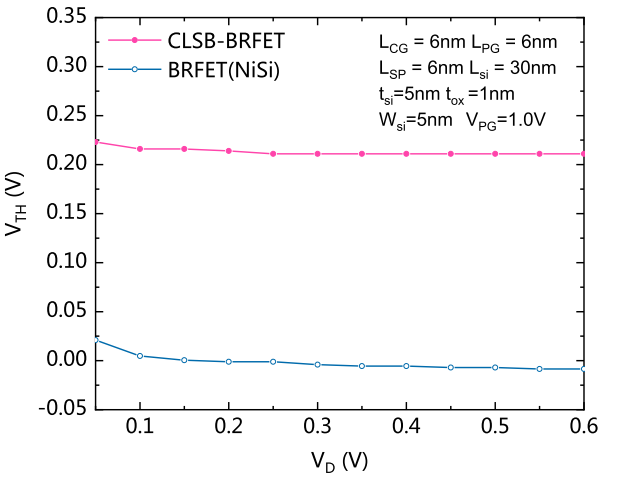

(c)

Fig. 7 **a** Comparison of the I_{on}/I_{off} current ratio between the proposed CLSB-BRFET and the conventional BRFETs. **b** Comparison of the subthreshold swing between the proposed CLSB-BRFET and the conventional BRFETs. **c** Comparison of the threshold voltage between the proposed CLSB-BRFET and the conventional BRFET (NiSi)

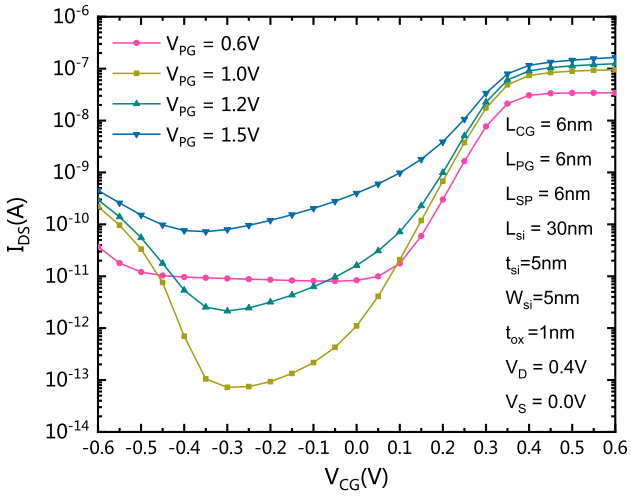

Fig. 8 **a** Comparison of the transfer characteristics of the CLSB-BRFET with different V_{PG} in n-mode. **b** Comparison of the transfer characteristics of the CLSB-BRFET with different V_{PG} in p-mode

Schottky barrier for the valence band are formed simultaneously. Therefore, more carriers from the source electrode can easily flow into the semiconductor region through thermionic emission compared to the conventional BRFET, which generates carriers through the band-to-band tunneling (BTBT) effect. A higher forward conduction current, sharper subthreshold slope and larger I_{on}/I_{off} ratio are achieved compared to conventional BRFET operation. If V_{PG} is appropriately selected and large enough, V_D does not affect the I_{on}/I_{off} ratio. The average SS of the proposed CLSB-BRFET is approximately 100 mV/dec, while the minimum SS of the NBRFET with NiSi S/D electrodes is larger than 100 mV/dec. The optimized value of V_{PG} is approximately 1 V in n-mode, while the optimized value of V_{PG} is approximately − 1 V in p-mode. The change in L_{CG} and L_{PG} has no obvious effect on the transfer characteristics unless L_{CG} and L_{PG} are reduced to 3 nm. V_{PG} determines the conduction mode of the proposed CLSB-BRFET. When the PG, the CG and the drain electrode are all positively biased, electrons flow from the ErSi source into the conduction band to form the forward current. The proposed CLSB-BRFET operates in the turn-on state of the n-mode. Similarly, when the PG, CG and the drain electrode are all negatively biased, the holes flow from the PtSi source into the valence band to form the forward current. The proposed CLSB-BRFET operates in the turn-on state of the p-mode. In both modes, the proposed CLSB-BRFET has good on-state conduction characteristics and low static power consumption, and the I_{on}/I_{off} ratio in both n-mode and p-mode reaches approximately 10^5.

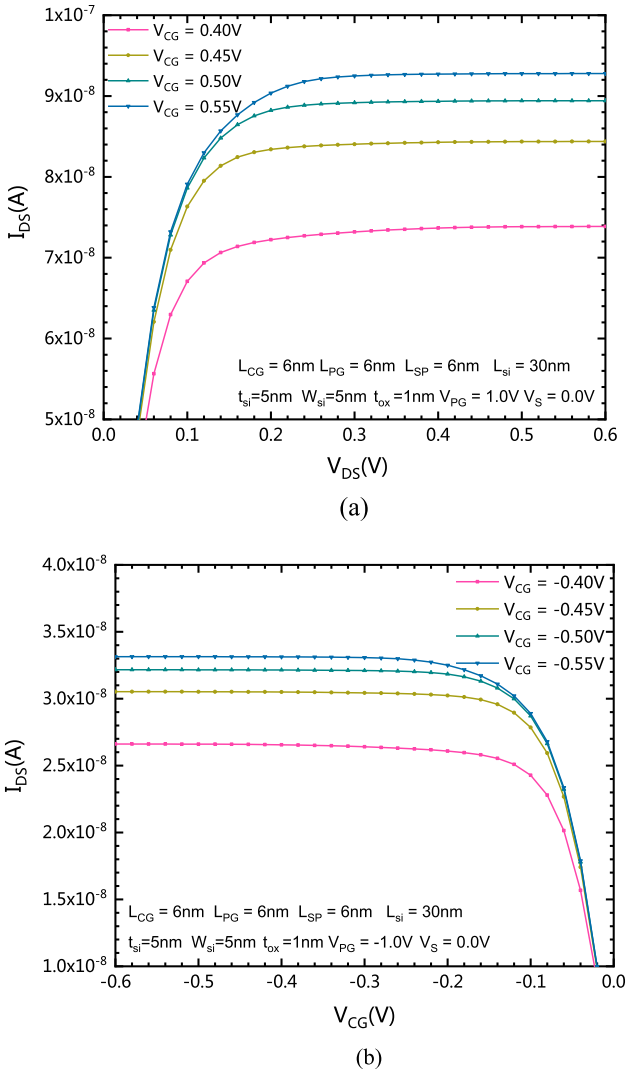

Fig. 9 **a** The output characteristics of the proposed CLSB-BRFET with different V_{CG} in n-mode. **b** The output characteristics of the proposed CLSB-BRFET with different V_{CG} in p-mode

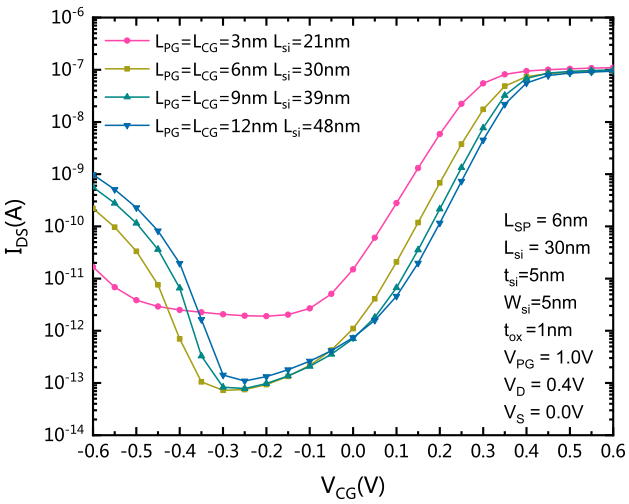

Fig. 10 The transfer characteristics of the proposed CLSB-BRFET with different L_{CG} and L_{PG} values

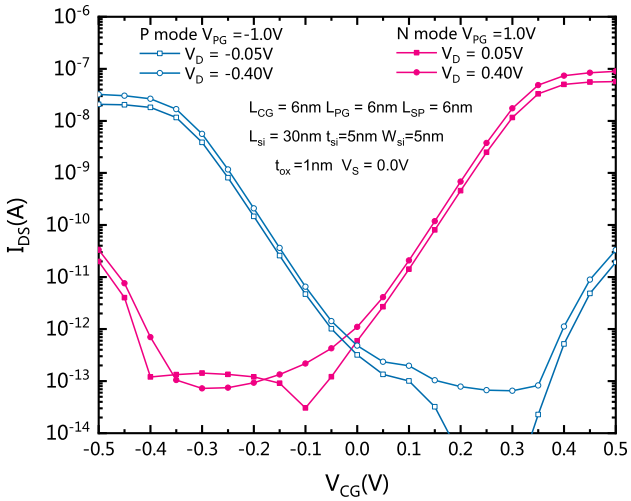

Fig. 11 Reconfigurable characteristics of the proposed CLSB-BRFET

Author contributions XJ: Manuscript writing and theoretical guidance. SZ: Simulation and data analysis. CZ: data analysis and figure editing. ML: data analysis and figure editing. XL: Data analysis, sorting and figure editing. All authors read and approved the final manuscript.

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Data availability All available data and material are original work. All data have been clearly provided in the manuscript without additional data and supporting materials. The datasets used and/or analyzed during the current study are also available from the corresponding author on reasonable request.

Code availability Source code is available upon request from the corresponding author.

Declarations

Competing interests The authors declare that they have no competing interests.

References

1. Heinzig A, Slesazeck S, Kreupl F, Mikolajick T, Weber WM. Reconfigurable silicon nanowire transistors. Nano Lett. 2012;12:119–24.
2. Sun B, Richstein B, Liebisch P, Frahm T, Scholz S, Trommer J, Mikolajick T, Knoch J. On the operation-modes of dual-gate reconfigurable nanowire transistors. IEEE Trans Electron Devices. 2021;68:3684–9.
3. Zhang J, Tang X, Gaillardon PE, De Micheli G. Configurable circuits featuring dual-threshold-voltage design with three-independentgate silicon nanowire FETs. IEEE Trans Circ Syst I Regular Pap. 2014;61:2851–61.
4. Weber WM, Heinzig A, Trommer J, Grube M, Kreupl F, Mikolajick T. Reconfigurable nanowire electronics-enabling a single CMOS circuit technology. IEEE Trans Nanotechnol. 2014;13:1020–8.
5. Mikolajick T, Heinzig A, Trommer J, Baldauf T, Weber WM. The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. Semicond Sci Technol. 2017;32: 043001.
6. Rai S, Trommer J, Raitza M, Mikolajick T, Weber WM, Kumar A. Designing efficient circuits based on runtime-reconfigurable field-effect transistors. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2019;27:560–72.
7. Galderisi G, Mikolajick T, Trommer J. Reconfigurable field effect transistors design solutions for delay-invariant logic gates. IEEE Embed Syst Lett. 2022;14:107–10.
8. Hauenstein RJ, Schlesinger TE, McGill TC. Schottky barrier height measurements of epitaxial NiSi2 on Si. Appl Phys Lett. 1985;47:853.

9. Bashir F, Alharbi AG, Loan SA. Electrostatically doped DSL high Schottky barrier MOSFET on SOI for low power applications. IEEE J Electron Devices Soc. 2017;6:19–25.
10. Bashir F, Loan SA, Rafat M, Alamoud A, Abbasi SA. A high-performance source engineered charge plasma-based Schottky MOSFET on SOI. IEEE Trans Electron Devices. 2015;62(10):3357–64.
11. Kale S, Kondekar PN. Design and investigation of double gate high Schottky barrier MOSFET using gate engineering. Micro Nano Lett. 2015;10(12):707–11.
12. Jun M, Kim Y, Choi C, Kim T, Oh S, Jang M. Schottky barrier heights of n/p-type erbium-silicided schottky diodes. Microelectron Eng. 2008;85:1395–8.
13. Calvet LE, Luebben H, Reed MA, Wang C, Snyder JP, Tucker JR. Subthreshold and scaling of PtSi Schottky barrier MOSFETs. Superlattices Microstruct. 2000;28:501–6.
14. Chin VWL, Storey JWV, Green MA. P-type PtSi Schottky-diode barrier height determined from I–V measurement. Solid-State Electron. 1989;32:475–8.
15. https://www.silvaco.com/products/tcad/device_simulation/device_simulation.html.