Nanoscale Research Letters

NANO EXPRESS

Open Access

Wide range detector of plasma induced charging effect for advanced CMOS BEOL processes

Yi-Jie Chao, Kai-Wei Yang, Chi Su, Chrong-Jung Lin and Ya-Chin King*

Abstract

This work proposed a modified plasma induced charging (PID) detector to widen the detection range, for monitoring the possible plasma damage across a wafer during advanced CMOS BEOL processes. New antenna designs for plasma induced damage patterns with extended capacitors are investigated. By adapting the novel PID detectors, the maximum charging levels of the detectors have been enhanced.

Keywords: Plasma induced damage, Advanced FinFET technology, Detection range

Introduction

In recent years, the evolution of semiconductor process technology continues to scale down the critical dimension in large-scale integrated circuits [1–3]. Advanced FinFET logic processes have become more complex for realizing more tightly packed transistors in multi-functional and more powerful Si chips. Reactive ion etching steps enhanced by plasma [4, 5] become inevitable in advanced nano-scale processes for achieving high aspect ratio structures which are essential for high packing density circuits [6]. For CMOS technology nodes beyond 45 nm, the transistor gates changed from the conventional poly-silicon gate with silicon dioxide to high-k metal gate stacks [7, 8]. This change makes the devices more susceptible to the plasma induced damage and might lead to unforeseen latent damages to the high-k dielectric layers. [9]. In state-of-art manufacturing processes of FinFETs, numerous RF plasma steps such as etching, deposition and cleaning processes are inevitable, which create higher frequencies of plasma induced charging events [10]. Both positive and negative charging on metal structures may occur. As these charges flow through the conductive paths made of pre-existing metal lines, via and contacts, the undesirable discharging through vulnerable parts of the circuits, particularly through the transistor gate dielectric may lead to significant reliability concerns. For instance, in the dry etching step, scattering impinging ions and sputtered materials at the reaction surface cause more defects in the bulk fins [11, 12]. To avoid the plasma charging event leading to irreversible damage to circuits, design rules that limit the size of metal structures are given. Another example of alleviating PID includes using protective diodes, which could shunt the plasma charging current away from sensitive circuits [13]. The introduction of In-Situ Steam Generation (ISSG) gate oxide reported improving its tolerance for plasma damage [14]. Furthermore, trimming the chamber and modifying PECVD-Ti deposition process were also found to alleviated plasma induced damage [15]. Most of these methods however result in undesirable limitations on circuit design flexibility or processing tradeoffs.

Conventionally, on-wafer test patterns have been used to monitor the plasma induced damage (PID) levels [16]. The most common and widely used parameter for monitoring on-wafer PID is the time-to-breakdown (TDDB) characteristics of the transistor gates with large antenna structures. The latent damage on gate dielectrics can be

*Correspondence: ycking@ee.nthu.edu.tw
Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan

revealed by measuring the degradation of the gate dielectric layer under voltage or current stress tests. Hence, these patterns are not able to provide real-time feedback on the plasma processes [17]. In our previous works, an on-wafer plasma induced charging effect detector is demonstrated in advanced FinFET technologies. The PID detector uses capacitive coupling structure to induce a response on the floating gate [18–20]. Therefore, there is no damage to the gate dielectric layer as it does in a conventional PID detector. On these new detectors, one measures the shifting I–V curves to find out both the intensity, duration as well as polarity of charges on the antenna gate. It is found that these detectors may subject to saturation effect as the plasma intensity at certain recording sites exceeds critical levels. To extend the dynamic range of the PID detector, new antenna gate designs have been investigated in this work, where widening of the sensing ranges is successfully demonstrated.

Methods

The 3D schematic of plasma induced damage (PID) detector with a parasitic capacitor connected to the antenna node is shown in Fig. 1a. Differing from PID monitoring structure, this detector utilizes a long contact slot to couple the antenna voltage on the floating gate. The cross-sectional TEM photograph is shown in Fig. 1b. As shown in the figure, contact slots which collect charges are capacitively coupled to floating gate.

Figure 2 compares the recorded threshold voltage distributions from these detectors across a 12-inches wafer. The negative threshold voltage shift indicates that negative charges were collected on the antenna, drawing positive charges into floating gate, resulting in negative threshold voltage shifts. It is found that as the antenna area increases, the rising total capacitance leads to lowering of the overall antenna voltages, hence, smaller the shift in V_t.

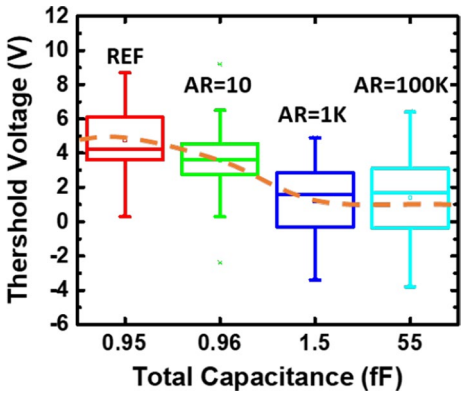


Fig. 2 Threshold voltage range of samples with different size of antenna, and the corresponding total capacitance on the antenna

Here, in Fig. 3a, the flow chart explaining the basic operation principles of the PID detector is outlined. As the plasma charge (Q_{Ant}) are collected on the antenna, the potential of the antenna gate, V_{Ant}, varies. V_{Ant} is then coupled to the floating gate (FG), promoting the tunneling of electrons either into or out of FG. After plasma processes, V_t of these detectors may become more negative or more positive based on the polarity of Q_{Ant}. V_t can be calculated by the FN tunneling current model with the parameter listed in Fig. 3b.

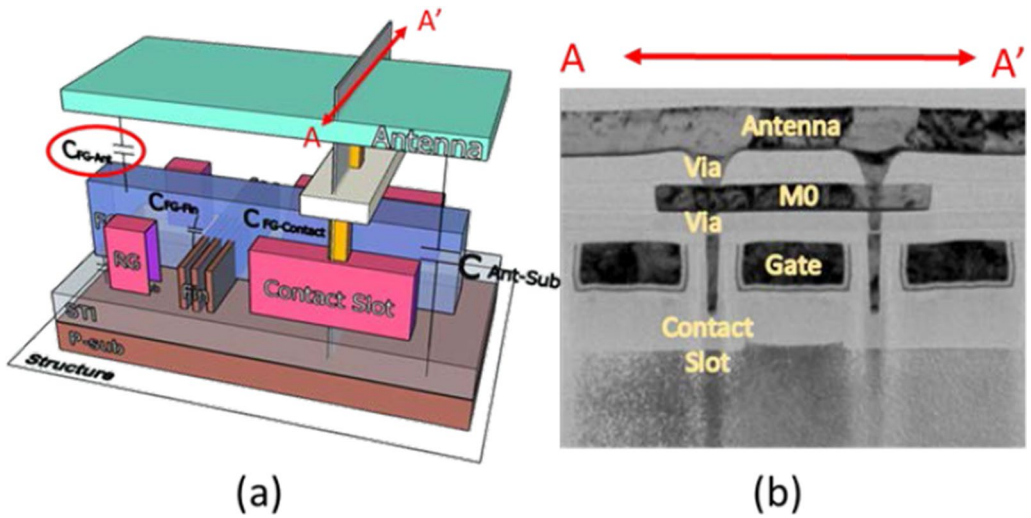
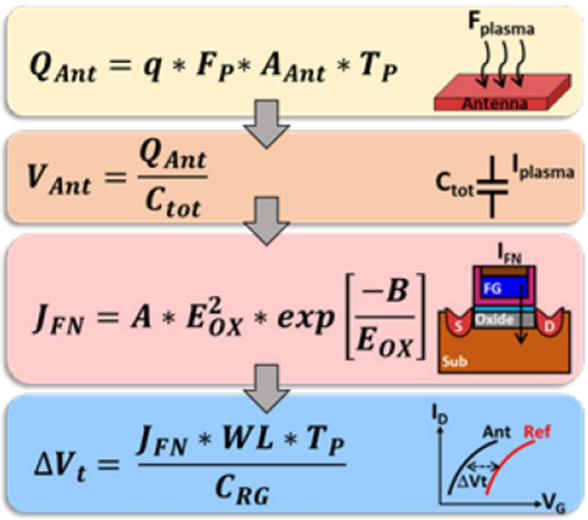


Fig. 1 **a** The 3D illustrations of previously reported in-situ PID detector and the antenna capacitor is highlighting in this structure. **b** The TEM photo of PID detector, where the gate length of this detector is 140 nm



(a)

Parm	Description	Unit	Parm	Description	Unit
Q_{Ant}	Charges on the antenna	Coul	E_{OX}	Electric field of oxide layer	V/cm
F_P	Plasma flux	A/cm²	V_{FB}	Flat Band voltage	V
A_{Ant}	Antenna area	cm²	τ_{OX}	Oxide thickness	cm
T_P	Plasma process time	sec	J_{FN}	FN tunneling flux	A/cm²
V_{Ant}	Antenna voltage	V	ΔVt	Threshold voltage variation	V
V_{FG}	Floating Gate voltage	V	WL	Oxide effective area	cm²
$\propto_{Ant}$	Coupling ratio of antenna		C_{RG}	Capacitance of Read Gate	

(b)

Fig. 3 **a** The flow chart from plasma charges (Q_{Ant}) collected on the antenna to shift V_t. Based on the FN tunneling model, ΔV_t can be calculated. **b** The list of parameters with its definitions

Figure 4 illustrates all the possible capacitance on the FG-based PID detector. From Fig. 5, it is found that as the antenna area increases, ΔV_t tends to saturate. As V_{Ant} reaches the maximum levels, Q_{Ant} starts to leak out when the voltage level is too high. To avoid the plasma flux level exceeding the detector limitation, the antenna capacitance is deliberately increased by adding loading capacitors which could reduce the proportion of antenna capacitance in the total capacitance.

Figure 6a shows the 2D structure of the previously reported in-situ PID detector, and three structures of realizing additional capacitors are presented. They are MOM capacitors, which use the larger overlap area of metal layers to increase the total capacitance in Fig. 6b, STI capacitors, which increase the capacitance by

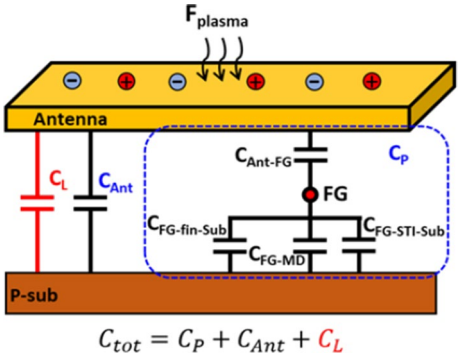


Fig. 4 Composition of capacitance on the antenna structure with the additional loading capacitor, which is designed to modify the sensitivity of the PID detectors. Where C_P is the overall parasitic capacitance on the floating gate

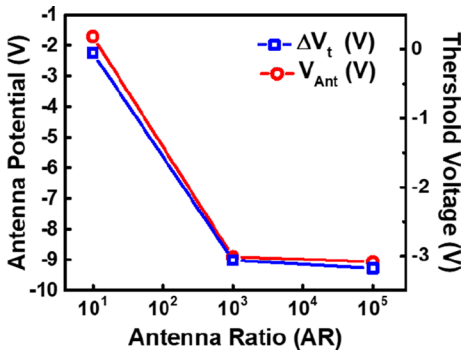


Fig. 5 Both the threshold voltage level as well as projected antenna voltage level saturates on patterns with increased antenna area

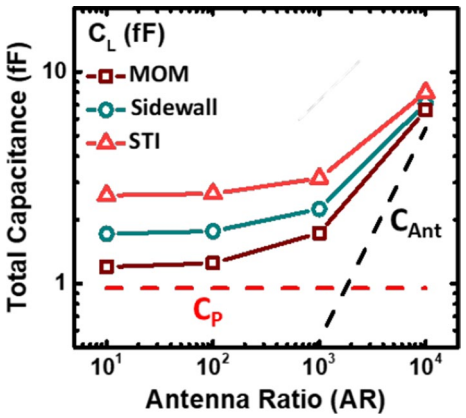


Fig. 7 Comparison of total capacitance versus antenna ratios as the three types of loading capacitors are added

adjusting the length of the metal gate in Fig. 6c, and sidewall capacitors, which use the overlap area of metal gate and contact to form additional capacitor Fig. 6d.

Experimental results and discussion

Figure 7 compares the total capacitance versus antenna ratios when different types of loading capacitors are added. The total capacitance is dominated by the antenna capacitance when the antenna ratio is greater than 1 K.

When the added loading capacitance become comparable to the antenna capacitance, total capacitance could then be affected by the loading capacitors. Since the maximum amount of charges collected by the antenna is fixed; by increasing total capacitance, ΔV is expected decreased, according to $\Delta Q = C\Delta V$. Thus, the sensitivity of the detection range could be suppressed, preventing saturation effect when plasma charging level exceed its original limits. Drain current characteristics for devices of AR = 10 with different STI capacitors are compared in Fig. 8. When a larger loading capacitor is added, the percentage of antenna capacitance in total capacitance is reduced. Under the same plasma charging flux, the total plasma charges after a period is proportional to the antenna area. Hence, when overall capacitance increases, V_{Ant} is expected to be lowered, allowing for the detection of high plasma flux levels. As shown in Fig. 8, smaller shifts are found on the I–V curves for the samples with additional loading capacitors.

Box charts of the threshold voltages measured from samples with AR = 1 K and different sizes of MOM, STI, and Sidewall capacitors are compared in Fig. 9 When the loading capacitance is increased, less threshold voltage shift is observed on average. In the experimental design, C_{L} by STI structure is too small to show impact of

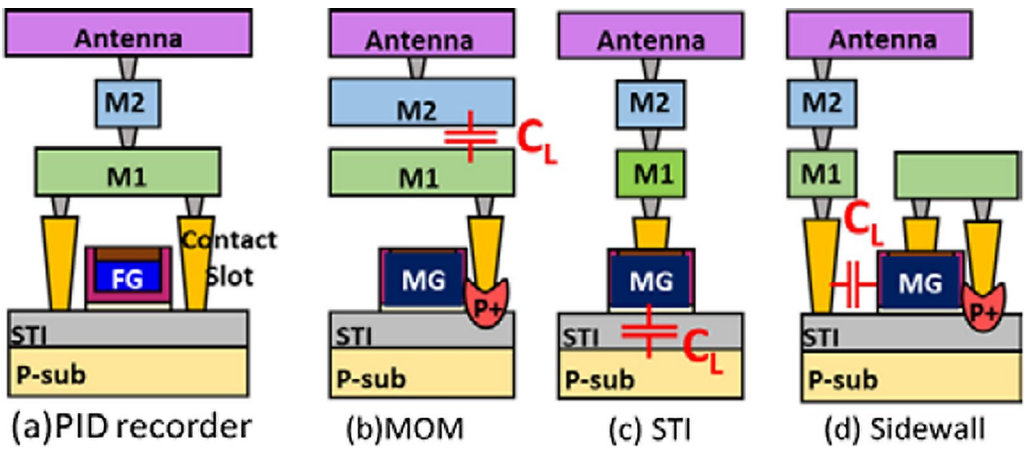


Fig. 6 Cross sectional illustration of **a** the in-situ PID detector, and those with a loading additional capacitor realized by **b** MOM, **c** STI, and **d** sidewall, respectively

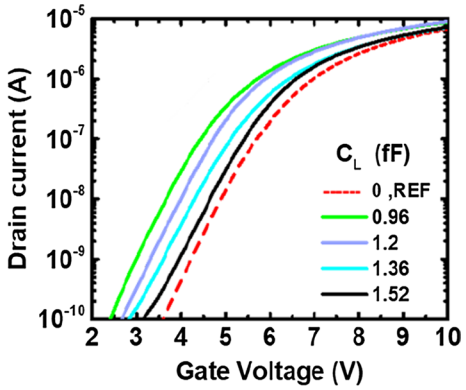


Fig. 8 I–V curve of different sizes of STI capacitor with AR = 10. When the external capacitance is larger, the I–V curve is closer to that of the reference cells

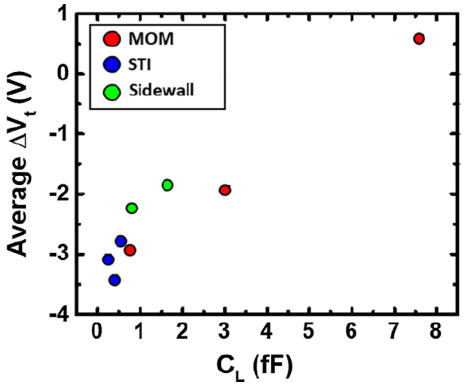


Fig. 10 Comparison of the average ΔV_t versus C_L implemented by the three types of capacitor structures, where ΔV_t is defined as the V_t difference between a detector cell and the reference cell. Data suggest that reduced sensitivity can be obtained as C_L increased

the charging level. Comparison in Fig. 10 suggested that three ways of adding loading capacitors can also effectively reduce the average response to plasma charging. The additional loading capacitor can successfully expand the detection range of the PID detector, while the sensitivity of the detectors is reduced. For achieving wide-range detection of plasma charging level, a series of PID detectors with different level of C_L can be designed in a 1-D array for detecting plasma charging levels on both the high and low end.

Conclusions

This study investigates a new antenna gate design to extend the sensing range of plasma induced charging levels on the PID monitoring detectors. By adding a loading capacitor, high antenna gate voltage subject to charge leak can be prevented, allowing for a higher level of charging level to be registered on the PID detectors. This novel design effectively widens the detection range of plasma charging levels in advanced CMOS BEOL processes.

Abbreviations

PID: Plasma induced damage; V_t: Threshold voltage; Q_{Ant}: Charges on the antenna; V_{Ant}: Antenna voltage; MOM: Metal-oxide-metal; AR: Antenna ratio; C_L: Loading capacitance; C_P: Parasitic capacitance; C_{Ant}: Antenna capacitance.

Acknowledgements

The authors would like to thank the support from the Ministry of Science and Technology (MOST), Taiwan, and Taiwan Semiconductor Manufacturing Company (TSMC).

Authors' contributions

Equal contributions for all authors and discussed the results. All authors read and approved the final manuscript.

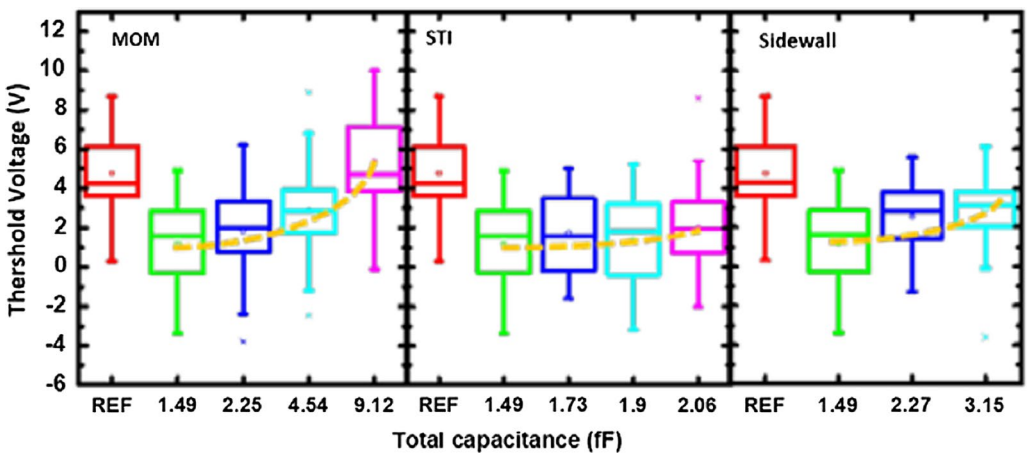


Fig. 9 Threshold voltages measured on samples with different sizes of MOM, STI and Sidewall capacitors are compared. All devices have the same AR of 1 K

Funding
This study is supported by the Ministry of Science and Technology (MOST) and the Taiwan Semiconductor Manufacturing Company (TSMC) and the internal funding from NTHU. (Project Number: MOST 109-2622-8-007-022).

Availability of data and material
Not Applicable.

Declarations

Competing interests
The authors declare that they have no competing interests.

Received: 7 December 2020 Accepted: 25 June 2021
Published online: 03 July 2021

References

1. Narasimham B et al (2018) Scaling trends and bias dependence of the soft error rate of 16 nm and 7 nm FinFET SRAMs. In: IEEE IRPS, Burlingame, CA, pp 4C.1-1–4C.1-4
2. Liu SE et al (2016) Aging of I/O overdrive circuit in FinFET technology and strategy for design optimization. In: IEEE IRPS, Pasadena, CA, USA, pp CR-3-1–CR-3-4
3. Fasarakis N, Tassis DH, Tsormpatzoglou A, Papathanasiou K, Dimitriadis CA, Ghibaudo G (2013) Compact modeling of nano-scale trapezoidal cross-sectional FinFETs. In: ISCDG, Dresden, Germany, pp 1–4
4. Roh HJ et al (2019) Development of the virtual metrology for the nitride thickness in multi-layer plasma-enhanced chemical vapor deposition using plasma-information variables. IEEE TSM 31(2):232–241
5. Zongjie H et al (2014) Plasma cleaning and its application in microwave module wire bonding technology. In: IEEE ICEPT, Chengdu, pp. 360–362
6. Dowling KM et al (2017) Profile evolution of high aspect ratio silicon carbide trenches by inductive coupled plasma etching. In: IEEE, pp 135–142
7. Oates AS (201) Reliability issues for high-k gate dielectrics. In: IEEE IEDM, Washington, pp 38.2.1–38.2.4
8. Okada K, Ota H, Nabatame T, Toriumi A (2007) Dielectric breakdown in high-K gate dielectrics—mechanism and lifetime assessment. In: IEEE IRPSP 45th annual, Phoenix, pp 36–43
9. Chu PK et al (2008) Fabrication of silicon-on-insulator (SOI) and high-k materials using plasma technology. In: IEEE, pp 757–760
10. Ackaert J et al (2000) Prevention of plasma induced damage on thin gate oxide of HDP oxide deposition, metal etch, Ar preclean processing in BEOL subhalf micron CMOS processing. In: IEEE, Santa Clara, CA, USA, pp 77–80
11. Eriguchi K et al (2008) Threshold voltage shift instability induced by plasma charging damage in MOSFETs with high-k dielectric. In: IEEE, pp 97–100
12. Hiblot G, Van der Plas G (2018) Factor analysis of plasma-induced damage in bulk FinFET technology. IEEE EDL 39(7):927–930
13. Wallash A et al (1999) A study of diode protection for giant magnetoresistive recording heads. In: IEEE, pp 385–390
14. Cellere G et al (2003) Plasma damage reduction by using ISSG gate oxides. In: IEEE, pp 65–68
15. Park HS et al (2003) Plasma-induced damage on sub-5 nm gate oxide by PECVD-Ti process. In: IEEE, pp 24–27
16. Cibrario G et al (2014) A high-level design rule library addressing CMOS and heterogeneous technologies, In: IEEE, pp 1–4
17. Kaganovich ID, Raitses Y, Khrabrov AV, Demidov VI, Sydorenko D (2010) Nonlocal collisionless and collisional electron transport in low temperature plasmas. In: IEEE, pp 1–1
18. Wu C et al (2015) Mapping of wafer-level plasma induced charge contour by novel on-chip in-situ recorders in advance FinFET technologies. In: IEDM, pp 7.1.1–7.1.4
19. Tsai Y et al (2016) Wafer-level mapping of plasma-induced charging effect by on-chip in situ recorders in FinFET technologies. In: IEEE, pp 2497–2502
20. Tsai Y et al (2018) 7nm FinFET plasma charge recording device. In: IEDM, pp 17.5.1–17.5.4

Publisher's Note