Nanoscale Research Letters

NANO EXPRESS Open Access

Selective Growth of WSe_2 with Graphene Contacts

Yu-Ting Lin[1], Xin-Quan Zhang[2], Po-Han Chen[2], Chong-Chi Chi[2], Erh-Chen Lin[2], Jian-Guo Rong[2], Chuenhou Ouyang[2], Yung-Fu Chen[1*] and Yi-Hsien Lee[2*]

Abstract

Nanoelectronics of two-dimensional (2D) materials and related applications are hindered with critical contact issues with the semiconducting monolayers. To solve these issues, a fundamental challenge is selective and controllable fabrication of p-type or ambipolar transistors with a low Schottky barrier. Most p-type transistors are demonstrated with tungsten selenides (WSe_2) but a high growth temperature is required. Here, we utilize seeding promoter and low pressure CVD process to enhance sequential WSe_2 growth with a reduced growth temperature of 800 °C for reduced compositional fluctuations and high hetero-interface quality. Growth behavior of the sequential WSe_2 growth at the edge of patterned graphene is discussed. With optimized growth conditions, high-quality interface of the laterally stitched WSe_2-graphene is achieved and characterized with transmission electron microscopy (TEM). Device fabrication and electronic performances of the laterally stitched WSe_2-graphene are presented.

Keywords: Contacts, WSe_2, Electronics, Heterostructures, Interfaces

Introduction

Monolayer van der Waals materials, such as graphene and transition metal dichalcogenide (TMD), exhibit excellent electronic performances and atomically thick body without dangling bonds on the surface, which offers potential solutions for fundamental limit of channel materials in Moore's law, such as short channel effects and various challenges in the scaling [1, 2]. In the past decade, nanoelectronics of two-dimensional (2D) materials and related applications are highly hindered by critical contact issues with the semiconducting TMD monolayers due to significant Fermi level pinning effect from the defects involved in the synthetic, fabrication, and integration processes [3–6]. Considerable efforts, including phase engineering of the channel materials (from semiconducting 1H phase to conductive 1T phase) [7], geometry of contacts [8–11], and interface engineering with graphene buffer layer [12, 13], are carried out for essential electronic performances with improved contact properties.

Recently, integration of conductive graphene and semiconducting TMD for improved contacts and novel properties is realized by direct growth of TMD using chemical vapor deposition at the edge of artificially patterned graphene [14–21]. Heterojunctions among different 2D materials enable essential multifunctionality of the monolayer channels for broader capacity and integration [22–27]. Weak tunneling barrier is achieved at the heterojunction of the laterally stitched MoS_2-graphene, enabling inverter and negative-AND (NAND) gates for a complete set of logic circuits based on 2D materials [16, 17]. The next essential goal is to realize basic electronic units of complementary metal-oxide semiconductor (CMOS) inverters and other logic circuits with scalable 2D materials. Towards this goal, however, it remains a long-lasting challenge on selective and controllable fabrication of p-type or ambipolar transistors with a low Schottky barrier [28]. Most p-type transistors are demonstrated with tungsten selenides (WSe_2) but a high temperature is required for the WSe_2 growth because of a higher evaporation temperature of the WO_3 precursor [29–31]. A low temperature synthesis of the sequential monolayer growth at the pre-patterned 2D materials is mainly achieved with Mo-based TMD.

* Correspondence: yfuchen@cc.ncu.edu.tw; yhlee.mse@mx.nthu.edu.tw
[1]Department of Physics, National Central University, Zhongli, Taoyuan 32001, Taiwan
[2]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

Springer Open

© The Author(s). 2020 **Open Access** This article is distributed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made.

Here, we utilize seeding promoter and low pressure CVD process to enhance sequential WSe_2 growth with a reduced growth temperature for reduced compositional fluctuations and high hetero-interface quality [32, 33]. Growth behavior of the sequential WSe_2 growth at the edge of patterned graphene is discussed. With optimized growth conditions, high-quality interface of the laterally stitched WSe_2-graphene is achieved and studied with TEM. Device fabrication and electronic performances of the laterally stitched WSe_2-graphene are presented.

Method/Experimental

Synthesis of WSe_2 and Graphene

Large-area WSe_2 films were synthesized on sapphire and SiO_2/Si substrates in the furnace. Before growth process, the substrates were cleaned with acetone, isopropanol, and then water for 10 min, respectively. Perylene-3,4,9, 10-tetracarboxylic acid tetrapotassium salt (PTAS) was uniformly coated on the substrate surface as seeding promoters to enhance the activity and growth rate of the monolayers. High purity solid precursors of WO_3 (Alfa Aesar, 99.9995% CAS#1313-27-5) and Se (Sigma-Aldrich, 99.5% CAS#7704-34-9) were placed in two ceramic crucibles, and the substrates were placed face up and next to the WO_3 powder. The WSe_2 samples were synthesized during 800~900 °C for 10 min with a heating rate of 30 °C min^{-1} and under a mixture of N_2/H_2 flow at 1.2 Torr. Graphene is synthesized on Cu foil at 1000 °C for 10 min with a heating rate of 30 °C min^{-1} and under a mixture of CH_4/H_2 flow at 4 Torr. The pattern graphene is carried out by e-beam lithography and oxygen plasma etching.

Device Fabrication

The graphene-WSe_2 devices were fabricated without sample transfer. E-beam lithography process was performed to define the electrodes on the patterned graphene layer. A thin metal layer of Pd (40 nm) was deposited using e-beam evaporation and a following lift-off process was carried out in acetone. Encapsulation layer and gate dielectric of the device are fabricated by using atomic layer deposition (ALD) of thin Al_2O_3 films (50 nm). A thin metal of Pd (40 nm) was deposited on the dielectric layer to use as the gate electrodes. To improve electronic performances, the devices are annealed at ~ 120 °C for ~ 12 h in a vacuum environment of ~ 10^{-5} Torr.

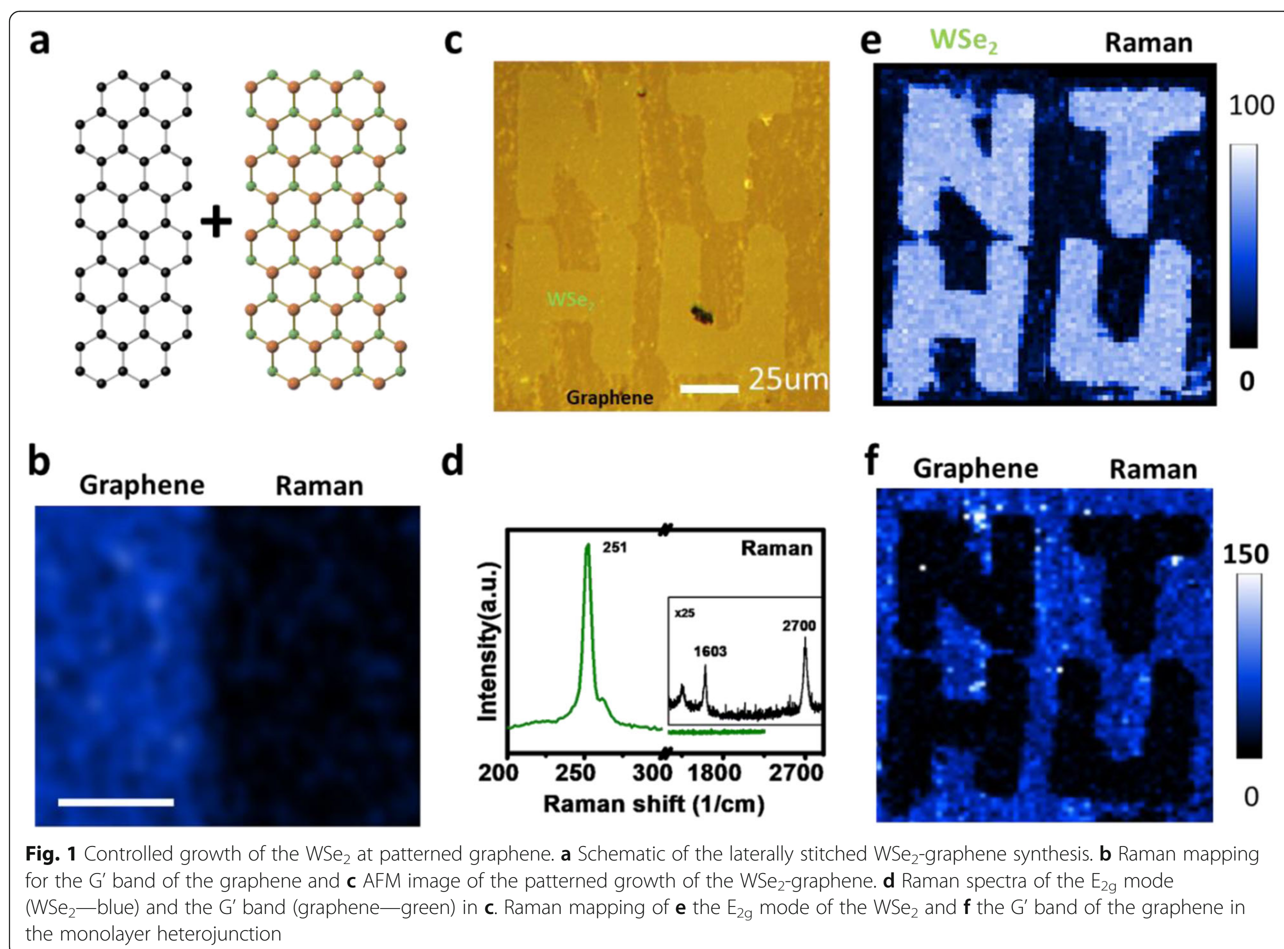

Fig. 1 Controlled growth of the WSe_2 at patterned graphene. **a** Schematic of the laterally stitched WSe_2-graphene synthesis. **b** Raman mapping for the G′ band of the graphene and **c** AFM image of the patterned growth of the WSe_2-graphene. **d** Raman spectra of the E_{2g} mode (WSe_2—blue) and the G′ band (graphene—green) in **c**. Raman mapping of **e** the E_{2g} mode of the WSe_2 and **f** the G′ band of the graphene in the monolayer heterojunction

Characterizations

Raman spectra and photoluminescence (PL) were obtained by commercial confocal Raman spectroscopy (Micro Raman/PL/TR-PL Spectrometer, Ramaker, Protrustech). Wavelength and spot size of the laser are 532 nm and 1–2 μm, respectively. Typical gratings were used with 300 g/mm for PL (low resolution) to get broadband spectrum and (high resolution) 1800 g/mm for Raman signals to get detail information of material. The TEM samples were prepared by using standard PMMA transfer technique to place the graphene-WSe_2 nanosheets onto the holey-carbon Cu grid. The TEM images were performed at an accelerate voltage of 80 kV (Cs-corrected STEM, JEOL, JEM-ARM200F). The electrical measurements were measured using an Agilent B1500a Semiconductor Device Analyzer.

Results and Discussion

To control the synthesis of the lateral heterojunction of graphene and WSe_2, sequential growth of the monolayer TMD at the graphene edges is demonstrated in Fig. 1a. Monolayer graphene is first grown on a copper foil and later transferred onto a fresh sapphire substrate by using standard PMMA-assisted transfer method. Conventional e-beam lithography and O_2 plasma etching processes are conducted to define the region for sequential growth of the monolayer WSe_2. Direct synthesis of monolayer WSe_2 at the edges of patterned graphene on sapphire substrate is achieved by low pressure CVD with PTAS as seeding promoters. More detailed information on the synthesis is described in the "Method/Experimental" section. In Fig. 1b, Raman mapping of the G' band in the laterally stitched graphene-WSe_2 displays a uniform contrast, which confirms a reduced damage of the pre-patterned graphene after the sequential CVD synthesis of the WSe_2 growth. In Fig. 1c, AFM image of the patterned growth of the graphene-WSe_2 indicates a smooth surface morphology of the monolayer heterojunction. Figure 1d presents the Raman spectra of the E_{2g} mode (WSe_2—blue) and the G' band (graphene—green) as the labels in Fig. 1c, which are consistent with the reported studies [34]. To illustrate uniformity of the as-grown heterojunction, Raman mapping of the patterned graphene-WSe_2 is shown in Fig. 1 e and f, respectively. A uniform contrast of the Raman intensity in the mapping images is clearly observed, suggesting controllable synthesis on heterogeneous growth of high-quality monolayer WSe_2 at the edges of the pre-patterned graphene.

To clarify growth behavior of the stitched graphene-TMD, the WSe_2 synthesis at the patterned graphene is

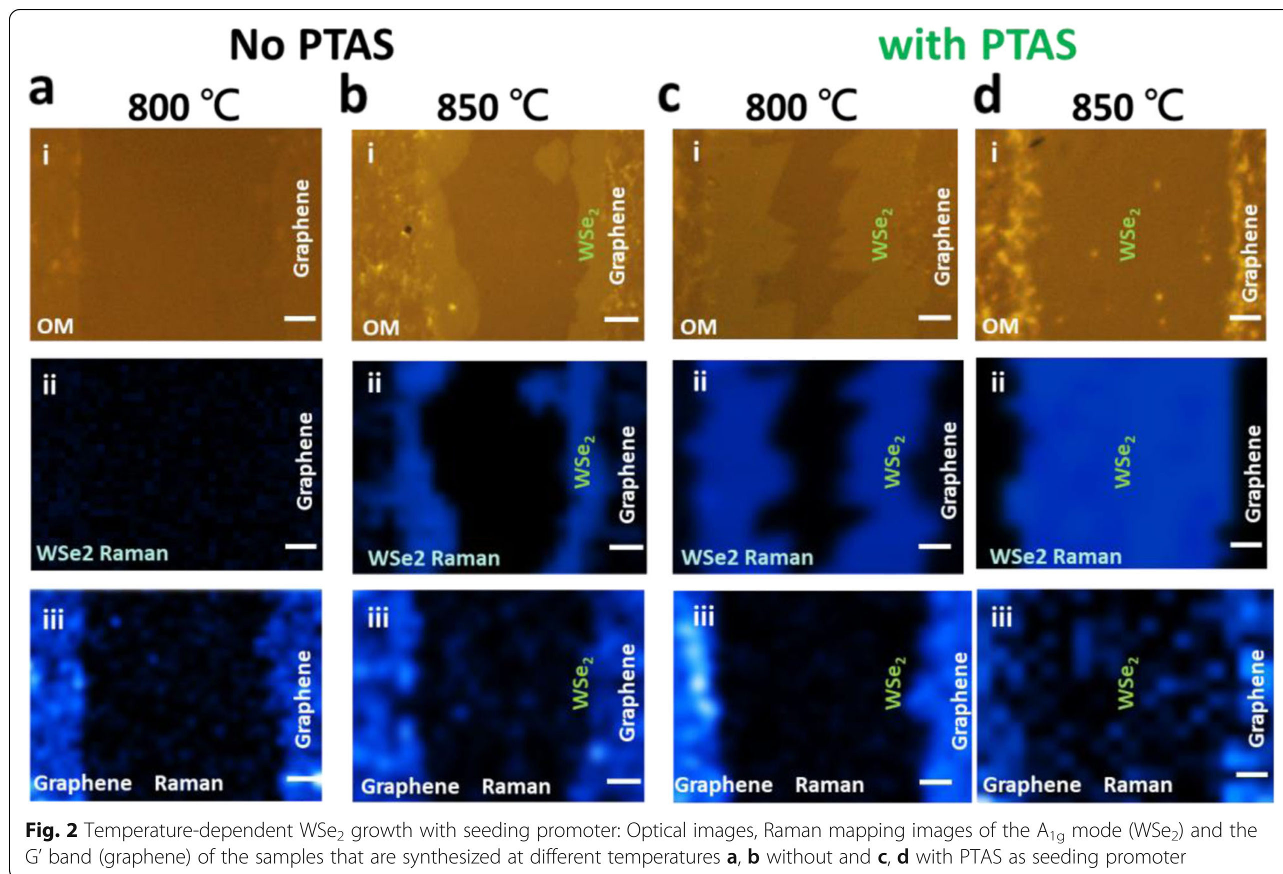

Fig. 2 Temperature-dependent WSe_2 growth with seeding promoter: Optical images, Raman mapping images of the A_{1g} mode (WSe_2) and the G' band (graphene) of the samples that are synthesized at different temperatures **a**, **b** without and **c**, **d** with PTAS as seeding promoter

carried out with and without promoters. Figure 2 a and b suggest the WSe_2 growth at different temperatures without PTAS as seeding promoter. Above 850 °C, the sequential growth of the WSe_2 appears at the graphene edges. A high growth temperature for WSe_2 growth is required due to reduced gaseous reactants for the solid precursor of the WO_3, as elaborated in previous papers [29–31]. A macroscopically smooth boundary of the as-grown WSe_2 implies random distributed and small size of grains. In contrast, the sequential WSe_2 growth at different temperatures with PTAS as seeding promoter is presented in Fig. 2 c and d. The PTAS promoters significantly reduce growth temperature for perfect sequential WSe_2 growth at the graphene edges with larger domain sizes, which is similar to the growth behavior in the TMD-TMD heterojunctions [22]. After the sequential WSe_2 growth at 800 °C, observation of a uniform contrast and higher intensity in Raman mapping of the G' band (graphene) indicates a reduced damage of the graphene because of the low temperature growth. With increased temperature, a continuous WSe_2 film fills in the patterned regions with ideal contact to the edges of the patterned graphene (Fig. 2d). Note that a larger domain size with a clear triangular shape of the monolayer WSe_2 stitched to the edges of the graphene (Fig. 2c), suggesting a better quality of the sequential WSe_2 growth. With optimized growth conditions on seeding promoters and temperature, scalable and high-quality monolayer WSe_2 is realized by the LPCVD system as presented in the supporting information (Additional file 1: Figure S1). It is noteworthy that the sequential TMD synthesis at the edges of patterned graphene is universally observed in other heterojunctions of different TMD and graphene as shown in the supporting information (Additional file 1: Figure S2).

To further investigate the heterojunction of the WSe_2-graphene, high-resolution transmission electron microscopy (HRTEM) measurement is performed. In Fig. 3a, selected area TEM image indicates that the overlap region between black (graphene end) and green (TMD end) dashed lines is composed of the pre-patterned graphene and the sequential grown WSe_2

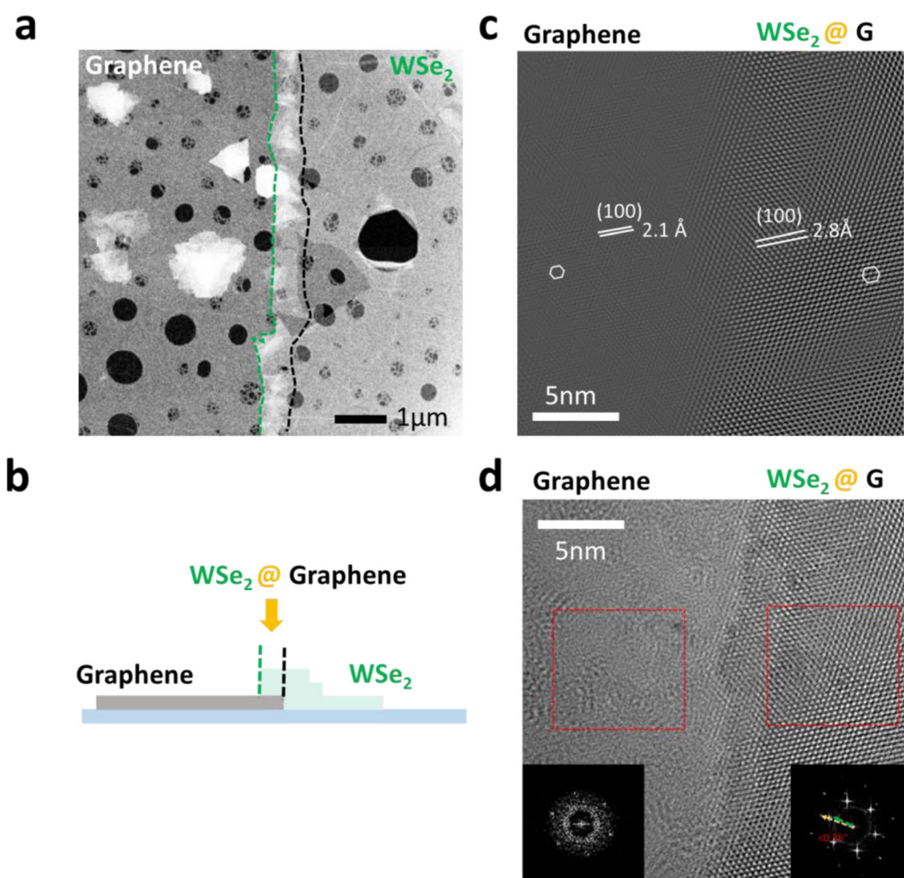

Fig. 3 TEM characterization of heterojunction of the laterally stitched graphene-WSe_2. **a** Low magnification image, **b** schematic illustrations, **c** simulated, and **d** observed HRTEM images of the heterojunction of the graphene-WSe_2. The right inset shows FFT image of the overlap region of the stacked WSe_2 on graphene, while the left inset displays that of the graphene. Raman mapping of **e** the E_{2g} mode of the WSe_2 and **f** the G' band of the graphene in the monolayer heterojunction

monolayer. Width of the overlapping region is about 500 nm. An amorphous-like TEM image for the graphene lattice is observed as expected because of unavoidable distortions of graphene with the energetic electron beam. Figure 3 c and d present the calculated and experimental observation on the HRTEM image for better understanding on the sequential TMD growth at the heterojunction. Observation of hexagonal lattices and unit cell of graphene (~ 2.5 Å) and WSe_2 (~ 3.3 Å) is consistent with the parameters in bulk lattices of graphene (2.46 Å) and WSe_2 (3.28 Å). The TEM characterizations indicate that the sequential WSe_2 growth initiates at the edges of the pre-patterned graphene because higher defect density at the graphene edge enhances the vertical island growth with more nucleation sites. A large lattice mismatch more than 20% between the lattice of graphene and TMD might be responsible for a disorder interface with higher defect density and for combined vertical and lateral TMD growth at the heterojunction. Moreover, the insets in Fig. 3d show the corresponding diffractograms by fast Fourier transform (FFT) of real space atomic images in the overlap region and graphene region. Only one set of diffraction pattern is observed at the graphene region (left), while two sets of diffraction patterns rotated with a twisting angle of 0.35° are observed at the overlapped region (right). A highly reduced twisting angle between graphene and WSe_2 lattices implies that the sequential growth of the WSe_2 favors coherent stacking at the graphene edges.

To demonstrate the field-effect properties of the as-grown WSe_2 stitched at the edges of patterned graphene hetero-device, the device is fabricated without sample transfer. Customized fabrication process based on surface functionality for e-beam lithography on an insulator is developed. Electronic transport performance of the stitched graphene-WSe_2 device is studied by connecting metal electrodes (Pd 40 nm) with the patterned graphene and depositing Al_2O_3 (50 nm) as gate dielectric. Figure 4 a and b show the schematic illustration of the top-gated heterojunction device and the optical image of the as-fabricated device, respectively. Two-terminal electronic transport measurements are carried out using commercial probe-station (Lake Shore Cryotronics PS-100 with Agilent B1500a) under vacuum at room temperature. The transfer curve of the device exhibits a p-type transport behavior with an on/off ratio (~ 10^4) and high on-current of approximately a few 100 nA (Fig. 4c). The field-effect mobility of the device in the linear region is around 0.07 cm^2/Vs at $V_d = 2$ V, which is evaluated using the following equation:

$$\mu = \frac{1}{C_{ox}} \frac{L}{W} \frac{\partial I_D}{\partial V_G} \frac{1}{V_D} \quad (1)$$

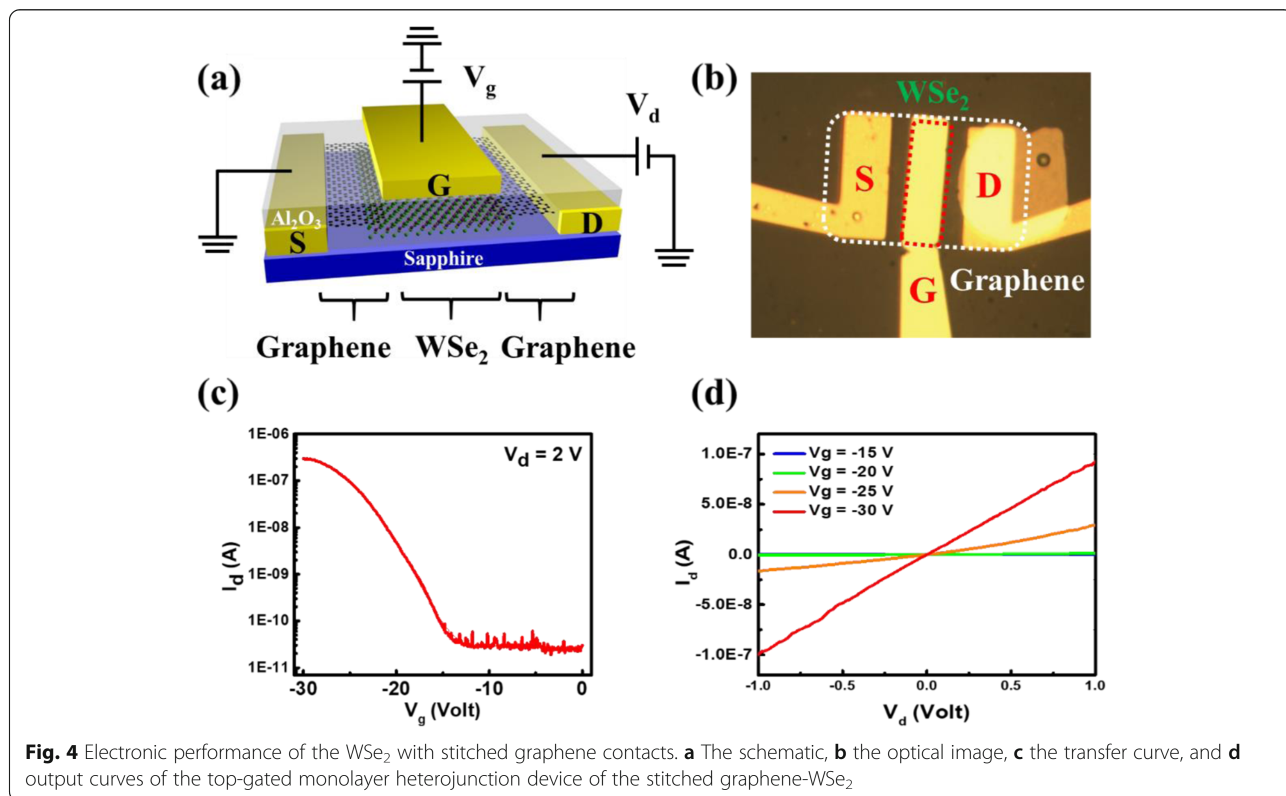

Fig. 4 Electronic performance of the WSe_2 with stitched graphene contacts. **a** The schematic, **b** the optical image, **c** the transfer curve, and **d** output curves of the top-gated monolayer heterojunction device of the stitched graphene-WSe_2

where $C_{ox} = \varepsilon_0\varepsilon_r/d$ is the oxide capacitance and L (9 μm) and W (24 μm) are the channel length and channel width, respectively. Moreover, the output curves of the device at various gate voltages are shown in Fig. 4d. The linear I-V curves confirm a good contact between graphene layer and WSe_2 layer. An enhanced electronic performance of the stitched TMD-graphene monolayer heterojunctions is achieved because of improved contact properties, suggesting the synthesis for sequential TMD growth at the edges of artificially patterned graphene moves a significant step towards 2D nanoelectronics.

Conclusions

Sequential WSe_2 growth at the edges of the patterned graphene is achieved on sapphire by using promoter-assisted LPCVD. The PTAS promoters significantly reduce growth temperature for ideal sequential WSe_2 growth at the graphene edges with larger domain sizes.

The TEM characterizations indicate that the sequential WSe_2 growth initiates at the edges of the pre-patterned graphene. A highly reduced twisting angle between graphene and WSe_2 lattices implies that the sequential WSe_2 growth favors coherent stacking at the graphene edges. An enhanced electronic performance of the stitched TMD-graphene monolayer heterojunctions is achieved because of improved contact properties.

Supplementary information

Supplementary information accompanies this paper at https://doi.org/10.1186/s11671-020-3261-y.

Additional file 1: Figure S1. Scalable synthesis of monolayer WSe_2 on sapphire: influence on (a) concentration of the seeding promoters and (b) temperature for the WSe_2 growth. **Figure S2.** Synthesis of the laterally stitched graphene-WS_2: (a) optical and (b)AFM image of the graphene-WS_2 and (c) PL spectrum of the WS_2. Raman mapping of (d) the E_{2g} mode of WS_2 and (e) the G' mode of graphene. (f) PL mapping of the Graphene-WS_2. (Scale bar: 4 μm).

Abbreviations

2D: Two-dimensional; AES: Auger electron spectroscopy; EIS: Electrochemical impedance spectroscopy; SEM: Scanning electron microscopy; TEM: Transmission electron microscopy; TMD: Transition metal dichalcogenides; XPS: X-ray photoelectron spectroscopy; XRD: X-ray diffraction

Authors' Contributions

YHL designed and supervised the project. YHL, XQZ, YTL, and YFC co-wrote the paper. XQZ and YTL contributed equally to this work. YTL and PHC performed device fabrication and measurements. XQZ, ECL, and JGR performed material synthesis, monolayer transfer, and material characterizations with the assistanceon TEM from C.C.C. and C.O. All authors discussed the results and commented on the manuscript at all stages. All authors read and approved the final manuscript.

Funding

We acknowledge the support from AOARD grant (co-funded with ONRG) FA2386-16-1-4009, Ministry of Science and Technology (MOST 108-2112-M-007-006-MY3, MOST 107-2923-M-007-002-MY3, MOST 106-2119-M-007-023-MY3, and MOST 105-2112-M-007-032-MY3), and Academia Sinica Research Program on Nanoscience and Nanotechnology (AS-iMATE-107-11), Taiwan. This work was partially supported by the "Frontier Research Center on Fundamental and Applied Sciences of Matters" and "Center for Quantum Technology" of National Tsing Hua University from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan.

Availability of Data and Materials

All data generated or analyzed during this study are included in this published article and its supplementary information files.

Competing Interests

The authors declare that they have no competing interests.

Received: 7 January 2020 Accepted: 20 January 2020
Published online: 12 March 2020

References

1. Novoselov KS, Geim AK, Morozov SV, Jiang D, Zhang Y, Dubonos SV, Grigorieva IV, Firsov AA (2004) Electric field effect in atomically thin carbon films. Science 306(5696):666–669
2. Desai SB, Madhvapathy SR, Sachid AB, Llinas JP, Wang QX, Ahn GH, Pitner G, Kim MJ, Bokor J, Hu CM, Wong HSP, Javey A (2016) MoS_2 transistors with 1-nanometer gate lengths. Science 354(6308):99–102
3. Chen PY, Zhang XQ, Lai YY, Lin EC, Chen CA, Guan SY, Chen JJ, Yang ZH, Tseng YW, Gwo S, Chang CS, Chen LJ, Lee YH (2019) Tunable moire superlattice of artificially twisted monolayers Adv Mater 31(37):1901077
4. Liu Y, Guo J, Zhu EB, Liao L, Lee SJ, Ding MN, Shakir I, Gambin V, Huang Y, Duan XF (2018) Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. Nature 557(7707):696
5. Yang TH, Chiu KC, Harn YW, Chen HY, Cai RF, Shyue JJ, Lo SC, Wu JM, Lee YH (2018) Electron field emission of geometrically modulated monolayer semiconductors. Adv Funct Mater 28(7):1706113
6. Allain A, Kang JH, Banerjee K, Kis A (2015) Electrical contacts to two-dimensional semiconductors. Nat Mater 14(12):1195
7. Kappera R, Voiry D, Yalcin SE, Branch B, Gupta G, Mohite AD, Chhowalla M (2014) Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors. Nat Mater 13(12):1128
8. Choi H, Moon BH, Kim JH, Yun SJ, Han GH, Leep SG, Gul HZ, Lee YH (2019) Edge contact for carrier injection and transport in MoS_2 field-effect transistors. ACS Nano 13(11):13169–13175
9. Khadka S, Lindquist M, Aleithan SH, Blumer AN, Wickramasinghe TE, Kordesch ME, Stinaff E (2017) Concurrent growth and formation of electrically contacted monolayer transition metal dichalcogenides on bulk metallic patterns. Adv Mater Interfaces 4(4):1600599
10. Yang Z, Kim C, Lee KY, Lee M, Appalakondaiah S, Ra CH, Watanabe K, Taniguchi T, Cho K, Hwang E, Hone J, Yoo WJ (2019) A Fermi-level-pinning-free 1D electrical contact at the intrinsic 2D MoS_2-metal junction. Adv Mater 31(25):1808231
11. Jain A, Szabo A, Parzefall M, Bonvin E, Taniguchi T, Watanabe K, Bharadwaj P, Luisier M, Novotny L (2019) One-dimensional edge contacts to a monolayer semiconductor. Nano Lett 19(10):6914–6923
12. Yu LL, Lee YH, Ling X, Santos EJG, Shin YC, Lin YX, Dubey M, Kaxiras E, Kong J, Wang H, Palacios T (2014) Graphene/MoS_2 hybrid technology for large-scale two-dimensional electronics. Nano Lett 14(6):3055–3063
13. Cui X, Lee GH, Kim YD, Arefe G, Huang PY, Lee CH, Chenet DA, Zhang X, Wang L, Ye F, Pizzocchero F, Jessen BS, Watanabe K, Taniguchi T, Muller DA, Low T, Kim P, Hone J (2015) Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. Nature Nanotechnol 10(6):534
14. Tang HL, Chiu MH, Tseng CC, Yang SH, Hou KJ, Wei SY, Huang JK, Lin YF, Lien CH, Li LJ (2017) Multilayer graphene-WSe_2 heterostructures for WSe_2 transistors. ACS Nano 11(12):12817–12823
15. Zheng CX, Zhang QH, Weber B, Ilatikhameneh H, Chen F, Sahasrabudhe H, Rahman R, Li SQ, Chen Z, Hellerstedt J, Zhang YP, Duan WH, Bao QL, Fuhrer MS (2017) Direct observation of 2D electrostatics and ohmic contacts in template-grown graphene/WS_2 heterostructures. ACS Nano 11(3):2785–2793
16. Ling X, Lin YX, Ma Q, Wang ZQ, Song Y, Yu LL, Huang SX, Fang WJ, Zhang X, Hsu AL, Bie YQ, Lee YH, Zhu YM, Wu LJ, Li J, Jarillo-Herrero P, Dresselhaus M, Palacios T, Kong J (2016) Parallel stitching of 2D materials. Adv Mater 28(12):2322–2329

17. Zhao MV, Ye Y, Han YM, Xia Y, Zhu HY, Wang SQ, Wang Y, Muller DA, Zhang X (2016) Large-scale chemical assembly of atomically thin transistors and circuits. Nature Nanotechnol 11(11):954
18. Hong W, Shim GW, Yang SY, Jung DY, Choi SY (2019) Improved electrical contact properties of MoS_2-graphene lateral heterostructure. Adv Funct Mater 29(6):1807550
19. Guimaraes MHD, Gao H, Han YM, Kang K, Xie S, Kim CJ, Muller DA, Ralph DC, Park J (2016) Atomically thin ohmic edge contacts between two-dimensional materials. ACS Nano 10(6):6392–6399
20. Chen X, Park YJ, Das T, Jang H, Lee JB, Ahn JH (2016) Lithography-free plasma-induced patterned growth of MoS_2 and its heterojunction with graphene. Nanoscale 8(33):15181–15188
21. Chen W, Yang Y, Zhang ZY, Kaxiras E (2017) Properties of in-plane graphene/MoS_2 heterojunctions. 2D Mater 4(4):045001
22. Chiu KC, Huang KH, Chen CA, Lai YY, Zhang XQ, Lin EC, Chuang MH, Wu JM, Lee YH (2018) Synthesis of in-plane artificial lattices of monolayer multijunctions. Adv Mater 30(7):1704796
23. Cai ZY, Liu BL, Zou XL, Cheng HM (2018) Chemical vapor deposition growth and applications of two-dimensional materials and their heterostructures. Chem Rev 118(13):6091–6133
24. Zhou W, Zhang YY, Chen JY, Li DD, Zhou JD, Liu Z, Chisholm MF, Pantelides ST, Loh KP (2018) Dislocation-driven growth of two-dimensional lateral quantum-well superlattices. Sci Adv 4(3):eaap9096
25. Yeh CH, Chen HC, Lin HC, Lin YC, Liang ZY, Chou MY, Suenaga K, Chiu PW (2019) Ultrafast monolayer In/Gr-WS_2-Gr hybrid photodetectors with high gain. ACS Nano 13(3):3269–3279
26. Duong DL, Yun SJ, Lee YH (2017) Van der Waals layered materials: opportunities and challenges. ACS Nano 11(12):11803–11830
27. Li MY, Pu J, Huang JK, Miyauchi Y, Matsuda K, Takenobu T, Li LJ (2018) Self-aligned and scalable growth of monolayer WSe2-MoS2 lateral heterojunctions. Adv Funct Mater 28(17):170686
28. Wang TJ, Andrews K, Bowman A, Hong T, Koehler M, Yan JQ, Mandrus D, Zhou ZX, Xu YQ (2018) High-performance WSe2 phototransistors with 2D/2D ohmic contacts. Nano Lett 18(5):2766–2771
29. Bosi M (2015) Growth and synthesis of mono and few-layers transition metal dichalcogenides by vapour techniques: a review. RSC Adv 5(92): 75500–75518
30. Huang JK, Pu J, Hsu CL, Chiu MH, Juang ZY, Chang YH, Chang WH, Iwasa Y, Takenobu T, Li LJ (2014) Large-area synthesis of highly crystalline WSe2 mono layers and device applications. ACS Nano 8(1):923–930
31. Li SS, Wang SF, Tang DM, Zhao WJ, Xu HL, Chu LQ, Bando Y, Golberg D, Eda G (2015) Halide-assisted atmospheric pressure growth of large WSe2 and WS2 monolayer crystals. Appl Mater Today 1(1):60–66
32. Ling X, Lee YH, Lin YX, Fang WJ, Yu LL, Dresselhaus MS, Kong J (2014) Role of the seeding promoter in MoS_2 growth by chemical vapor deposition. Nano Lett 14(2):464–472
33. Lee YH, Zhang XQ, Zhang WJ, Chang MT, Lin CT, Chang KD, Yu YC, Wang JTW, Chang CS, Li LJ, Lin TW (2012) Synthesis of large-area MoS_2 atomic layers with chemical vapor deposition. Adv Mater 24(17):2320–2325
34. Ferrari AC, Meyer JC, Scardaci V, Casiraghi C, Lazzeri M, Mauri F, Piscanec S, Jiang D, Novoselov KS, Roth S, Geim AK (2006) Raman spectrum of graphene and graphene layers. Phys Rev Lett 97(18):187401

Publisher's Note

Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Submit your manuscript to a SpringerOpen journal and benefit from:

- ► Convenient online submission
- ► Rigorous peer review
- ► Open access: articles freely available online
- ► High visibility within the field
- ► Retaining the copyright to your article

Submit your next manuscript at ► springeropen.com