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High Mobility Ge pMOSFETs with ZrO_2 Dielectric: Impacts of Post Annealing

Huan Liu, Genquan Han*, Yan Liu and Yue Hao

Abstract

This paper investigates the impacts of post metal annealing (PMA) and post deposition annealing (PDA) on the electrical performance of Ge p-type metal-oxide-semiconductor field-effect transistors (pMOSFETs) with ZrO_2 dielectric. For the transistors without PDA, on-state current (I_{ON}), subthreshold swing (SS), and capacitance equivalent thickness (CET) characteristics are improved with PMA temperature increasing from 350 to 500 °C. Crystallization of ZrO_2 dielectric at the higher PMA temperature contributes to the increase of the permittivity of ZrO_2 and the decrease of the density of interface states (D_{it}), resulting in a reduced CET and high effective hole mobility (μ_{eff}). It is demonstrated that Ge pMOSFETs with a PDA treatment at 400 °C have a lower CET and a steeper SS but a lower μ_{eff} compared to devices without PDA.

Keywords: Germanium, MOSFET, ZrO_2, PMA, PDA, Mobility

Background

Germanium (Ge) has been regarded as one of the attractive p-channel materials for advanced CMOS because it offers much higher hole mobility than does Si [1–3]. A high-quality gate dielectric and effective passivation of Ge surface are the keys to realizing the superior effective carrier mobility (μ_{eff}) and high drive current in Ge transistor [4–7]. Several high-κ materials such as HfO_2 [8], ZrO_2 [7, 9], La_2O_3 [10], and Y_2O_3 [11] have been studied as the alternative gate dielectrics for Ge p-type metal-oxide-semiconductor field-effect transistors (pMOSFETs) to achieve capacitance equivalent thickness (CET) scalability toward sub-1 nm. Among these, ZrO_2 dielectric has attracted most attention due to the much higher κ value [12, 13] and the better interfacial quality [14] compared to the Hf-based ones. It has widely been reported that crystallization of ZrO_2 can further improve the electrical performance of Ge pMOSFET, e.g., reducing CET and boosting μ_{eff} [15, 16]. However, there is a lack of study on the impacts of process steps for ZrO_2 crystallization on device performance of Ge transistors.

In this paper, we investigate the impacts of the post metal annealing (PMA) and the post deposition annealing (PDA) on the electrical performance of Ge pMOSFETs with ZrO_2 dielectric. Significantly improved μ_{eff} and reduced CET can be achieved in devices at higher PMA temperature.

Methods

Key process steps for fabricating Ge pMOSFETs with ZrO_2 dielectric are shown in Fig. 1a. The Ge pMOSFETs were fabricated on n-type Ge(001) wafer with a resistivity of 0.088–0.14 Ω·cm. After the several cycles of chemical cleaning in the diluted HF (1:50) solution and rinsing in DI water. Ge wafer was loaded into an atomic layer deposition (ALD) chamber. The Ge surface was passivated by an ozone post oxidation (OPO), i.e., an ultrathin Al_2O_3 layer was deposited at 300 °C, and then, the in situ OPO was carried out at 300 °C for 15 min. After that, a 5-nm-thick ZrO_2 was deposited at 250 °C in the same ALD chamber using TDMAZr and H_2O as precursors of Zr and O, respectively. During the deposition, $Zr[N(CH_3)_2]_4$ source was heated to 85 °C. PDA process was carried out on some sample at 400 °C for 60 s using the rapid thermal annealing. Samples with and without PDA were denoted wafer II and I, respectively. Then, a 100-nm-thick TaN gate electrode was deposited by reactive sputtering.

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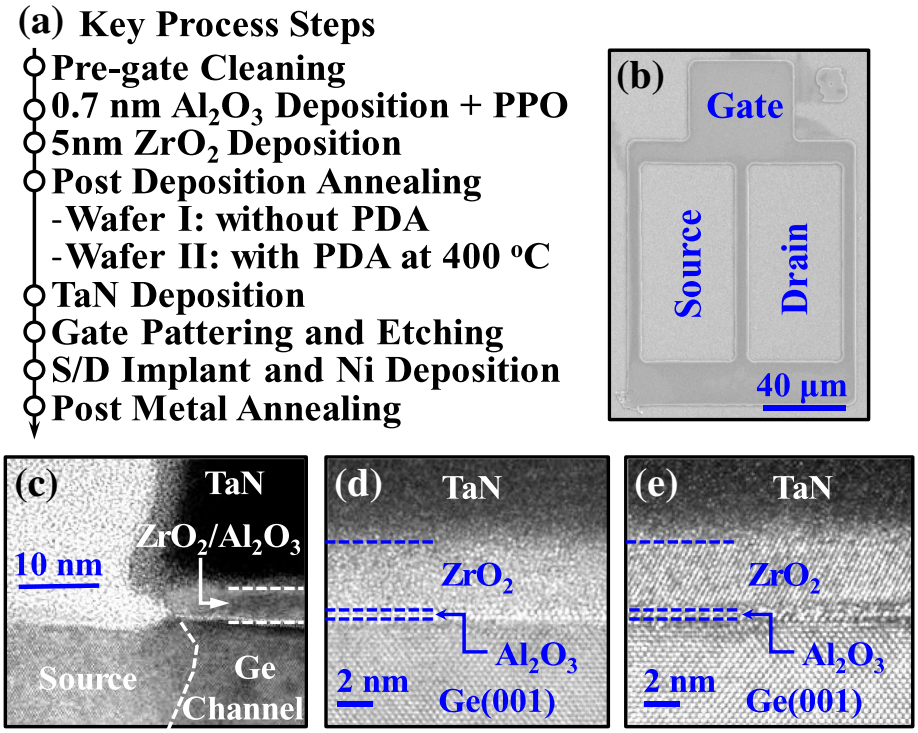

Fig. 1 **a** Key process steps for fabricating Ge pMOSFETs with ZrO_2 dielectric. **b** SEM image of the fabricated transistor. **c** XTEM image of Ge pMOSFET showing the gate and S/D regions. **d**, **e** HRTEM images of gate stacks of Ge pMOSFETs on wafer I annealed at 400 °C and 500 °C, respectively

After the gate patterning and etching, the source/drain (S/D) regions were formed by BF_2^+ implantation at an energy of 30 keV and a dose of 1×10^{15} cm^{-2}. Fifteen-nanometer nickel S/D contacts were formed by a lift-off process. Finally, the PMA at 350, 400, 450, and 500 °C for 30 s was carried out for dopant activation and S/D metallization.

Figure 1b shows the scanning electron microscope (SEM) image of a fabricated Ge pMOSFET. Figure 1c shows the cross-sectional transmission electron microscope (XTEM) image of Ge pMOSFET, showing the source/drain region, metal gate, and ZrO_2 dielectric. Figure 1d and e show the high-resolution TEM (HRTEM) images of the gate stacks of Ge pMOSFETs with a PMA at 400 and 500 °C, respectively, on wafer I. It is observed that the ZrO_2 dielectric was fully crystallized and underwent a PMA at 500 °C. The thickness of Al_2O_3 interfacial layer is about 0.7 nm.

Results and Discussion

Inversion capacitance C_{inv} vs. V_{GS} curves measured at a frequency of 300 kHz for the devices on wafer I are shown in Fig. 2. The CET values are extracted to be ~ 1.95, 1.80, 1.67, and 1.52 nm for the devices with PMA at 350, 400, 450, and 500 °C, respectively. The smaller CET is achieved at a higher PMA temperature due to the crystallization of ZrO_2. In general, the κ values for amorphous and crystalline ZrO_2 are about 20–23 and 28–30, respectively. A 5-nm-thick crystalline ZrO_2 contributes an EOT of ~ 0.7 nm. The shift of *C-V* curves with various PMA temperature is due to the fact that

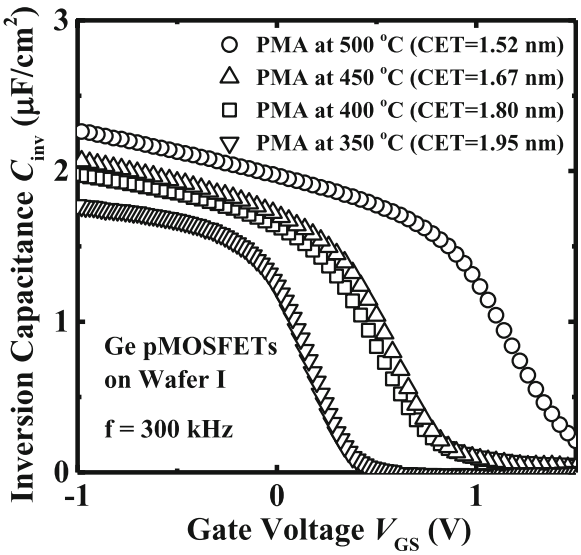

Fig. 2 Inversion C_{inv}-V_{GS} curves for the Ge pMOSFETs on wafer I with a PMA at 350 °C, 400 °C, 450 °C, and 500 °C

crystallization reduces the density of bulk traps in ZrO_2 dielectric.

Figure 3a shows the measured transfer characteristics and gate leakage currents I_G of Ge pMOSFETs on wafer I with the different PMA temperatures. All the devices have a gate length L_G of 4 μm and a gate width W of 100 μm. Ge pMOSFETs exhibit the much lower I_G compared to I_{DS} for all the PMA temperatures. An I_{ON}/I_{OFF} ratio above 10^4 is achieved for the device with a PMA at 500 °C. The I_{DS}-V_{DS} curves of the devices measured at the different gate overdrive $|V_{GS}$-$V_{TH}|$ are shown in Fig. 3b. It is noted that the threshold voltage V_{TH} is defined as the V_{GS} at I_{DS} of 10^{-7} A/μm. The Ge transistor with a PMA at 500 °C obtains the ~ 47% and 118% drive current improvement compared to the devices annealed at 450 °C and 350 °C, respectively, at a V_{DS} of − 1.0 V and a $|V_{GS}$-$V_{TH}|$ of 0.8 V. Figure 3c shows the statistical plot of the I_{ON} at a V_{DS} of − 0.5 V and a V_{GS}-V_{TH} of − 1 V for Ge pMOSFETs with the various PMA temperatures. All the transistors in this plot have an L_G of 4 μm and a W of 100 μm. Devices with a PMA at 500 °C exhibit an improved I_{ON} as compared to those with the lower PMA temperatures, which is attributed to the decreased S/D resistance, the reduced CET, and the higher μ_{eff}, which will be discussed later.

Figure 4 shows the statistical plots of midgap D_{it}, SS, and V_{TH} characteristics for the devices with the different PMA temperatures. As shown in Fig. 4a, based on the maximum conductance method [17], the midgap D_{it} values are extracted to be 1.3×10^{13}, 9.5×10^{12}, 9.2×10^{12}, and 6.3×10^{12} cm^{-2} eV^{-1} for the devices with the PMA at 350, 400, 450, and 500 °C,

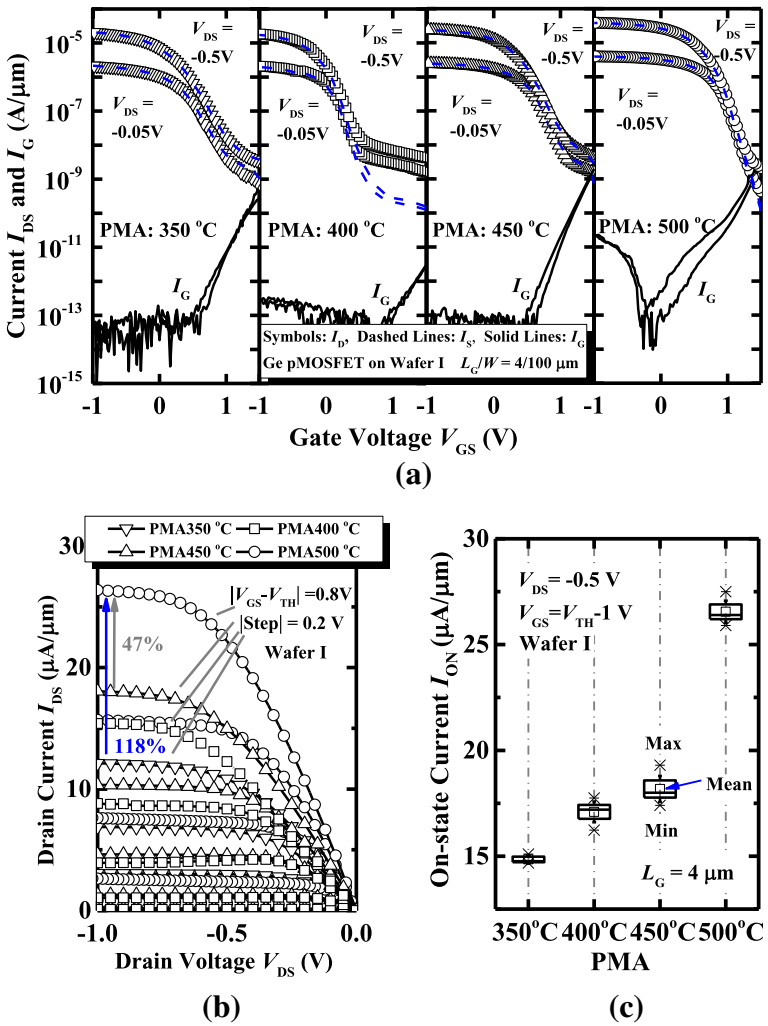

Fig. 3 **a** Measured I_D, I_S, and I_G *vs.* V_{GS} curves of Ge pMOSFETs on wafer I with the PMA at 350, 400, 450, and 500 °C. **b** I_{DS}-V_{DS} curves measured at the different V_{GS}-V_{TH} for the devices. **c** Device annealed at 500 °C has a higher on-state current I_{ON} compared to the transistors with the PMA at the lower temperatures

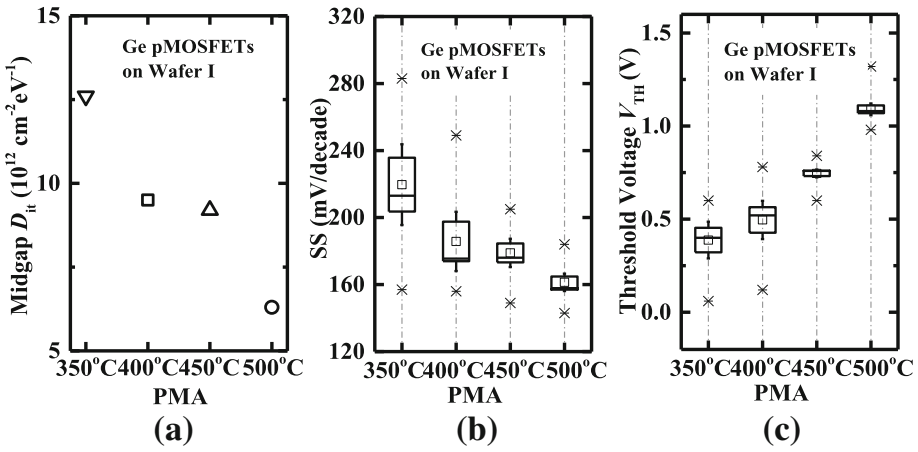

Fig. 4 Comparison of **a** midgap D_{it}, **b** SS, and **c** V_{TH} for Ge pMOSFETs on wafer I with the PMA at 350, 400, 450, and 500 °C

respectively. Figure 4b presents that Ge pMOSFETs annealed at 500 °C have the improved SS characteristics than the transistors annealed at the lower temperatures, due to the smaller midgap D_{it} and CET. The values of D_{it} and SS of Ge pMOSFETs with PMA are still higher than those of the best reported Ge transistors. It could possibly be reduced by optimizing the OPO passivation module, e.g., Al_2O_3 thickness and ozone oxidation temperature and duration. V_{TH} shifts to the positive V_{GS} with the increasing of PMA temperature, which is originated from the reduced CET and D_{it}. It is concluded that the best electrical performance is achieved for Ge pMOSFETs with a PMA at 500 °C.

μ_{eff}, as a crucial factor affecting device drive current and transconductance in Ge pMOSFETs, was measured using the $\Delta R_{tot}/\Delta L_G$ method [18]. A large number of devices were measured with L_G ranging from 1.5 to 9 μm. Figure 5a illustrates the total resistance R_{tot} extracted at a $|V_{GS}\text{-}V_{TH}|$ of − 1 V and a V_{DS} of − 0.05 V as a function of L_G. The R_{SD} is the value at which the fitted line intersects at the y-axis. The R_{SD} values were estimated about to be 7.85, 7.15, 6.10, and 4.35 kΩ·μm for devices with PMA at 350, 400, 450, and 500 °C, respectively. This is indicative of the better dopant activation of S/D at higher PMA temperature. μ_{eff} can be extracted by $\mu_{eff} = 1/[WQ_{inv}(\Delta R_{tot}/\Delta L_G)]$, where Q_{inv} is the inversion charge density in Ge channel and $\Delta R_{tot}/\Delta L_G$ is the slope of the R_{tot} vs. L_G as shown in Fig. 5a. The smaller $\Delta R_{tot}/\Delta L_G$ for devices with PMA at 500 °C indicates an enhancement in μ_{eff} as compared with transistors with PMA at 450 °C. Figure 5b shows μ_{eff} as a function of Q_{inv} curves, extracted using the split C-V method. The peak hole mobility is 384 cm^2/V·s for devices with a PMA at 500 °C, which is 31% higher than that of the devices with a PMA at 400 °C. At a high Q_{inv} of 1×10^{13} cm^{-2}, Ge

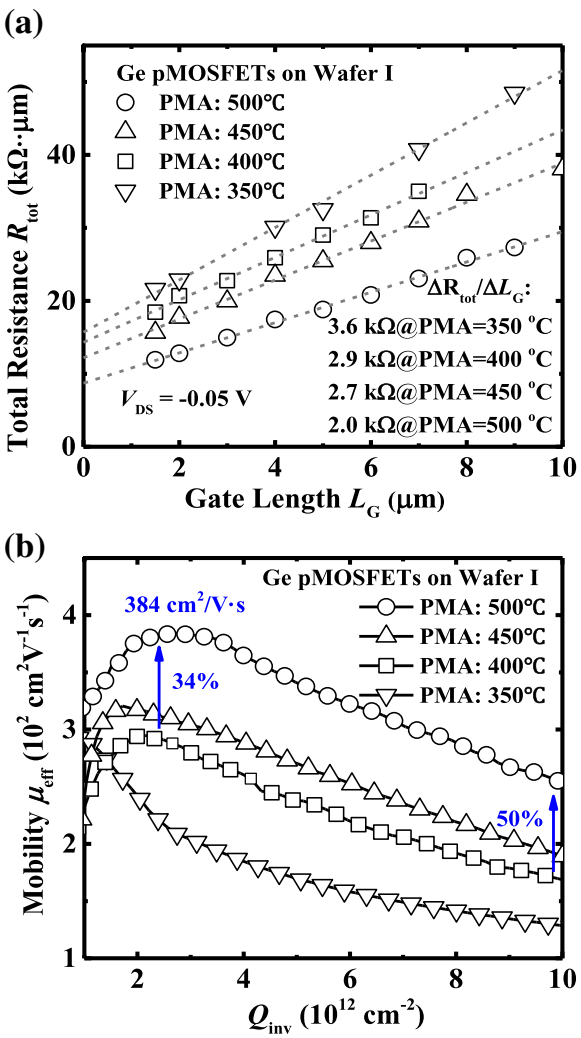

Fig. 5 **a** R_{tot} as a function of L_G at a V_{GS}-V_{TH} of − 1 V and a V_{DS} of − 0.05 V for devices on wafer I with various PMA temperatures. **b** μ_{eff} *vs.* Q_{inv} extracted by the split C-V method. The highest mobility is obtained in devices with a PMA at 500 °C

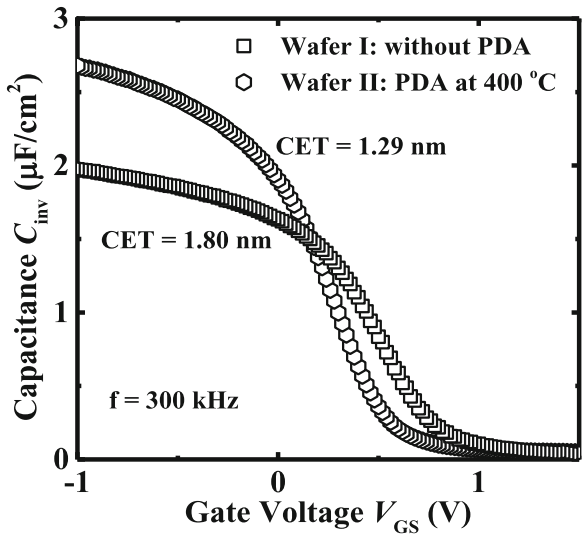

Fig. 6 C_{inv}-V_{GS} plots for the devices on wafer I and II with a PMA at 400 °C

pMOSFETs which underwent a PMA at 500 °C achieve a mobility enhancement in comparison with the devices annealed at 400 °C. Ge transistors with crystalline ZrO_2 have the lower density of bulk trap charge resulting in the lower remote Coulomb scattering of holes, compared to the devices with amorphous ZrO_2. Owing to the smooth interface between crystalline ZrO_2 and Ge, Ge devices annealed at 500 °C have a lower surface roughness scattering and show a shift of peak mobility to the higher Q_{inv}.

Next, we discuss the impacts of PDA on the electrical characteristics of Ge pMOSFETs. Figure 6 shows the measured C_{inv} vs. V_{GS} of the Ge pMOSFETs on wafer I and wafer II with a PMA at 400 °C. The device which underwent a PDA at 400 °C has a much lower CET value of 1.29 nm compared to the device without PDA, 1.80 nm. Figure 7a shows the I_D, I_S, and I_G-V_{GS} characteristic curves of Ge pMOSFETs on wafer I and wafer II, and the devices which underwent a PMA at 400 °C. A larger gate leakage current is obtained for the device with PDA compared to the transistor without PDA, which is due to the lower CET. The corresponding I_{DS}-V_{DS} curves of the devices measured at different gate overdrive V_{GS}-V_{TH} are shown in Fig. 7b. The Ge transistor without PDA shows a ~24% improvement in drive current over the one with PDA at 400 °C at the same overdrive of − 0.8 V in the saturation region.

Figure 8 plots the statistical results of midgap D_{it}, SS, and V_{TH} of the Ge pMOSFETs with and without PDA. Figure 8a shows that the smaller D_{it} is achieved in Ge pMOSFETs with PDA at 400 °C compared to devices without PDA. In Fig. 8b, the lower value of mean subthreshold swing of 142 mV/decade is achieved for devices with PDA at 400 °C, corresponding to the lower CET and the lower D_{it}. It indicates that devices with PDA at 400 °C have a superior ZrO_2/Ge interface. Figure 8c shows that devices with and without PDA have a different V_{TH}; it may be attributed to the density of traps in the lower bandgap half dominant in the V_{TH}.

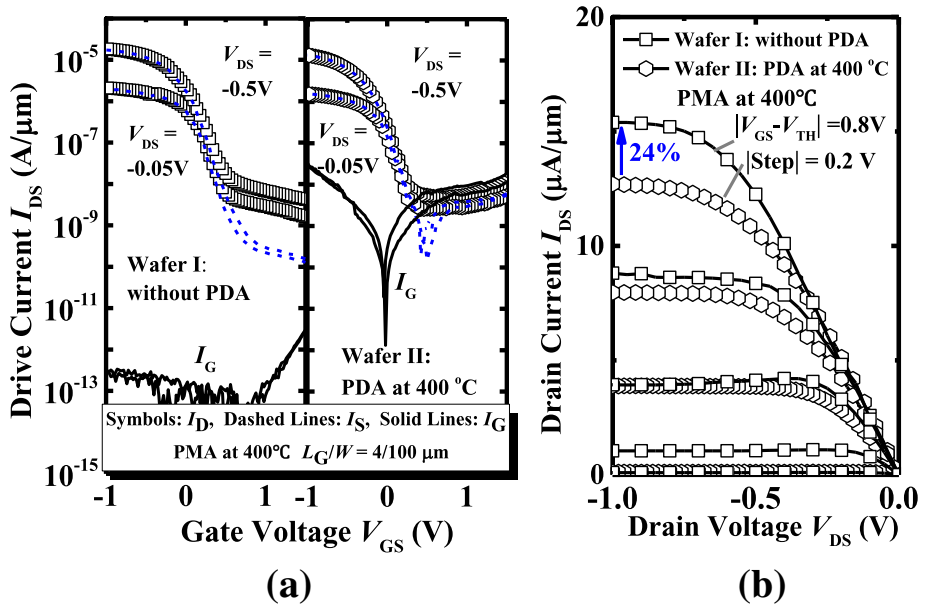

Fig. 7 **a** I_D, I_S, and I_G *vs.* V_{GS} curves of Ge pMOSFETs on wafer I and II with PMA at 400 °C. **b** I_{DS}-V_{DS} curves measured at different V_{GS}-V_{TH} for the devices

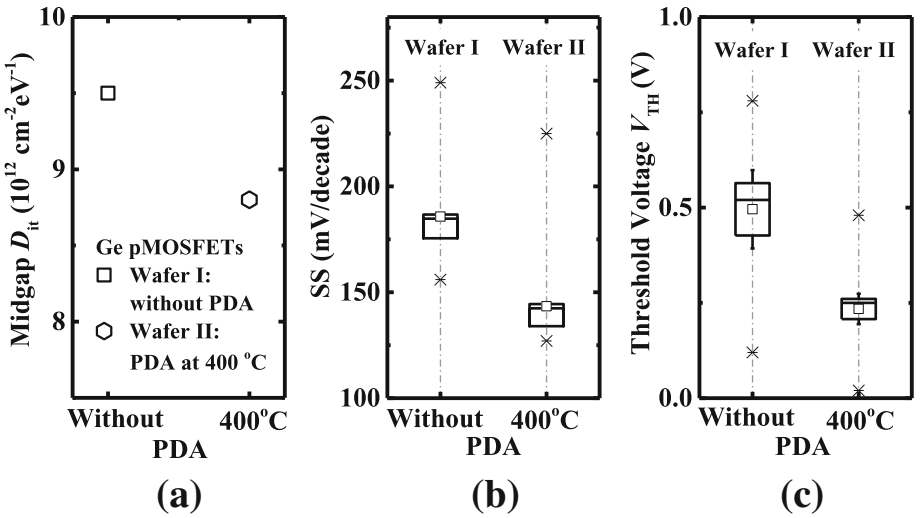

Fig. 8 Comparison of **a** midgap D_{it}, **b** SS, and **c** V_{TH} for Ge pMOSFETs on wafer I and II with PMA at 400 °C

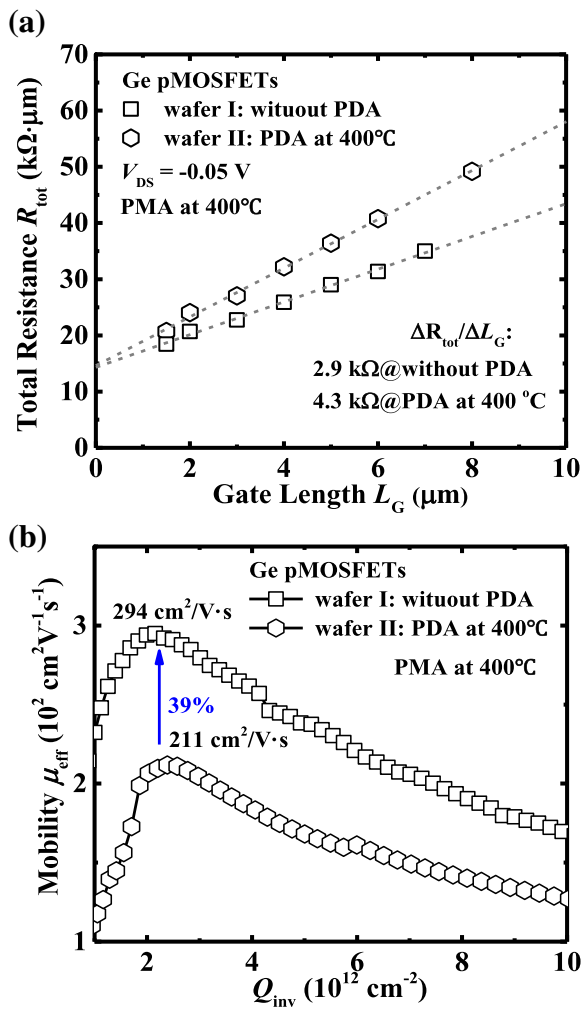

Fig. 9 **a** R_{tot} vs. L_G curves for devices on wafer I and wafer II with PMA at 400 °C. **b** Hole mobility μ_{eff} vs. Q_{inv} for devices with and without PDA

Figure 9a shows the R_{tot} vs. L_G curves at a gate overdrive of − 1 V and V_{DS} of − 0.05 V for devices with a PMA at 400 °C. The R_{SD} values are estimated about to be 7.15 and 7.30 kΩ·μm for devices without and with PDA at 400 °C, respectively. As shown in Fig. 9b, a remarkable higher peak μ_{eff} is achieved for Ge pMOSFETs without PDA, corresponding the smaller $\Delta R_{tot}/\Delta L_G$ in Fig. 9a, compared to devices with PDA. The devices with a PDA at 400 °C exhibit a peak μ_{eff} of 211 cm^2/V·s; the lower hole mobility might be mainly attributed to the strong remote Coulomb scattering contributed by the fixed charge in ZrO_2 dielectric.

Conclusions

In summary, the impacts of PMA and PDA on Ge pMOSFET with ZrO_2 dielectric were extensively investigated. Crystallization of ZrO_2 gate dielectric provides for significantly enhanced hole mobility and reduced CET compared to devices at the lower PMA temperature. A peak hole mobility of 384 cm^2/V·s and enhanced drive current have been achieved in devices with PMA at 500 °C. Devices with PDA at 400 °C exhibited the lower CET and the smaller D_{it} but the poor hole mobility and the larger leakage current compared with transistors without PDA.

Abbreviations

ALD: Atomic layer deposition; BF_2^+: Boron fluoride ion; CET: Capacitive effective thickness; Ge: Germanium; HF: Hydrofluoric acid; HRTEM: High-resolution transmission electron microscope; IL: Interfacial layer; MOSFETs: Metal-oxide-semiconductor field-effect transistors; Ni: Nickel; PDA: Post deposition annealing; PMA: Post metal annealing; SS: Subthreshold swing; TaN: Tantalum nitride; TDMAZr: Tetrakis (dimethylamido) hafnium; ZrO_2: Zirconium dioxide; μ_{eff}: Effective carrier mobility

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Author's Contributions

HL carried out the experiments and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. YH provided constructive advice in the drafting. All the authors read and approved the final manuscript.

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

Competing Interests

The authors declare that they have no competing interests.

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