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Comparative Study of Negative Capacitance Field-Effect Transistors with Different MOS Capacitances

Jing Li, Yan Liu*, Genquan Han*, Jiuren Zhou and Yue Hao

Abstract

We demonstrate the negative capacitance (NC) effect of $HfZrO_x$-based field-effect transistors (FETs) in the experiments. Improved I_{DS}, SS, and G_m of NCFET have been achieved in comparison with control metal oxide semiconductor (MOS) FET. In this experiment, the bottom MIS transistors with different passivation time are equivalent to the NC devices with different MOS capacitances. Meanwhile, the electrical properties of NCFET with 40 min passivation are superior to that of NCFET with 60 min passivation owing to the good matching between C_{FE} and C_{MOS}. Although SS of sub-60 mV/decade is not achieved, the non-hysteretic transfer characteristics beneficial to the logic applications are obtained.

Keywords: Germanium, Negative capacitance, Passivation time

Introduction

With the scaling down of transistor, the integration level of integrated circuit (IC) is continuous growing. An accompanying power dissipation problem is urgent to be solved. In order to circumvent this problem, the operation voltage of the transistor should be reduced [1]. The subthreshold swing (SS) of MOSFET cannot be below 60 mV/decade at room temperature, which restricts the reduction of threshold voltage V_{TH} and supply voltage V_{DD} [2]. Many efforts have been devoted to the research and the development of devices with novel transport and switching mechanisms to beat the Boltzmann limit, including negative capacitance field-effect transistor (NCEFT) [3, 4], resistive gate FET [5], nano-electro mechanical FET (NEMFET) [6, 7], impact ionization metal-oxide-semiconductor (I-MOS) [8, 9], and tunneling FET [10, 11]. Among them, NCFET has aroused much attention because it can achieve a steep SS without losing the drive current [12–15]. Doped HfO_2 (e.g., $HfZrO_x$ (HZO) and $HfSiO_x$) has been widely used in NCFETs [4, 16, 17]; it is compatible with the CMOS process [18]. A theoretical study has shown that the undesired hysteresis occurs due to unmatched ferroelectric capacitance C_{FE} to underlying MOS capacitance C_{MOS} in NCFET [19]. However, the effect of matching between C_{FE} and C_{MOS} on the electrical characteristics of NCFETs is still a concern in the experiments.

In this work, the electrical characteristics of NC Ge FETs with different MOS capacitances are studied based on the different matching between C_{FE} and C_{MOS}. Although SS less than 60 mV/decade does not appear, the hysteresis-free transfer characteristics and better electrical properties are obtained. Apparent peaks of C_{FE} versus V_{FE} curves demonstrate NC effect of HZO based NCFETs. The better matching of C_{FE} and C_{MOS} contributes to steeper SS and higher on current, which is beneficial to the logic applications.

Methods

The key fabrication process of Ge NCFETs is shown in Fig. 1a. Four-inch n-Ge(001) wafers with a resistivity of 0.088–0.14 Ω·cm were used as the starting substrates. After pre-gate cleaning, Ge wafers were loaded into an ultra-high vacuum chamber for surface passivation using Si_2H_6. Two passivation durations of 40 and 60 min were used. Then, $TaN/HZO/TaN/HfO_2$ stack was deposited. The thicknesses of the HfO_2 dielectric layer and HZO

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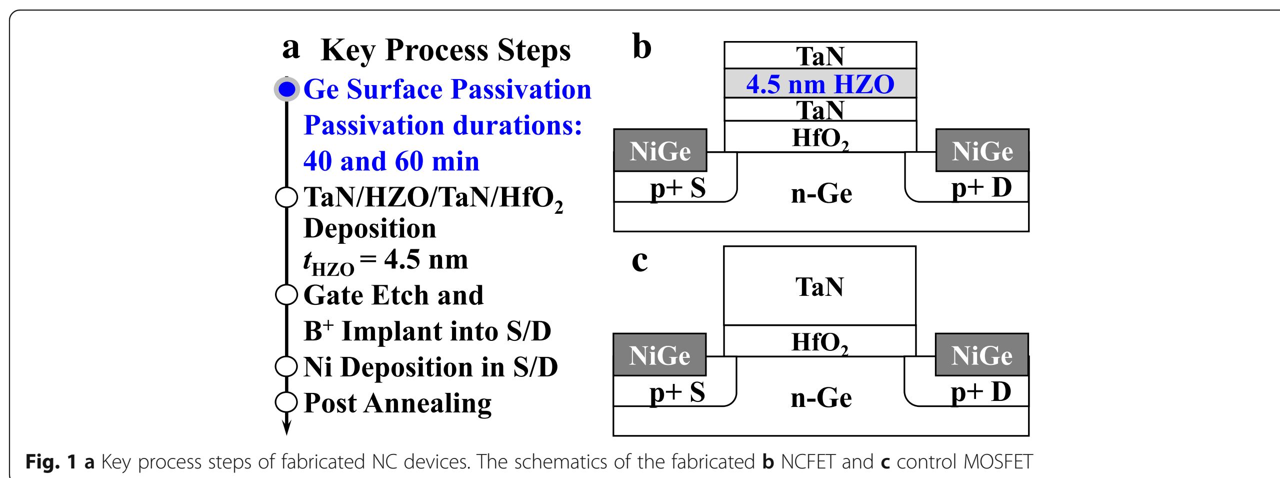

Fig. 1 a Key process steps of fabricated NC devices. The schematics of the fabricated **b** NCFET and **c** control MOSFET

FE layer are 4.35 and 4.5 nm, respectively. After gate patterning and etching, source/drain (S/D) regions were implanted using boron ions (B^+) at an energy of 30 keV and a dose of 1 × 10^{15} cm^{-2}. S/D metal Nickel was formed using a lift-off process. Finally, rapid thermal annealing at 450 °C for 30 s was carried out. Control MOSFET with TaN/HfO_2 stack was also fabricated. Figures 1b and c show the schematics of fabricated NCFET and control MOSFET, respectively. The internal metal gate in the fabricated NCFET counterbalances the potential at the channel surface, which is called the MFMIS structure.

Results and Discussion

Figure 2a plots the measured I_{DS}-V_{GS} curves of a pair of NCFET and control MOSFET with 40 min surface passivation. Both devices have a gate length L_G of 3.5 μm. The NC device with 40 min passivation has a significantly improved I_{DS} than the control MOSFET. The transfer curves of NCFET exhibit a non-hysteretic feature. Point SS versus I_{DS} curves in Fig. 2b show that the NC transistor has improved SS over the control device, although SS of sub-60 mV/decade does not appear. Figure 2c shows that NC transistor obtains a significantly boosted linear transconductance G_m over the control device at V_{DS} of − 0.05 V. Figure 3 compares the electrical performances of NCFET and control MOSFET with surface passivation for 60 min. Similarly, the I_{DS}, point SS and G_m of NCFET are superior to that of control MOSFET.

Figure 4a shows the statistical results of the drive current of NCFETs and control MOSFETs at V_{DS} of − 0.05 V and V_{GS}-V_{TH} = − 1.0 V. NCFETs demonstrate 18.7% and 35.6% improvement in I_{DS} for the 60 min and 40 min surface passivation, respectively, in comparison with the control devices. It is speculated that the

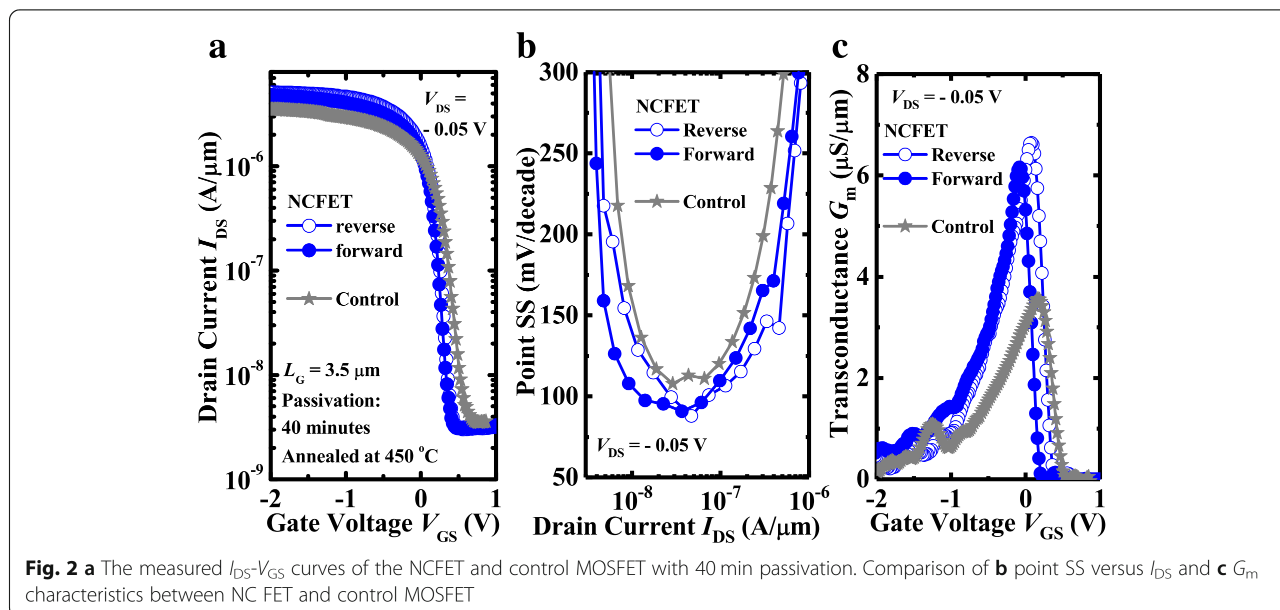

Fig. 2 a The measured I_{DS}-V_{GS} curves of the NCFET and control MOSFET with 40 min passivation. Comparison of **b** point SS versus I_{DS} and **c** G_m characteristics between NC FET and control MOSFET

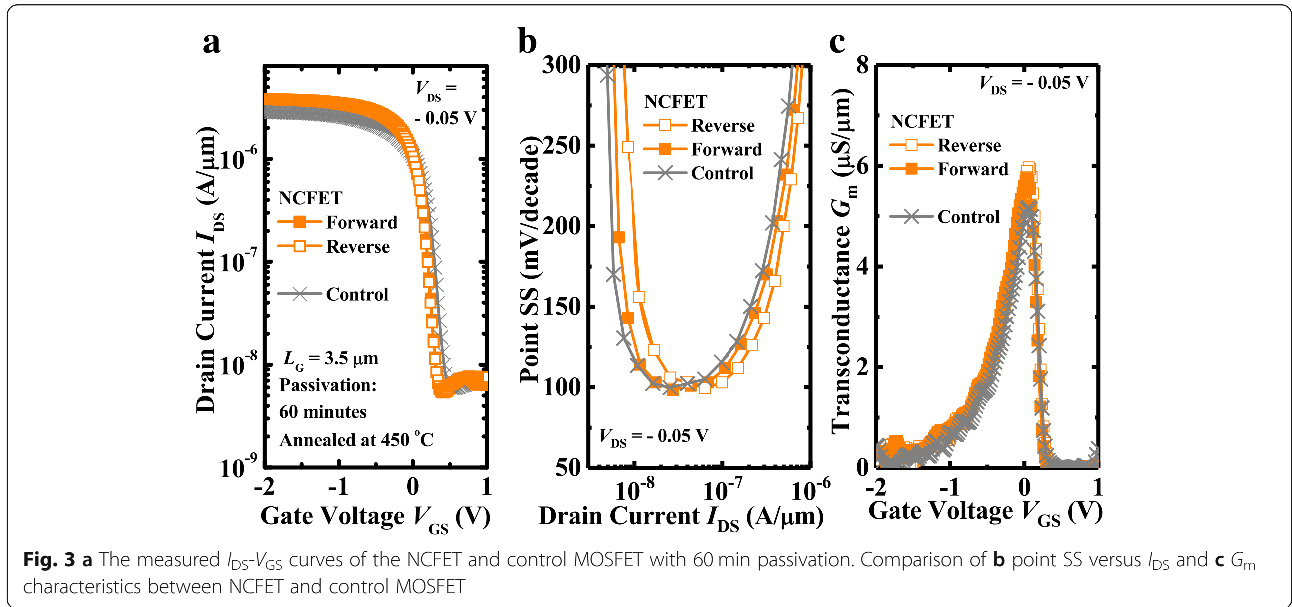

Fig. 3 **a** The measured I_{DS}-V_{GS} curves of the NCFET and control MOSFET with 60 min passivation. Comparison of **b** point SS versus I_{DS} and **c** G_m characteristics between NCFET and control MOSFET

NCFETs passivated for 40 min have a better matching between C_{MOS} and C_{FE} over the NC devices with 60 min. Figure 4b shows that NCFETs obtain 26.4% and 51.3% improvement in maximum transconductance $G_{m,max}$ for 60 min and 40 min surface passivation, respectively, in comparison with the control devices. It is seen that the control MOSFETs with surface passivation for 40 min have a higher I_{DS} and $G_{m,max}$ than the devices passivated for 60 min, which is due to the larger C_{MOS} induced by the smaller equivalent oxide thickness (E_{OT}). The internal metal gate provides an equipotential plane; the device can be equivalently modeled as a capacitive voltage divider. The total capacitance C_G is a series of C_{FE} and C_{MOS}. The internal gate voltage is amplified owing to the NC effect. The internal voltage amplification coefficient $\beta = |C_{FE}| / |C_{FE}| - C_{MOS}$ gets the maximum when $|C_{MOS}| = |C_{FE}|$ [20, 21]. Achieving the optimized matching of C_{FE} and C_{MOS} is the prerequisite of the improvement of on current.

The extracted V_{int} versus gate voltage V_{GS} curves are shown in Fig. 5a. V_{int} of NC transistor can be extracted on account of the hypothesis that I_{DS}-V_{int} curve of NC transistor is exactly identical with I_{DS}-V_{GS} curve of the control device. The internal voltage amplification coefficient dV_{int}/dV_{GS} is shown in Fig. 5b. $dV_{int}/dV_{GS} > 1$ is achieved in the wide sweeping range of V_{GS} for the NCFET with 40 min surface passivation, contributing to a steeper SS than the control device during the measuring process,

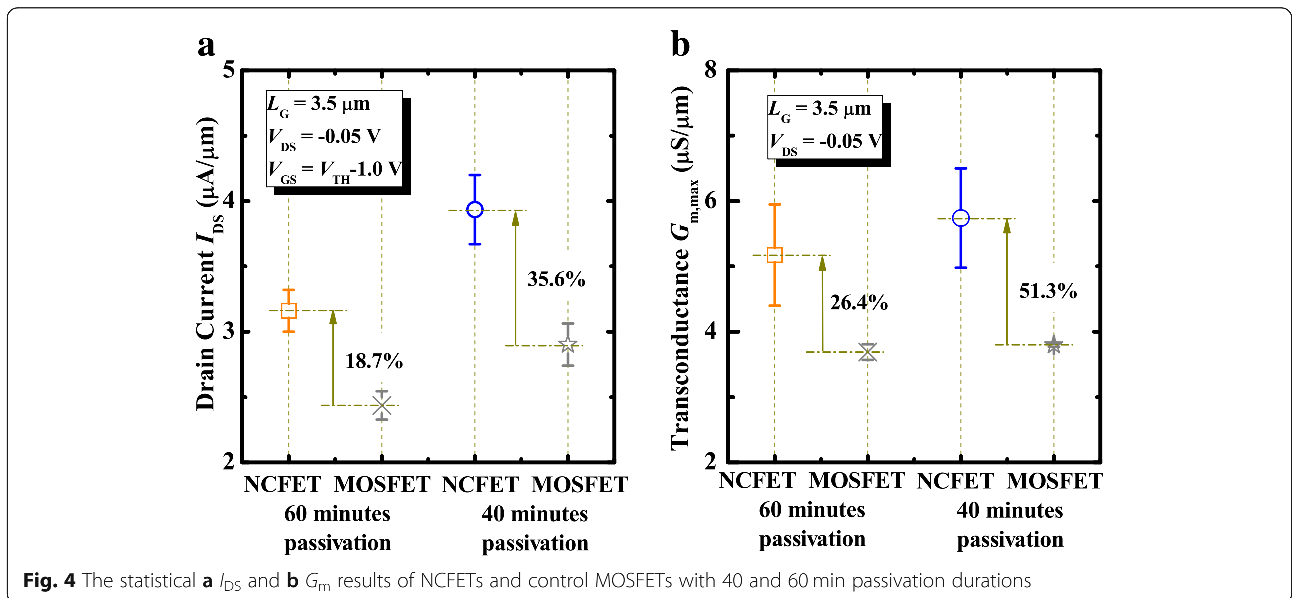

Fig. 4 The statistical **a** I_{DS} and **b** G_m results of NCFETs and control MOSFETs with 40 and 60 min passivation durations

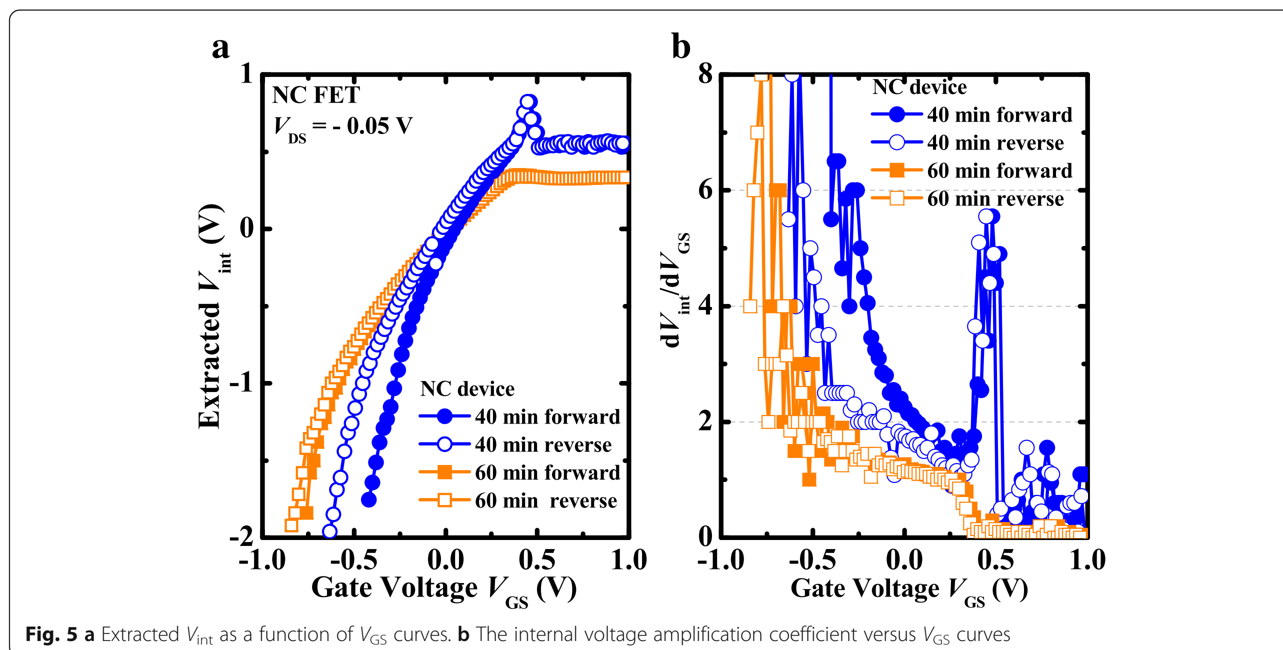

Fig. 5 **a** Extracted V_{int} as a function of V_{GS} curves. **b** The internal voltage amplification coefficient versus V_{GS} curves

which is due to the local polarization switching [22]. It is consistent with the aforementioned results in Fig. 2b. For the NCFET with 60 min passivation, the internal voltage amplification coefficient $dV_{int}/dV_{GS} > 1$ is achieved during the range of $V_{GS} < 0$ V for the double sweeping of V_{GS}, which is in agreement with the elevated SS in Fig. 3b.

Figure 6a shows the extracted C_{MOS} versus V_{GS} curves for NC transistor, which is relying on the V_{int}-V_{GS} in Fig. 5a and the C_G-V_{GS} curves of control MOSFETs. The extracted C_{MOS} is in good agreement with the measured C_G. Hence, the validity of the calculation method is demonstrated. The C_{FE} and C_{MOS} versus V_{FE} curves are depicted in Fig. 6b. From the initiation of NC effect, the absolute value of negative C_{FE} of the transistor exceeds C_{MOS} for double sweeping of V_{GS} all the time in Fig. 6b. $|C_{FE}| > C_{MOS}$ and $C_{FE} < 0$ can cause hysteresis-free characteristics, and the matching of C_{MOS} and C_{FE} is beneficial to the logic applications [23, 24]. Hysteresis-free characteristics in Figs. 2a and 3a are observed attributed to all the domain matching and inhibited charge trapping [25]. The

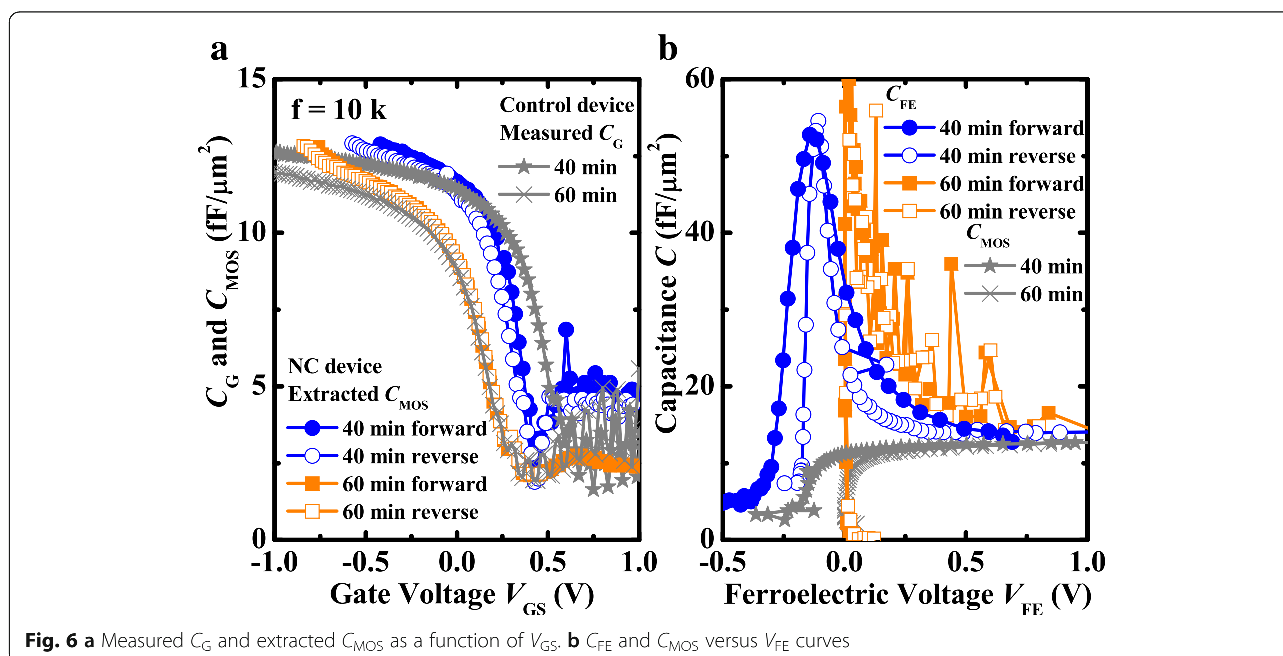

Fig. 6 **a** Measured C_G and extracted C_{MOS} as a function of V_{GS}. **b** C_{FE} and C_{MOS} versus V_{FE} curves

stable polarization switching is responsible for the non-hysteretic characteristics [26]. Furthermore, the large internal gate gain $dV_{int}/dV_G > 1$ is ascribed to the slight discrepancy between $|C_{FE}|$ and C_{MOS} in the subthreshold region, resulting in the steep SS of NC device. Meanwhile, there is a better matching between C_{FE} and C_{MOS} for the NCFET with 40 min passivation than the NCFET with 60 min passivation. Thus, this provides direct evidence to indicate that the NCFET with 40 min passivation possesses a better electrical performance than the NCFET with 60 min passivation. The FE polarization changes the V_{FE}; hence the charge of FE varies. The total charge multiplies, which is attributed to the FE polarization besides the increment of V_{GS}. In other words, for the given V_{GS}, the charge in the channel increases so the I_{DS} improves. As a consequence, the steep SS of transfer characteristic appears in the experiments.

Conclusions

The hysteresis-free transfer characteristics are obtained for the NCFETs with 40 and 60 min passivation. NC Ge pFETs with 40 min passivation have better electrical characteristics than the NC device with 60 min passivation in experiments. We also demonstrate the NC effect of HZO based NCFETs. For NCFETs, the steep SS and $dV_{int}/dV_{GS} > 1$ are obtained. The NCFET with 40 min passivation has achieved a good matching between C_{FE} and C_{MOS}, which contributes to the non-hysteretic characteristics. The different NC behaviors are considered to be related to the microscopic domain wall switching in the FE thin films.

Abbreviations

B^+: Boron ions; E_{OT}: Equivalent oxide thickness; FETs: Field-effect transistors; HZO: $HfZrO_x$; IC: Integrated circuit; I-MOS: Impact ionization metal-oxide-semiconductor; MOS: Metal oxide semiconductor; NC: Negative capacitance; NCFET: Negative capacitance field-effect transistor; NEMFET: Nano-electro mechanical FET; S/D: Source/drain; SS: Subthreshold swing

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Not applicable.

Author's Contributions

RJZ carried out the experiments. JL tested the experimental results and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. All the authors read and approved the final manuscript.

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Availability of Data and Materials

The datasets supporting the conclusions of this article are included in the article.

Competing Interests

The authors declare that they have no competing interests.

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References

1. Ionescu AM, Michielis D, Dagtekin N, Salvatore G, Cao I AR, Bartsch S (2011) Ultra low power: emerging devices and their benefits for integrated circuits. In: IEEE International Electron Devices Meeting, Washington. https://doi.org/10.1109/IEDM.2011.6131563
2. Avci UE, Morris DH, Young IA (2015) Tunnel field-effect transistors: prospects and challenges. IEEE Journal of the Electron Devices Society 3:88–95
3. Chung W, Meng S, Peide DY (2017) Hysteresis-free negative capacitance germanium CMOS FinFETs with bi-directional sub-60 mV/dec. In: IEEE International Electron Devices Meeting, San Francisco. https://doi.org/10.1109/IEDM.2017.8268395
4. Kwon D, Chatterjee K, Tan AJ, Yadav AK, Zhou H, Sachid AB, Reis RD, Hu C, Salahuddin S (2017) Improved subthreshold swing and short channel effect in FDSOI n-channel negative capacitance field effect transistors. IEEE Electron Device Lett 39:300–303
5. Huang Q, Huang R, Pan Y, Tan S, Wang Y (2014) Resistive-gate field-effect transistor: a novel steep-slope device based on a metal-insulator-metal-oxide gate stack. IEEE Electron Device Letters 35:877–879
6. Kam H, Lee DT, Howe RT, King T-J (2005) A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics. In: IEEE International Electron Device Meeting, Washington, DC. https://doi.org/10.1109/IEDM.2005.1609380
7. Abele N, Fritschi N, Boucart K, Casset F, Ancey P, Ionescu AM (2005) Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor. In: IEEE International Electron Device Meeting, Washington, DC. https://doi.org/10.1109/IEDM.2005.1609384
8. Choi WY, Song JY, Lee JD, Park YJ, Park B-G (2005) 100-nm n-/p-channel I-MOS using a novel self-aligned structure. IEEE Electron Device Lett 26:261–263
9. Ramaswamy S, Kumar MJ (2014) Junction-less impact ionization MOS: proposal and investigation. IEEE Trans Electron Devices 61:4295–4298
10. Han G, Wang Y, Liu Y, Zhang C, Feng Q, Liu M, Zhao S, Cheng B, Zhang J, Hao Y (2016) GeSn Quantum Well P-Channel Tunneling FETs Fabricated on Si(001) and (111) with improved subthreshold swing. IEEE Electron Device Lett 37:701–704
11. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. Nature 479:329–337
12. Garam K, Lee J, Kim JH, Kim S (2019) High on-current Ge-channel heterojunction tunnel field-effect transistor using direct band-to-band tunneling. Micromachines 10:E77
13. Zhou J, Han G, Li Q, Peng Y, Lu X, Zhang C, Zhang J, Sun Q, Zhang D, Hao Y (2016) Ferroelectric $HfZrO_x$ Ge and GeSn PMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved I_{DS}. In: IEEE International Electron Devices Meeting, San Francisco. https://doi.org/10.1109/IEDM.2016.7838401
14. Zhou J, Peng Y, Han G, Li Q, Liu Y, Zhang J, Liao M, Sun Q, Zhang D, Zhou Y, Hao Y (2018) Hysteresis reduction in negative capacitance Ge PFETs enabled by modulating ferroelectric properties in $HfZrO_x$. IEEE J Electron Devices Soc 6:41–48
15. Wu J, KanYang R, Han G, Zhou J, Liu Y, Wang Y, Peng Y, Zhang J, Sun Q, Zhang D, Hao Y (2018) Nonideality of negative capacitance Ge field-effect transistors without internal metal gate. IEEE Electron Device Lett 39:614–617
16. Sharma P, Zhang J, Ni K, Datta S (2018) Time-resolved measurement of negative capacitance. IEEE Electron Device Letters 39:272–275
17. Li KS, Chen P-G, Lai TY, Lin CH, Cheng C-C, Chen CC, Liao M-H, Lee MH, Chen MC, Sheih JM, Sheih WK, Yeh WK, Yang FL, Salahuddin S, Hu C (2015) Sub-60 mV-Swing negative-capacitance FinFET without hysteresis. In: IEEE International Electron Devices Meeting, Washington, DC. https://doi.org/10.1109/IEDM.2015.7409760
18. Lee MH, Lin J-C, Wei Y-T, Chen C-W, Tu W-H, Zhuang H-K, Tang M (2013) Ferroelectric negative capacitance hetero-tunnel field-effect-transistors with internal voltage amplification. In: IEEE International Electron Devices Meeting, Washington, DC. https://doi.org/10.1109/IEDM.2013.6724561
19. Khan AI, Chatterjee K, Duarte JP, Lu Z, Sachid A, Khandelwal S, Ramesh R, Hu C, Salahuddin S (2016) Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor. IEEE Electron Device Letters 37:111–114. https://doi.org/10.1109/LED.2015.2501319

20. Khan AI, Yeung CW, Hu C, Salahuddin S (2011) Ferroelectric negative capacitance MOSFET: capacitance tuning & antiferroelectric operation. In: IEEE International Electron Devices Meeting, Washington, DC. https://doi.org/10.1109/IEDM.2011.6131532
21. Yueng CW, Khan AI, Sarker A, Salahuddin S, Hu C (2013) Low power negative capacitance FETs for future quantum-well body technology. In: international symposium on VLSI Technology, Hsinchu. https://doi.org/10.1109/VLSI-TSA.2013.6545648
22. Li X, Toriumi A (2018) Direct relationship between sub-60 mV/dec subthreshold swing and internal potential instability in MOSFET externally connected to ferroelectric capacitor. In: IEEE International Electron Devices Meeting. https://doi.org/10.1109/IEDM.2018.8614703
23. Pahwa G, Dutta T, Agarwal A, Chauhan YS (2017) Compact model for ferroelectric negative capacitance transistor with MFIS structure. IEEE Trans Electron Devices 64:1366–1374
24. Khan AI, Radhakrishna U, Salahuddin S, Antoniadis D (2017) Work function engineering for performance improvement in leaky negative capacitance FETs. IEEE Electron Device Letters 38:1335–1338
25. Hoffmann M, Max B, Mittmann T, Schroeder U, Slesazeck S, Mikolajick T (2018) Demonstration of high-speed hysteresis-free negative capacitance in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. In: IEEE International Electron Devices Meeting. https://doi.org/10.1109/IEDM.2018.8614677
26. Zhou J, Han G, Xu N, Li J, Peng Y, Liu Y, Zhang J, Sun Q, Zhang D, Hao Y (2019) Incomplete dipoles flipping produced near hysteresis-free negative capacitance transistors. IEEE Electron Device Lett 40:329–332

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