Nanoscale Research Letters

NANO EXPRESS Open Access

Improved Ferroelectric Performance of Mg-Doped $LiNbO_3$ Films by an Ideal Atomic Layer Deposited Al_2O_3 Tunnel Switch Layer

Yan Zhang[1], Qing Hua Ren[2*], Xiao Jie Chai[1], Jun Jiang[1], Jian Guo Yang[1] and An Quan Jiang[1*]

Abstract

Bilayer structures composed of 5% Mg-doped $LiNbO_3$ single-crystal films and ultrathin Al_2O_3 layers with thickness ranging from 2 to 6 nm have been fabricated by using ion slicing technique combined with atomic layer deposition method. The transient domain switching current measurement results reveal that the *P-V* hysteresis loops are symmetry in type II mode with single voltage pulse per cycle, which may be attributed to the built-in electric field formed by asymmetric electrodes and compensation of an internal imprint field. Besides, the inlaid Al_2O_3, as an ideal tunnel switch layer, turns on during ferroelectric switching, but closes during the post-switching or non-switching under the applied pulse voltage. The Al_2O_3 layer blocks the adverse effects such as by-electrode charge injection and improves the fatigue endurance properties of Mg-doped $LiNbO_3$ ferroelectric capacitors. This study provides a possible way to improve the reliability properties of ferroelectric devices in the non-volatile memory application.

Keywords: Tunnel switch, Mg-doped $LiNbO_3$, Atomic layer deposition, Ion slicing, Ferroelectric memory

Background

Lithium niobate (LN) single-crystal films, due to their excellent physical properties, [1–6] have been widely used in surface acoustic wave oscillators, electro-optic modulators, and data storage based on the domain switching. Recently, wafer-scale lithium niobate-on-insulator (LNOI), which has great potential application for high-density integrated circuits in electro-optic, acousto-optic, and data storage devices, is fabricated by an ion implantation and wafer bonding technology. This technology allows for a wide variety of substrates, such as LN, silicon, and even the CMOS circuit [3, 7–9]. However, the imprint hysteresis loop originated from preferred orientations and the poor fatigue endurance of LN films, due to by-electrode charge injection, destabilize the retention of polarization reversal, which limits their application in non-volatile memory devices [10–13]. The preferred orientations related to interfacial passive layers formed between ferroelectric layers and electrodes, which can induce a strong depolarization field in the opposite direction of polarization. It can drive out the injected charges after the removal of the applied voltage or during intermittent time of the sequent pulse stressing [11, 12]. On the other hand, because of the presence of interfacial passive layers, the fatigue endurance of LN films will be improved by blocking the charge injection from by-electrode after ferroelectric switching. However, the fatigue process accelerates if the time of the applied pulse periodicity is shorted below 0.5 s. This is described by the interfacial passive layers contribution of the accumulative space charge at certain frequencies [11]. It is reported that an inlaid Al_2O_3 dielectric film can play as a tunnel switch in the dielectric/ferroelectric bilayer capacitor, for example, in Al_2O_3/Pb $(Zr,Ti)O_3$, and Al_2O_3/Mn-doped $BiFeO_3$ bilayer structures [14–16]. The Al_2O_3 tunnel switch turns on as a conductor during polarization switching, but switches off as an insulator to block the by-electrode charge injection after completed polarization switching or no switching operation [14]. Therefore, it can prevent the unwanted injected charges and polarization backswitching, and then improve the reliability of dielectric/ferroelectric bilayer capacitor.

* Correspondence: qhren@mail.sim.ac.cn; aqjiang@fudan.edu.cn
[2]State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
[1]State Key Laboratory of ASIC & System, School of Microelectronics, Fudan University, Shanghai 200433, China

In this paper, we fabricated 200-nm-thickness Z-cut 5% Mg-doped congruent LN single-crystal thin films and then deposited ultrathin Al_2O_3 layers with various thicknesses (2–6 nm) on LN to form bilayer capacitor structures. The Al_2O_3 films as tunnel switch layers can improve the fatigue endurance. Asymmetric electrodes (Au/Pt electrodes) are designed to form a built-in electric field against the depolarization field induced by the interfacial passive layers. The electrical results exhibit the symmetrisation of hysteresis loop transferred from the domain switching current transients with time. Meanwhile, it also proves that the inlaid Al_2O_3 layer plays as a tunnel switch layer, which can turn up during the ferroelectric switching and close after completed polarization switching or no switching operation.

Methods

The Z-cut 5% Mg-doped congruent $LiNbO_3$ (LN) single-crystal thin films were peeled off from their bulk crystals by using an ionic implantation and wafer bonding technology, as described elsewhere [10, 11, 17, 18]. In detail, the surface layer of a LN bulk crystal was first implanted with He ions in desired depth by controlling the implantation energy and the dose of injected ions, and then 5 nm Cr adhesion layer and 100 nm Pt bottom electrode layer are deposited by DC sputtering (K. J. Lesker PVD-75). The surface layer was bonded to another LN substrate covered with 1-μm-thick SiO_2 buffer layer and sliced off. The thickness of LN film is controlled to about 200 nm by chemical mechanical polishing. Subsequently, ultrathin Al_2O_3 films with thicknesses (d) of 2–6 nm were deposited by ALD (TFS-200, Beneq, Finland). In detail, the precursor gases are diethyl zinc and de-ionized water. They were pulsed alternately into the reaction chamber with a pulse time of 50 ms and separated by purging steps using argon for 2 s at the reaction temperature of 200 °C [19]. Finally, top Au square electrodes with areas of 1.0×10^{-4} cm^2 were deposited through a metal shallow mask.

The thicknesses of Al_2O_3 layers deposited on the Si wafer as contrast were measured by a spectroscopic ellipsometry system (GES-5E, SOPRA, Courbevoie, France). The film structure was analyzed by the X-ray diffraction (XRD) (Bruker D8 Advance) in a θ-2θ scanning mode with Cu K_α radiation as well as cross-sectional scanning electron microscopy (SEM, Sigma HD, Zeiss). To study the domain switching dynamics, several square pulses with a rising time of 10 ns were applied to top electrodes by using a single-channel Agilent 8114A pulse generator, where bottom electrodes were grounded. In the circuit, the domain switching current (I_{sw}) across in-series internal resistors of all instruments with the total resistance was monitored using a LeCroy HDO6054 oscilloscope. The values of both output resistance of the pulse generator R_W and the input resistance of the oscilloscope R_O are 50 Ω, respectively.

Results and Discussion

Figure 1a shows the XRD result of the LN thin film on a Pt/Cr/SiO_2/LN substrate. The film has strong (00 l) reflections indexed in the rhombohedral phase symmetry. In addition, there are also some diffraction peaks of Pt and Cr films marked in Fig. 1a. The absence of any other peaks confirms the high crystallinity of the LN film without phase impurity. The cross-sectional SEM image of the sample shown in Fig. 1b demonstrates the clear interface structure with LN, Pt, Cr, and SiO_2 stacking layers.

In order to study the domain switching kinetic mechanism, two types of pulse voltage modes are designed as clearly shown in Fig. 2a and b [11]. Type I is configured as double pulses in opposite polarities with the time interval of 5 s. The first pulse is applied to switch the upward polarization state pointing to the top electrode and the second one can switch the downward polarization. However, limited by programming time of a single-channel pulse generation, the minimum time interval is too long

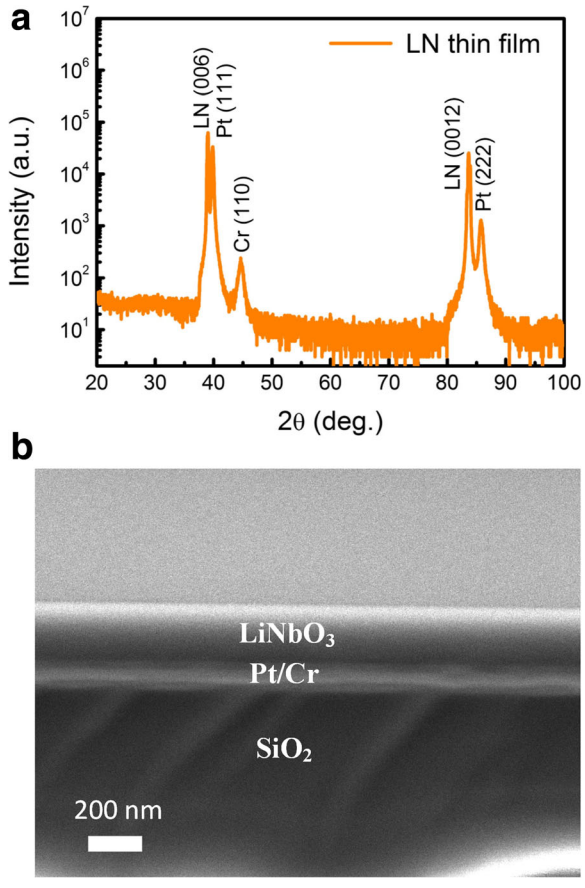

Fig. 1 **a** The XRD pattern and **b** cross-section SEM image of the Z-cut 200-nm-thick LN/Pt/Cr/SiO_2/LN film

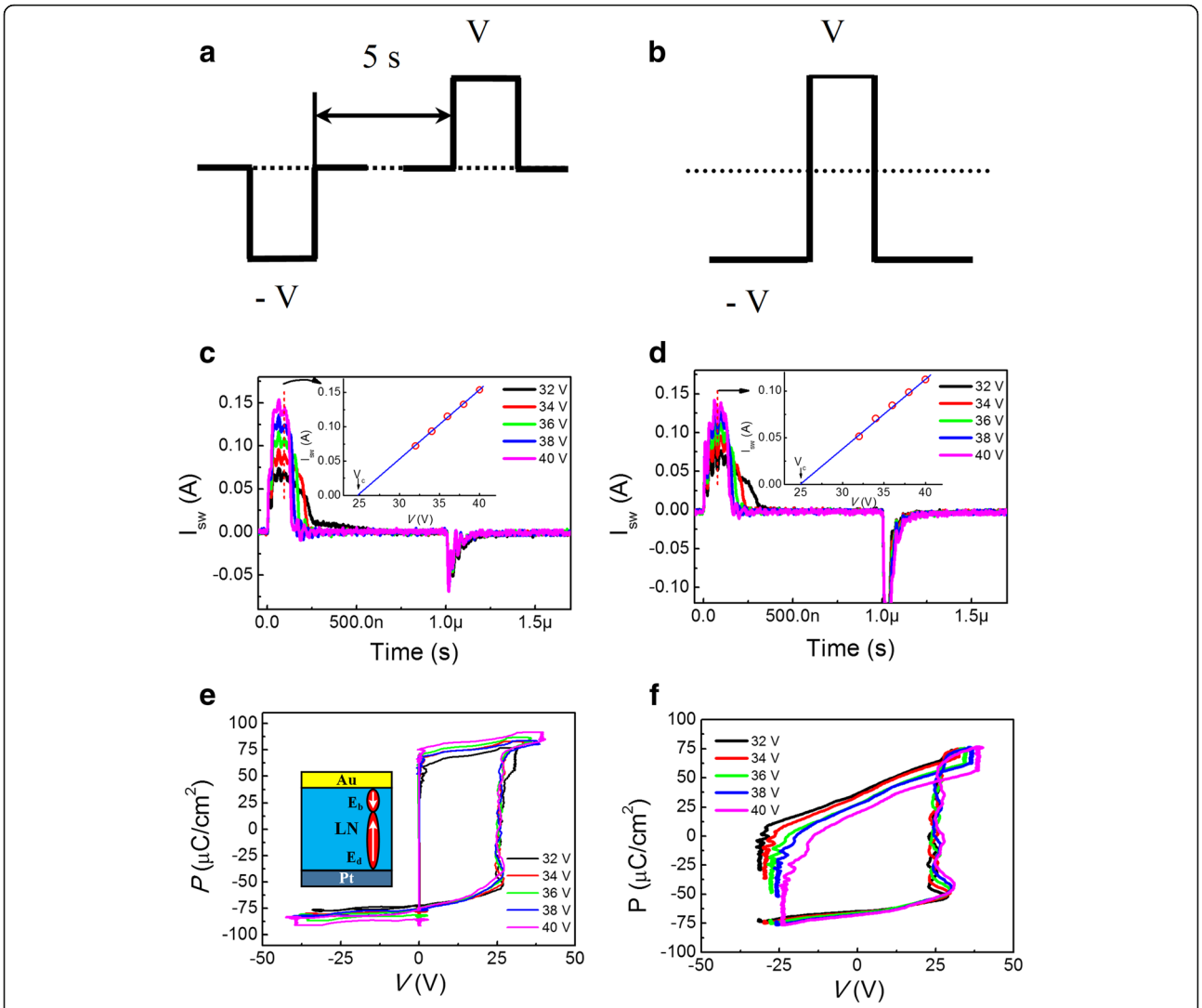

Fig. 2 The sketch of the two sequence pulse voltage modes with **a** type I (double pulses in two opposite polarities) and **b** type II (a single switching pulse overlapping a negative DC bias). Domain switching current transients under different *V* applied to a virgin sample in **c** type I and **d** type II modes, where the insets show the linear fit of the dependence of the plateaus of domain switching current on *V*. *P-V* hysteresis loops under different *V* transferred from domain switching current transients in **e** type I and **f** type II. Schematic diagram of the Au/LN/Pt structure and the directions of the built-in electric field E_b and depolarization field E_d in the inset of **e**

to catch the domain switching current transient invoked by the second pulse, due to the preferred domain orientation. To catch the domain switching current transient, a single pulse overlapping a negative baseline DC bias is proposed in type II, where the initial negative DC bias can switch the upward polarization state and the positive pulse sets the domain downward. Here, the width of the two type pulses is set to1 μs.

Figure 2c and d show the domain switching current transients versus time (*t*) of Au/LN/Pt structure sample under various applied voltages (*V*) in type I and type II modes, respectively. The plateaus of domain switching current transients are observed that narrow in width but increase in height with *V* increasing after the initial capacitor charging current at 30 ns. The height of plateau in two modes both shows a linear relationship with the increase of *V* and the results are summarized in the insets by the solid-line fitting of the data [11, 13]. The coercive voltage (V_c) value in the two modes can be derived to about 24.7 V from the line interception with the voltage axis. After the termination of the switching pulse, the capacitor discharging current occurs after 1 μs, which suggests that the preferred domain orientation is the upward polarization state pointing to the top electrode.

P-V hysteresis loops under different applied voltages in two type modes can be transferred directly from the corresponding domain switching current transients in Fig. 2c and d, and the results are shown in Fig. 2e and f,

respectively [11, 20]. A determined forward coercive voltage of about 25 V invariable with V is obtained in the two types pulses. The coercive voltage approaches to V_c extracted from the linear I_{sw}-V plot in the inset of Fig. 2c and d. Unlike the non-doped LN film, the V_c is variable and the value is equal to the maximum applied voltages [10]. For the 5% Mg-doped LN, the defined V_c is invariable with V, as shown in Fig. 2e and f. This is because the Mg doping can generate Li-site metal vacancies and oxygen vacancy-related defects, [21–23] which can trap space charges and effectively shorten the resistance degradation time across the interfacial layers between the film and top/bottom electrodes [11]. Therefore, domain switching currents overlap with capacitor charging currents in acceleration of domain switching speed with a definite V_c, as shown in Fig. 2c and d. However, limited by the pulse generator, the output baseline voltage in type II mode cannot be shift symmetrically when increasing applied pulse voltage over 32 V. Compared to the imprinted loops along the positive voltage axis in Fig. 2e, the symmetrisation of the loops are achieved along the voltage axis in Fig. 2f, different from those in Pt/$LiNbO_3$/Pt structures where the P-V hysteresis loops in either type I or type II are imprinted toward a positive voltage [11]. The reason of the symmetrical P-V loops in Fig. 2f may be attributed to the designed asymmetric electrodes (here Au/Pt). The work function of Au electrode is 5.1 eV, which is slightly smaller than that of Pt (5.65 eV) [24]. There will induce a built-in electric field (E_b) with the direction pointing from the top electrode to the bottom electrode, shown in the inset of Fig. 2e. The depolarization field (E_d) induced by the interfacial passive layers has the opposite direction to E_b. The E_d can switch back the polarization in a very short time after the termination of the switching pulse in type II for the symmetrical electrodes (Pt/Pt) [11]. In our experiment, the E_b can partially screen the E_d and accumulate injected charges in compensation of an internal imprint field, [16] which can slow down the backswitching time. Hence, the switched domain can maintain and backswitching current transient will be captured by type II pulse. However, the time interval of the two pulses with opposite polarities in type I mode is too long. After the first pulse, the trapped injected charges by E_b will be gradually driven out of the film by E_d before the arrival of the second pulse in type I [11]. In order to prove the attribution of built-in electric field to the symmetrisation of the loops, Pt/$LiNbO_3$/Pt symmetrical structure sample was prepared and the imprinted loops along the positive voltage axis were transferred directly from the corresponding domain switching current transients in Additional file 1: Figure S1a at positive pulse with voltages/widths of 30–40 V/500 ns, shown in Additional file 1: Figure S1b.

Figure 3a and b show the domain switching current (I_{sw}) transients versus time (t) of LN and Al_2O_3 (6 nm)/LN samples under different applied voltage (V) in type I mode. After the plateau of domain switching, the switching current I_{sw} decays and is given by: [13]

$$I_{sw} = {I_{sw}}^0 \exp\left(-\frac{t-t_0}{R_L C_i}\right) \quad (t_0 \le t \le t_{sw}) \tag{1}$$

where t_0, t_{sw}, R_L, and C_i are the beginning time of domain switching, the completion time of domain switching, the total resistance of all the in-series resistors in the circuit, and the interfacial non-ferroelectric capacitance, respectively. This describes the charge trapping effect which can be modeled as an interfacial passive layer in series with an ideal ferroelectric layer. ${I_{sw}}^0$ is defined as switching current and is given by:

$${I_{sw}}^0 = \frac{V - V_{fc}}{R_L} \tag{2}$$

During domain switching, the voltage applied on the ferroelectric layer is fixed at the coercive voltage V_{fc}, and the extra voltage (V-V_{fc}) is applied to R_L. R_L also included the circuit parasitic resistance (R_P) and contact resistance (R_C) between the film and electrodes; hence, $R_L = R_O + R_W + R_P + R_C$. The decayed part of the switching current transients versus time can be fitted by Eq. (1). The time constant $R_L C_i$ can be estimated from the slope of the fitted lines. Figure 3c shows ${I_{sw}}^0$-V plots with different Al_2O_3 thicknesses. R_L and V_C were estimated from the slopes and the X-axis intercept of the linear fitted lines. It can be seen that the V_C is increased linearly with increasing the Al_2O_3 thickness d, as shown in Fig. 3d. Here, the C_i values were estimated as the error bounds at each V in Fig. 3e [13]. The results show that C_i value almost kept constant (1.4 ± 0.2) nF with increasing Al_2O_3 layer thickness from 0 to 6 nm.

In order to calculate R_C, the top and bottom electrodes are shorted, which can obtain the R_P (~ 2 Ω) with different applied voltages, shown as the circuit calibration by the opened symbols in Fig. 3c. Therefore, the R_C corresponding to d is calculated and the result is showed in Fig. 3f. R_C increases linearly from 3 ± 2.5 Ω at d = 0 to 55 ± 10 Ω at d = 6 nm. The almost d-independent large C_i values suggest that the Al_2O_3 layer works as a series resistor during domain switching. This means that the Al_2O_3 tunnel switch was switched on during FE switching.

In order to obtain the total capacitance of the bilayer during FE nonswitching, the switching (P_{sw}) and nonswitching (P_{nsw}) polarizations vesus V with d increased from 0 to 6 nm under pulses in type I mode are measured and the result are showed in Fig. 4a. The purpose of choosing the type I pulse is to obtain the curve of P_{nsw}-V when the direction of the applied voltage is

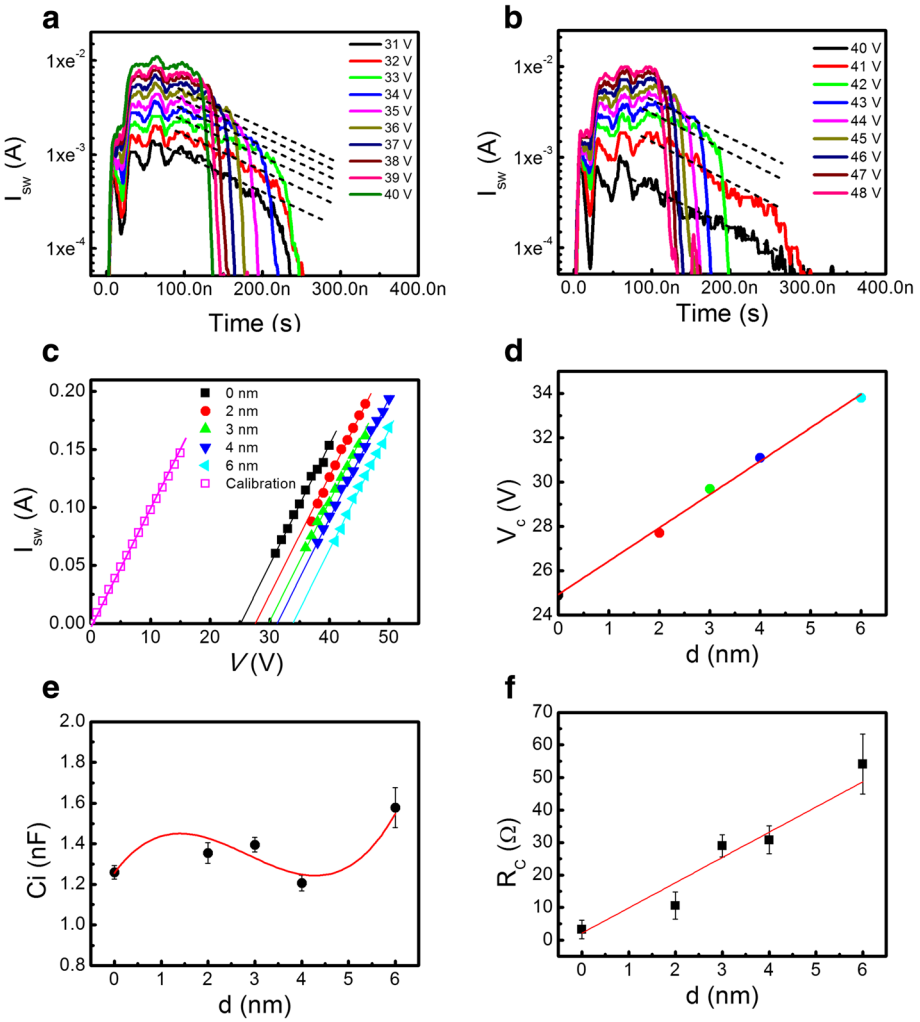

Fig. 3 **a**, **b** I_{sw}-t dependences in type I under different V applied to the Al_2O_3/LN bilayer with the Al_2O_3 thickness $d = 0$ and 6 nm, respectively, fitted by a series of parallel dotted lines to Eq. (1). **c** The plateaus of domain switching current as a function of the applied voltage with different Al_2O_3 layer thicknesses, where the solid lines show the best fit of the data to Eq. (2). **d** The Al_2O_3-layer-thickness d dependence of the coercive voltage (V_c) extracted from **c**. **e**, **f** The extracted interfacial capacitance C_i and contact resistance R_C as functions of the Al_2O_3 layer thickness d

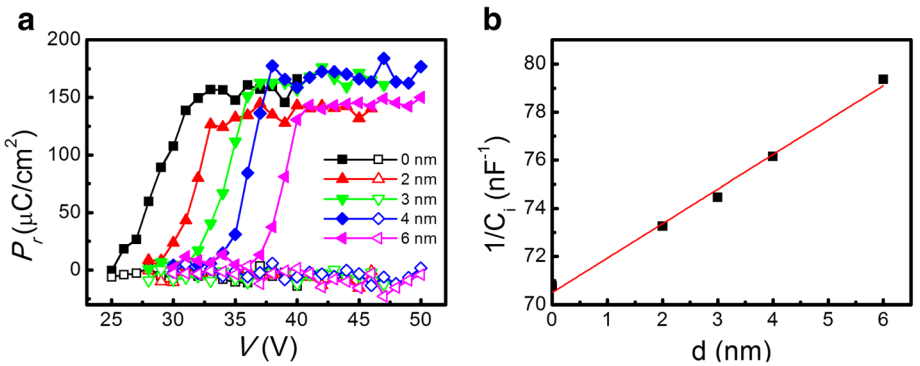

Fig. 4 **a** The switching (P_{sw}) and nonswitching (P_{nsw}) polarizations versus V with d increased from 0 to 6 nm under pulses in type I mode. **b** The Al_2O_3-layer-thickness d dependence of $1/C_{tot}$ measured by an impedance analyzer at 100 kHz

consistent with the polarization orientation, from which the total capacitance (C_{tot}) of the bilayer can be calculated from the relation, $C_{tot} = S{\cdot}dP_{nsw}/dV$, where S is the electrode area. It can totally exclude the charge effects by FE switching in the type I pulse mode, but using the type II mode cannot achieve this effect with the negative switching polarization, which can switch back the polarization involved with the charges injection. The difference between P_{sw} and P_{nsw} is 2Pr, as shown in Fig. 4a. It has small change with d from 0 to 6 nm, whereas the P_{nsw} (open symbols) signals are too weak to be monitored by an oscilloscope. To prove the Al_2O_3 tunnel switch layer working as a dielectric capacitor, the direct C_{tot} measurements using a low-frequency impedance analyzer at 100 kHz with no additional DC bias were carried out and their results are shown in Fig. 4b, which can be fitted by Eq. (3):

$$\frac{1}{C_{tot}} = \frac{1}{C_f} + \frac{d}{\varepsilon_0 \varepsilon_{Al} S} \tag{3}$$

where ε_{Al} is the dielectric constant of the Al_2O_3 layer and ε_0 is the vacuum permittivity of free space. C_f and S represent the capacitance of the ferroelectric layer and the electrode area, respectively. Figure 4b shows the linear $1/C_{tot}$ versus d plot, which suggests that the Al_2O_3 layer becomes a highly insulating dielectric film under nonswitching situation or post-switching. It can be derived that $C_f \approx 14$ pF and $\varepsilon_{Al} \approx 7.9$ from Eq. (3). Therefore, the interposed thin Al_2O_3 layer is proved as a dielectric capacitor. During FE nonswitching as well as after FE switching, the Al_2O_3 tunnel switch closes as an insulator.

Figures 5 show schematic diagrams of the Al_2O_3/LN bilayer structure switched in type I or type II mode. Figure 5a sketches the equivalent on-off circuit of the in-series resistors and capacitors for the Al_2O_3 tunnel switch. In the initial state, as shown in Fig. 5b, the preferred polarization orientation is the upward polarization state pointing to the top electrode. The built-in electric field induced by the asymmetric electrodes directs from Au electrode to Pt electrode. When applying the polarization voltage, the FE switching occurs. It is understood that the voltage is applied inversely proportional to the capacitance in the circuit. In Al_2O_3/LN bilayer structure, during the FE switching, the LN layer has a large capacitance. Therefore, most of the external applied voltage applies on the Al_2O_3 layer. Ultrathin Al_2O_3 layer is injected by electrode charge. It switches on as a resistor when the applied voltage exceeds the Al_2O_3 tunneling threshold, as shown in Fig. 5c. After the completion of FE switching or for the case of a nonswitching situation, the capacitance of LN layer is very small and the applied voltage on Al_2O_3 decreases lower than the tunneling threshold voltage. At this moment, the Al_2O_3 layer plays as an insulator and switches off, as shown in Fig. 5d.

Figure 6 shows the cycling number dependences of switched polarizations in Al_2O_3/LN bilayer structure with the thickness of Al_2O_3 ranging from 0 to 6 nm in type I mode. The width of pulses is 1000 ns with a periodicity of 0.5 s. It can be clearly seen that the fatigue endurance of the Al_2O_3/LN bilayer structure is improved gradually with increasing the Al_2O_3 thickness with over 10^4 cycles of pulse stressing. The fatigue property in type II mode is similar to the result in type I mode, which was showed in Additional file 1: Figure S2 of supporting

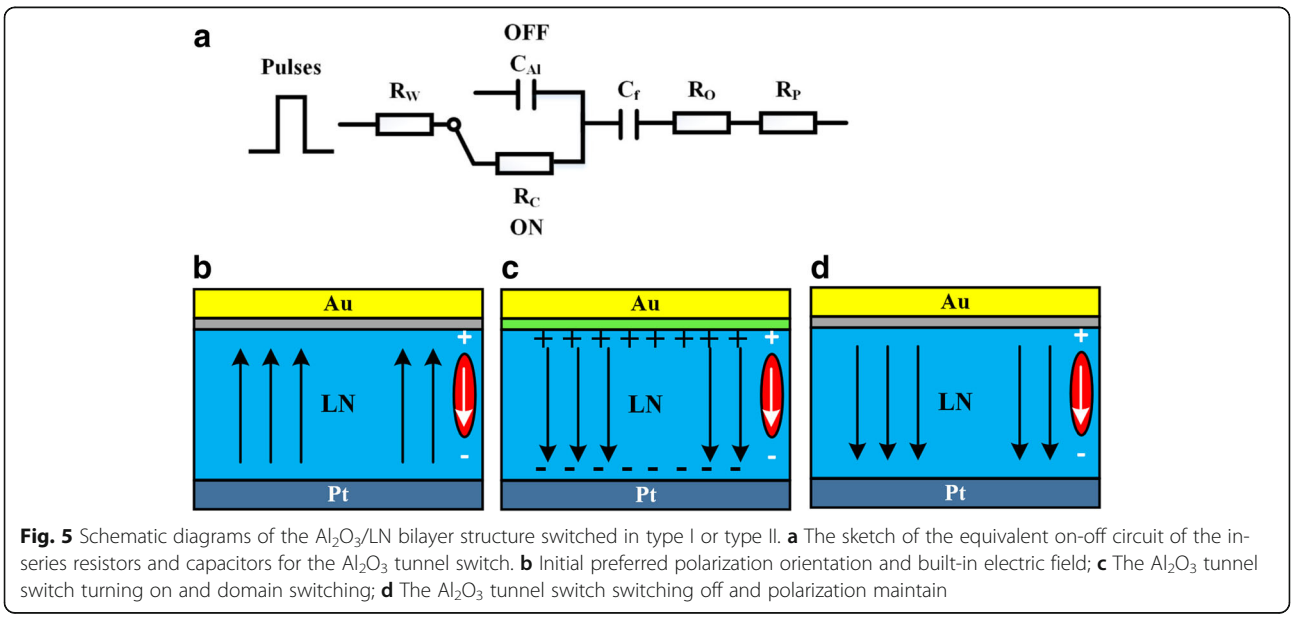

Fig. 5 Schematic diagrams of the Al_2O_3/LN bilayer structure switched in type I or type II. **a** The sketch of the equivalent on-off circuit of the in-series resistors and capacitors for the Al_2O_3 tunnel switch. **b** Initial preferred polarization orientation and built-in electric field; **c** The Al_2O_3 tunnel switch turning on and domain switching; **d** The Al_2O_3 tunnel switch switching off and polarization maintain

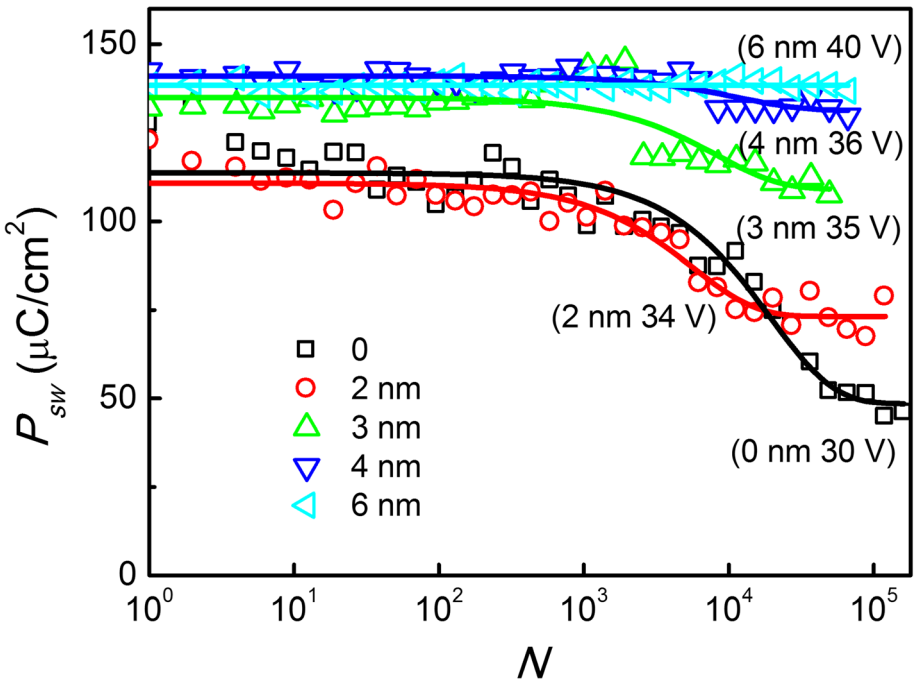

Fig. 6 Cycling number dependences of switched polarizations in Al_2O_3/LN bilayer structure with the thickness of Al_2O_3 ranging from 0 to 6 nm under over 10^4 cycles of pulse stressing. The width of pulses is 1000 ns in the periodicity of 0.5 s

information. Unfortunately, the electrical breakdown would occur easily in the type II mode after longtime DC voltage applied with near 10^4 cycles of pulse stressing. The data can be fitted using the model for the coexistence of domain-wall pinning and depinning within each cycle, as shown by the solid lines in Fig. 6, where the fatigue physics was attributed to by-electrode charge injection [13]. When the Al_2O_3 layer inserted between the Au electrode and LN layer, it can block the by-electrode injection charge path and improve the fatigue endurance. However, in the bilayer structure, some issues should be further considered. For example, with increasing the thicknesses of Al_2O_3 from 0 to 6 nm, the coercive voltage enlarged from near 25 to 34 V, which can be reduced by improving the quality of the Al_2O_3 layer. Actually, a few atomic layers of Al_2O_3 with high quality or less defect can effectively block the charges injected by electrodes, which is confirmed elsewhere by optimizing atomic layer deposition processing conditions (such as temperature and time) [25].

Recently, ferroelectric domain-wall memories based on the erasable conducting charged domain walls and the non-destructive electrical read-out of the polarization states have been proposed in our following research work [26, 27]. Large conductivity of charged domain walls in lithium niobate single crystals is obtained after domain switching [28, 29]. Therefore, the thinner lithium niobate single crystal thin films on silicon substrates are the promising materials for integrated ferroelectric domain-wall memories and its retention and fatigue endurance properties can be improved by design of Al_2O_3/lithium niobate bilayer.

Conclusions

Two hundred nanometer $LiNbO_3$ single-crystal films with 5% Mg-doping were prepared by ion slicing of surface layers from bulk LN single crystals, and then the ultrathin Al_2O_3 films with thicknesses ranging from 2 to 6 nm as tunnel switch layers were deposited on 5% Mg-doped LN film to form bilayer structures by atomic layer deposition. The symmetrized *P-V* hysteresis loops along the voltage axis are observed under applied pulse voltages in type II mode, which may be attributed to the built-in electric field induced by asymmetric electrodes in Au/$LiNbO_3$/Pt and compensation of the internal imprint field. The domain switching current (I_{sw}) transients and its transferred *P-V* hysteresis loops reveal that the ultrathin Al_2O_3 layer plays as an idea tunnel switch. It turns on during FE switching, but closes during the nonswitching or after FE switching, minimizing the adverse interference with FE switching. Furthermore, the fatigue endurance of the FE capacitor is improved gradually with increasing the tunnel switch layer thicknesses from 2 to 6 nm. The Al_2O_3/LN bilayer structure paves the way to design robust ferroelectric devices in alleviating the fatigue problem by-electrode charge injection.

Additional file

Additional file 1: The imprinted P-V hysteresis loops of Pt/$LiNbO_3$/Pt symmetrical structure sample in type II mode and the fatigue property of Al_2O_3/$LiNbO_3$ bilayer structure in type II mode. (DOCX 144 kb)

Abbreviations

ALD: Atomic layer deposition; CMOS: Complementary metal oxide semiconductor; FE: Ferroelectric; LN: Lithium niobate; SEM: Scanning electron microscopy; XRD: X-ray diffraction

Acknowledgements

This work was supported by the National Natural Science Foundation of China (grant number 61674044), the Basic Research Project of Shanghai Science and Technology Innovation Action (grant number 17JC1400300), the National Key Basic Research Program of China (grant number 2014CB921004), and the Program of Shanghai Subject Chief Scientist (grant number 17XD1400800).

Availability of Data and Materials

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Authors' Contributions

YZ and QHR prepared the materials and draft the manuscript. AQJ, YZ, and JJ designed the work. YZ, XJC, JGY, and QHR carried out the structural analyses and switching current measurements of the samples. AQJ edited the whole manuscript. All authors had read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

Publisher's Note

Received: 28 January 2019 Accepted: 3 April 2019
Published online: 16 April 2019

References

1. Fujiwara T, Takahashi M, Ohama M, Ikushima AJ, Furukawa Y, Kitamura K (1999) Comparison of electro-optic effect between stoichiometric and congruent $LiNbO_3$. Electron Lett 35:499–501
2. Volk TR, Gainutdinov RV, Zhang HH (2017) Domain-wall conduction in AFM-written domain patterns in ion-sliced $LiNbO_3$ films. Appl Phys Lett 110:132905
3. Poberaj G, Hu H, Sohler W, Gunter P (2012) Lithium niobate on insulator (LNOI) for micro-photonic devices. Laser Photonics Rev 6:488–503
4. Cho YS, Fujimoto K, Hiranaga Y, Wagatsuma Y, Onoe A, Terabe K, Kitamura K (2002) Tbit/inch^2 ferroelectric data storage based on scanning nonlinear dielectric microscopy. Appl Phys Lett 81:4401–4403
5. Wang C, Burek MJ, Lin Z, Atikian HA, Venkataraman V, Huang IC, Stark P, Loncar M (2014) Integrated high quality factor lithium niobate microdisk resonators. Opt Express 22:30924–30933
6. Gainutdinov RV, Volk TR, Zhang HH (2015) Domain formation and polarization reversal under atomic force microscopy-tip voltages in ion-sliced $LiNbO_3$ films on SiO_2/$LiNbO_3$ substrates. Appl Phys Lett 107:162903
7. Hu H, Yang J, Gui L, Sohler W (2012) Lithium niobate-on-insulator (LNOI): status and perspectives. Proc SPIE 8431:84311D
8. Wang C, Zhang M, Chen X, Bertrand M, Shams-Ansari A, Chandrasekhar S, Winzer P, Loncar M (2018) Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages. Nature 562:101–104
9. Tanaka S, Park K, Esashi M (2012) Lithium-niobate-based surface acoustic wave oscillator directly integrated with CMOS sustaining amplifier. Ieee T Ultrason Ferr 59:1800–1805
10. Jiang J, Meng XJ, Geng DQ, Jiang AQ (2015) Accelerated domain switching speed in single-crystal $LiNbO_3$ thin films. J Appl Phys 117:104101
11. Zhang Y, Jiang AQ (2018) Low-frequency charge trapping and bistable domain switching in Mg-doped $LiNbO_3$ single crystal films. J Appl Phys 124: 124103
12. Jiang AQ, Lin YY, Tang TA (2007) Unsaturated charge injection at high-frequency fatigue of Pt/Pb $(Zr,Ti)O_3$/Pt thin-film capacitors. Appl Phys Lett 91:082901
13. Jiang AQ, Lee HJ, Hwang CS, Scott JF (2012) Sub-picosecond processes of ferroelectric domain switching from field and temperature experiments. Adv Funct Mater 22:192–199
14. Jiang AQ, Lee HJ, Kim GH, Hwang CS (2009) The inlaid Al_2O_3 tunnel switch for ultrathin ferroelectric films. Adv Mater 21:2870–2875
15. Lee HJ, Kim GH, Park MH, Jiang AQ, Hwang CS (2010) Polarization reversal behavior in the Pt/Pb $(Zr,Ti)O_3$/Pt and Pt/Al_2O_3/Pb $(Zr,Ti)O_3$/Pt capacitors for different reversal directions. Appl Phys Lett 96:212902
16. Lee HJ, Park MH, Kim YJ, Hwang CS, Kim JH, Funakubo H, Ishiwara H (2011) Improved ferroelectric property of very thin Mn-doped $BiFeO_3$ films by an inlaid Al_2O_3 tunnel switch. J Appl Phys 10:074111
17. Levy M, Osgood RM, Liu R, Cross LE, Cargill GS, Kumar A, Bakhru H (1998) Fabrication of single-crystal lithium niobate films by crystal ion slicing. Appl Phys Lett 73:2293–2295
18. Han HP, Cai LT, Xiang BX, Jiang YP, Hu H (2015) Lithium-rich vapor transport equilibration in single-crystal lithium niobate thin film at low temperature. Opt Mater Express 5:2634–2641
19. Ren QH, Zhang Y, Lu HL, Chen HY, Zhang Y, Li DH, Liu WJ, Ding SJ, Jiang AQ, Zhang DW (2016) Surface-plasmon mediated photoluminescence enhancement of Pt-coated ZnO nanowires by inserting an atomic-layer-deposited Al_2O_3 spacer layer. Nanotechnology 27:165705
20. Jiang AQ, Liu XB, Zhang Q (2011) Nanosecond-range imprint and retention characterized from polarization-voltage hysteresis loops in insulating or leaky ferroelectric thin films. Appl Phys Lett 99:142905
21. Nakamura M, Higuchi S, Takekawa S, Terabe K, Furukawa Y, Kitamura K (2002) Optical damage resistance and refractive indices in near-stoichiometric MgO-doped LiNbO3. Jpn J Appl Phys 41:L49–L51
22. Furukawa Y, Kitamura K, Takekawa S, Miyamoto A, Terao M, Suda N (2000) Photorefraction in LiNbO3 as a function of [Li]/[Nb] and MgO concentrations. Appl Phys Lett 77:2494–2496
23. Furukawa Y, Kitamura K, Takekawa S, Niwa K, Yajima Y, Iyi N, Mnushkina I, Guggenheim P, Martin JM (2000) The correlation of MgO-doped near-stoichiometric $LiNbO_3$ composition to the defect structure. J Cryst Growth 211:230–236
24. Pintilie L, Vrejoiu I, Hesse D, Alexe M (2008) The influence of the top-contact metal on the ferroelectric properties of epitaxial ferroelectric Pb $(Zr_{0.2}Ti_{0.8})O_3$ thin films. J Appl Phys 104:114101
25. Wilt J, Sakidja R, Goul R, Wu JZ (2017) Effect of an interfacial layer on electron tunneling through atomically thin Al_2O_3 tunnel barriers. ACS Appl Mater Interfaces 9:37468–37475
26. Jiang J, Bai ZL, Chen ZH, He L, Zhang DW, Zhang QH, Shi JA, Park MH, Scott JF, Hwang CS, Jiang AQ (2018) Temporary formation of highly conducting domain walls for non-destructive read-out of ferroelectric domain-wall resistance switching memories. Nat Mater 17:49–56
27. Ma J, Ma J, Zhang QH, Peng RC, Wang J, Liu C, Wang M, Li N, Chen MF, Cheng XX, Gao P, Gu L, Chen LQ, Yu P, Zhang JX, Nan CW (2018) Controllable conductive readout in self-assembled, topologically confined ferroelectric domain walls. Nat Nanotechnol 13:947–952
28. Werner CS, Herr SJ, Buse K, Sturman B, Soergel E, Razzaghi C, Breunig I (2017) Large and accessible conductivity of charged domain walls in lithium niobate. Sci Rep 7:9862
29. Godau C, Kampfe T, Thiessen A, Eng LM, Haussmann A (2017) Enhancing the domain wall conductivity in lithium niobate single crystals. ACS Nano 11:4816–4824