Nanoscale Research Letters

NANO EXPRESS Open Access

Enhanced Si Passivation and PERC Solar Cell Efficiency by Atomic Layer Deposited Aluminum Oxide with Two-step Post Annealing

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Abstract

In this study, aluminum oxide (Al_2O_3) films were prepared by a spatial atomic layer deposition using deionized water and trimethylaluminum, followed by oxygen (O_2), forming gas (FG), or two-step annealing. Minority carrier lifetime of the samples was measured by Sinton WCT-120. Field-effect passivation and chemical passivation were evaluated by fixed oxide charge (Q_f) and interface defect density (D_{it}), respectively, using capacitance-voltage measurement. The results show that O_2 annealing gives a high Q_f of -3.9×10^{12} cm^{-2}, whereas FG annealing leads to excellent Si interface hydrogenation with a low D_{it} of 3.7×10^{11} eV^{-1} cm^{-2}. Based on the consideration of the best field-effect passivation brought by oxygen annealing and the best chemical passivation brought by forming gas, the two-step annealing process was optimized. It is verified that the Al_2O_3 film annealed sequentially in oxygen and then in forming gas exhibits a high Q_f (2.4×10^{12} cm^{-2}) and a low D_{it} (3.1×10^{11} eV^{-1} cm^{-2}), yielding the best minority carrier lifetime of 1097 μs. The SiN_x/Al_2O_3 passivation stack with two-step annealing has a lifetime of 2072 μs, close to the intrinsic lifetime limit. Finally, the passivated emitter and rear cell conversion efficiency was improved from 21.61% by using an industry annealing process to 21.97% by using the two-step annealing process.

Keywords: Passivated emitter and rear cell, Aluminum oxide, Atomic layer deposition, Passivation, Two-step annealing

Introduction

Passivated emitter and rear cells (PERCs) have emerged as a promising technology for both high efficiency and competitive cost in recent years. The most difference between the PERC and the traditional full-aluminum back surface field silicon solar cell is rear passivation of wafers. Considerable efforts have been made in order to improve wafer surface passivation. Minority carrier lifetimes of 0.8–8 ms have been reported for p-type floating zone wafers passivated by vacuum [1–4] or spatial atomic layer deposition (ALD) aluminum oxide (Al_2O_3) [5–7]. The passivation quality for p-type Czochralski wafers is lower, in the range of 0.1–2 ms [8, 9]. Spatial ALD Al_2O_3 have been extensively studied and applied to the industry in recent years due to their higher deposition rate (0.03–1.2 nm/s) compared to that of a conventional vacuum-type ALD (< 0.03 nm/s) [10, 11]. Trimethylaluminum (TMA) and H_2O are the most widely used precursors as they are inexpensively volatile liquid and easy to handle. Some research groups use other precursors such as $AlCl_3$ or O_3 [12–14]. Al_2O_3 is currently considered to be the best passivation material due to its field effect and chemical passivation [15]. It is found that the H_2O-based ALD process mostly leads to a silicon oxide (SiO_x) layer at the Al_2O_3/Si interface, and this interfacial layer can appear after deposition or annealing [16]. Post annealing for Al_2O_3 films in either nitrogen or forming gas (FG) has been shown to significantly increase the wafer lifetime [12, 17]. Hydrogen in FG or Al_2O_3 cause hydrogenation of Si interface during

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annealing. The annealing temperature is typically below 500 °C, beyond which dehydrogenation occurs. However, other annealing processes for further improving passivation quality are rarely reported.

In this study, Al_2O_3 films are prepared on Si by spatial ALD with TMA and H_2O as precursors. Effects of oxygen (O_2) and FG post annealing on passivation of Si wafers are investigated and analyzed. A two-step annealing as a combination of O_2 and FG annealing is proposed and demonstrates a higher wafer lifetime compared to the individual gas annealing process. Finally, photovoltaic performance of PERCs fabricated with industry standard, O_2, FG, and two-step annealing are presented.

Methods

P-type (100) Czochralski silicon wafers with resistivity of 1 Ω-cm and thickness of 200 μm were used as substrates. The wafers were cleaned using standard RCA process, followed by a 30-s HF dip to remove native oxide on the wafers. The Al_2O_3 thin films with a thickness of 18 nm were deposited using a spatial ALD system, with H_2O and TMA as oxidant and aluminum source, respectively. The gap between gas injection heads and the movable substrate holder was about 1 mm. The detailed deposition parameters are summarized in Table 1. The temperature of the pipes was 70 °C to prevent condensation of precursors. Some of the wafers were passivated with silicon nitride (SiN_x, 120 nm)/Al_2O_3 (18 nm) stack, where the SiN_x layer was deposited using a 13.56-MHz inductively coupled plasma vapor deposition at 120 °C with a gas mixture of ammonia (NH_3) and tetramethylsilane (TMS). Other parameters for SiN_x deposition are listed in Table 2. The oxygen, FG, or two-step annealing process was performed on the samples, and the annealing parameters are listed in Table 3. The lifetime of the samples was measured by Sinton WCT-120. The capacitance-voltage (*C-V*) measurement was carried out on metal-oxide-semiconductor (MOS) samples by a capacitor meter (HP 4284a) at 1 MHz at room temperature. For MOS fabrication, the wafers were deposited with an 18-nm-thick Al_2O_3 layer and annealed. Aluminum films with a thickness of 500 nm were evaporated on both sides of the samples as electrodes. The area of the MOS samples was 1 mm^2. The cross-sectional images of the samples were obtained using a transmission electron microscope (TEM). For PERC fabrication, a schematic of the devices is shown in Fig. 1, where the ALD passivation is only on the rear side. The wafers were textured using alkaline solution to generate random pyramids. Emitter was formed by $POCl_3$ diffusion in a standard tube thermal furnace with a sheet resistance of 100 ohms/square. A SiN_x of 85 nm thickness was deposited on the front side of the wafer as an antireflective layer by inductively coupled plasma vapor deposition (ICPCVD). The back side of the wafer was polished by KOH solution for 3 min at 70 °C. The Al_2O_3 films of 18 nm in thickness were deposited using spatial ALD. An ICPCVD SiN_x of 120 nm in thickness was deposited on Al_2O_3. The samples were annealed with different annealing processes. The rear local openings with a diameter of 40 μm and a pitch of 260 μm were created by 532-nm laser scribing. Finally, a silver grid was screen printed on the front and aluminum on the rear dielectric, followed by co-firing at a peak temperature of 850 °C. The current density-voltage (*J-V*) curves were measured by a dual light source-type solar simulator (Wacom Co., Japan) using both xenon lamp and halogen lamp with a calibrated class A AM 1.5G simulated light spectrum.

Table 1 Deposition parameters of the ALD Al_2O_3 layer

Parameter	Value
Substrate temperature (°C)	150
TMA bubbler temperature (°C)	17.5
H_2O bubbler temperature (°C)	30
Pressure (Torr)	760
TMA flow rate (sccm)	200
H_2O flow rate (sccm)	500
Thickness (nm)	15

Table 2 Deposition parameters of the SiN_x layer

Parameter	Value
Substrate temperature (°C)	120
Pressure (Torr)	0.005
TMS flow rate (sccm)	15
NH_3 flow rate (sccm)	45
Power (W)	1200
Thickness (nm)	120

Results and Discussion

Figure 2a shows the injection-level-dependent minority carrier lifetimes of the Al_2O_3/Si/Al_2O_3 samples without and with different annealing processes. Before annealing, the minority carrier lifetime is low as below 100 μs over the whole injection level range. The lifetime greatly improves after the annealing process as a consequence of chemical passivation and field effect passivation brought

Table 3 Parameters of O_2, FG, and two-step annealing processes

	O_2-600	FG-450	Two-step	
			Step 1	Step 2
Annealing gas	O_2	5% H_2, 95% N_2	O_2	FG
Temperature (°C)	600	450	600	450
Time (min)	20	20	10	10

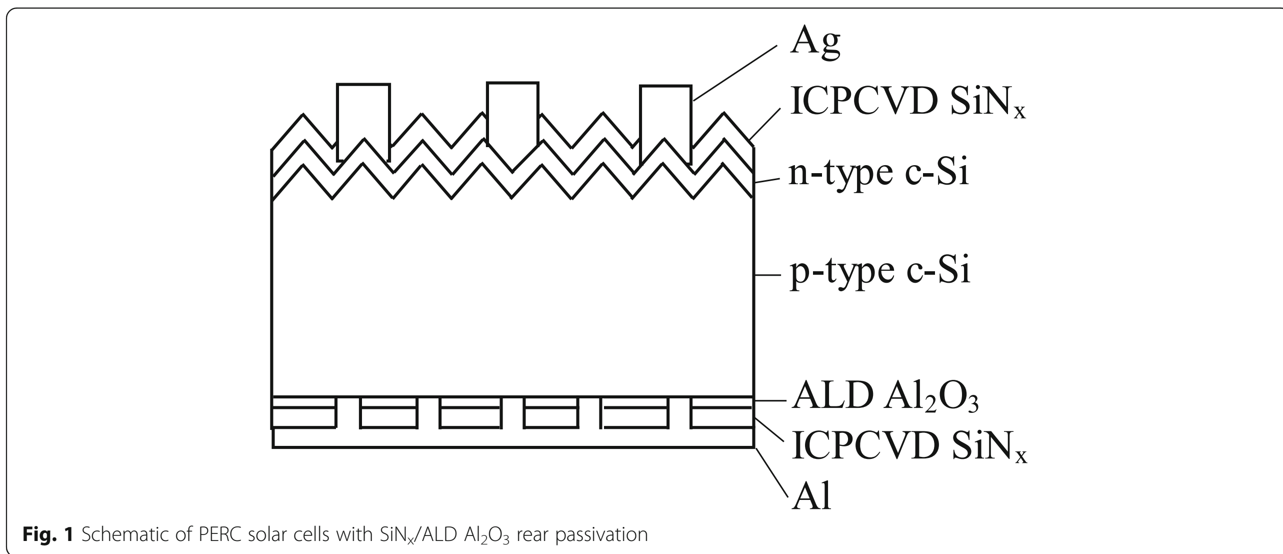

Fig. 1 Schematic of PERC solar cells with SiN_x/ALD Al_2O_3 rear passivation

Fig. 2 **a** Injection-level-dependent minority carrier lifetime. **b** Lifetime at an injection level of 3×10^{15} cm^{-3} for Al_2O_3/Si/Al_2O_3 samples with O_2, FG, and two-step annealing

by annealed Al_2O_3. However, the lifetime values are different in these three annealing conditions, in which oxygen annealing has the lowest curve, FG annealing has the intermediate, and the two-step annealing has the highest. The lifetime values at the injection level of $3 \times 10^{15}\ cm^{-3}$ are extracted as shown in Fig. 2b. The O_2-, FG-, and two-step-annealed samples have lifetimes of 818, 934, and 1098 μs, respectively. Note that the two-step annealing can obtain the highest lifetime only with the annealing sequence of the first step in O_2 and the second step in FG. The reverse sequence results in a lifetime similar to that of the sample with O_2 annealing alone. This might be because if FG annealing was performed first, the following O_2 annealing might cause dehydrogenation. Niwano et al. reported that for a wafer terminated by Si–H or Si–H_2 bonds, exposure to oxygen results in the replacement of the hydrogen bonds with the Si–O bonds [18].

As overall passivation is governed by field effect and chemical passivation, the *C-V* measurement is helpful to clarify which passivation dominates in the cases of O_2, FG, and two-step annealing. Figure 3a shows the normalized *C-V* curves for the samples without and with different annealing processes. The slope magnitude of the curves in the depletion region can be used as an indicator of interface defect density (D_{it}), since the existence of interface traps causes *C-V* curve stretch-out [19]. The two-step annealing gives the largest slope among the others, and thus the lowest D_{it} is expected. To gain further information, the values of fixed oxide charge density (Q_f) and D_{it} are extracted from the *C-V* curves as plotted in Fig. 3b. The Q_f is helpful for evaluating the field effect passivation and is calculated by [20]

$$Q_f = \frac{C_{ox}(W_{ms} - V_{fb})}{q\,A} \quad (1)$$

where C_{ox} is the accumulation oxide capacitance, W_{ms} is the work function difference between semiconductor and electrode (in this case − 0.9 V), V_{fb} is the flat band voltage, q is the electron charge, and A is the area of the MOS devices. The Q_f is $-3.2 \times 10^{-11}\ cm^{-2}$ for the as-deposited sample. Q_f at this level leads to weak field effect passivation [21]. All the annealed samples elevate Q_f to the level of $10^{12}\ cm^{-2}$. It is seen that the O_2 annealing gives the highest Q_f of $3.9 \times 10^{12}\ cm^{-2}$, the two-step annealing gives the intermediate Q_f, and the

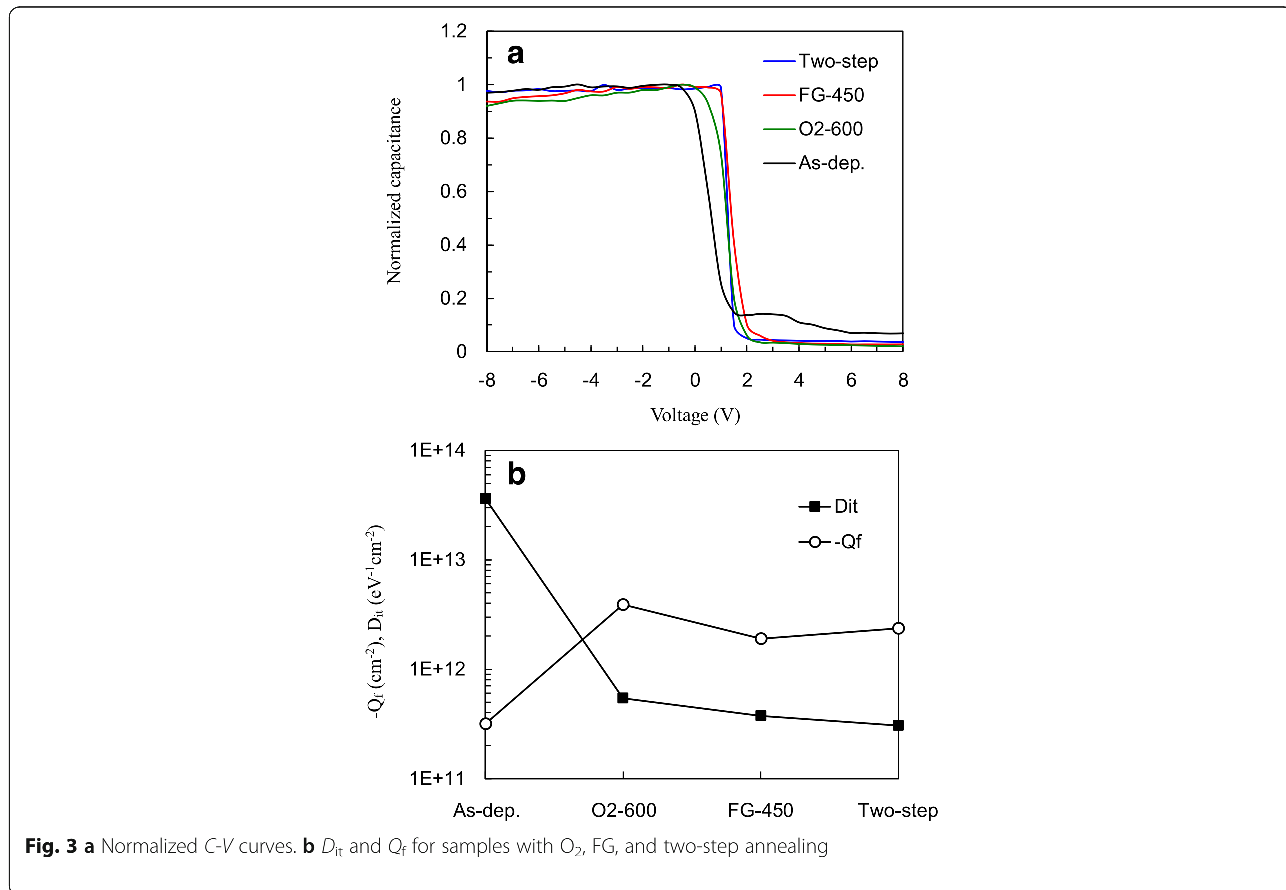

Fig. 3 **a** Normalized *C-V* curves. **b** D_{it} and Q_f for samples with O_2, FG, and two-step annealing

FG annealing gives the lowest Q_f. On the other hand, D_{it} value estimated by the Terman method [22] is also shown to evaluate chemical passivation. The as-deposited sample has a D_{it} of more than 10^{13} eV^{-1} cm^{-2}. It reduces to 5.4×10^{11} eV^{-1} cm^{-2} for O_2 annealing, 3.7×10^{11} eV^{-1} cm^{-2} for FG annealing, and 3.1×10^{11} eV^{-1} cm^{-2} for two-step annealing. Thus, by comparing O_2 and FG annealing, it is found that O_2 annealing has the better field effect passivation, whereas FG has the better chemical passivation. The former might be linked to the interfacial SiO_x growth. Unlike FG annealing which is performed at a relatively low temperature and with lack of oxygen, O_2 annealing is expected to have an improved SiO_x interfacial layer growth. This could increase the possibility of Al substitution for Si at the Al_2O_3/SiO_2 interface, which is regarded to be one possible origin of negative fixed charges [23]. Considering the two-step annealing, the intermediate Q_f is reasonable as a combination of O_2 and FG annealing. However, its D_{it} value is lower than that of the FG annealing. This is explained by the additional contribution by the higher quality of the interfacial oxide layer due to the first-step O_2 annealing. Some studies also reported that a denser SiO_x results in a better passivation [24]. The lower D_{it} in two-step annealing sample can also be attributed to the hydrogenation improvement of silicon surface induced by the hydrogen in Al_2O_3 film.

Figure 4 shows the cross-sectional TEM images of the samples without and with different annealing processes. Before annealing, a SiO_x interfacial layer between Si and Al_2O_3 is observed although the interface is not clear. This might be because H_2O was used in the first-half ALD cycle. For O_2 annealing, the interfacial layer thickness increases to 5.6 nm, due to annealing at a high temperature (600 °C) and in oxygen ambient. It has been reported that oxygen has a very small diffusion coefficient in Al_2O_3 (~ 10^{-38} cm^{-1} at 600 °C) [25], and thus, it is unlikely for oxygen to diffuse through the Al_2O_3 layer to reach the Si interface. Instead, ambient oxygen interchanges with the oxygen in Al_2O_3, creating a mobile oxygen that can repeat the interchange process in the deeper Al_2O_3 region until the oxygen reaches the Si interface [26]. The sample annealed in FG shows a clearer interface with a very thin SiO_x interfacial layer of

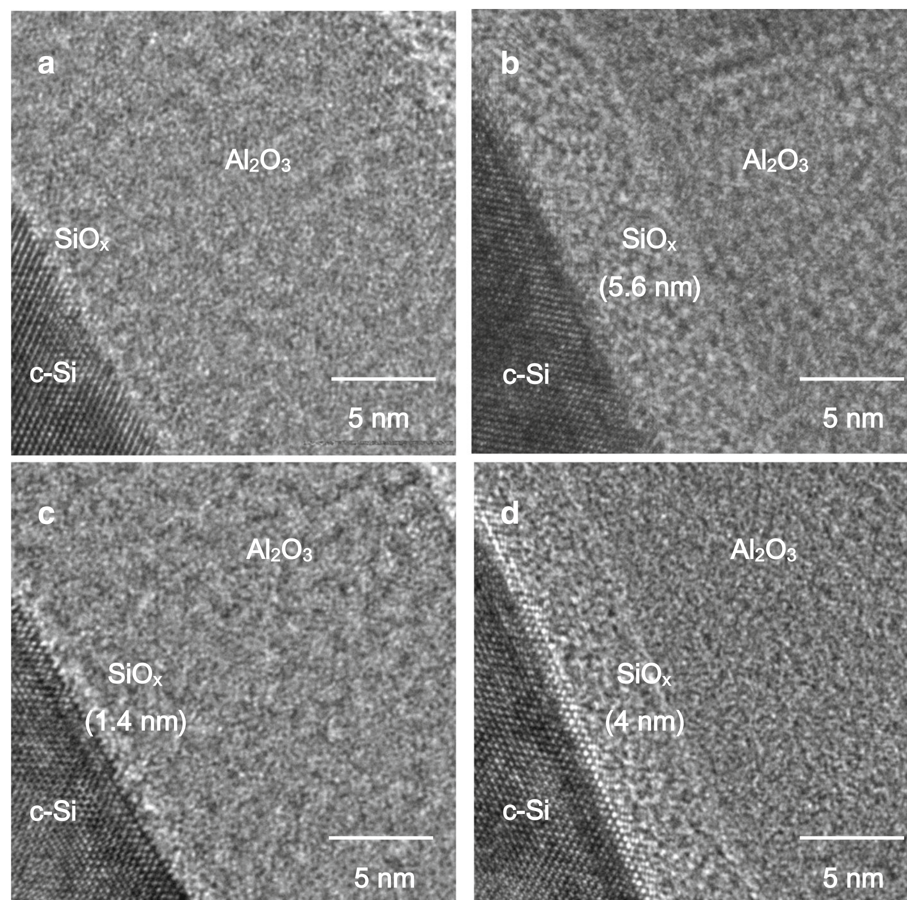

Fig. 4 Cross-sectional TEM images for samples **a** without annealing and with **b** O_2, **c** FG, and **d** two-step annealing

1.4 nm, which is similar to other research groups performing the annealing process in N_2 or FG [16]. This evidences that FG annealing limits the interfacial layer growth. The two-step annealing shows an intermediate SiO_x interfacial layer thickness of about 4 nm, as a consequence of the reduced time of the O_2 annealing.

Figure 5a shows the injection level-dependent minority carrier lifetime of the SiN_x/Al_2O_3-passivated wafers without and with different annealing processes. The lifetimes at the injection level of 3×10^{15} cm^{-3} are 1569, 1579, and 2072 μs for O_2, FG, and two-step annealing, respectively. The improvements are related to that the plasma chemical vapor-deposited SiN_x films may contain certain amounts of hydrogen depending on the deposition process parameters. During the annealing process, some of the hydrogen would move towards the Si interface, and this enhances the Si interface hydrogenation [27]. As reported in literature [6, 28–30], the lifetime of SiN_x/Al_2O_3-passivated p-type CZ wafers is in the range of 0.1–2 ms. The optimal temperature of post-deposition annealing either in nitrogen or in FG is around 400–500 °C. In this work, the SiN_x/Al_2O_3-passivated CZ wafer annealed in FG shows a lifetime of 1579 μs and an optimal annealing temperature of 450 °C, which are in accordance with the reported values. However, this optimal temperature is limited by the hydrogenation of the silicon interface. From the viewpoint of the silicon oxide interfacial layer, this layer might have different optimal temperature as high temperatures generally improve qualities of silicon oxide films. Thus, the two-step annealing could optimize both of the interfacial oxide quality and silicon interface hydrogenation, and leads to a higher lifetime of 2072 μs compared to the case of forming gas single-step annealing. To investigate the reproducibility, 50 samples with two-step annealing were prepared, and their minority carrier lifetime is shown in Fig. 5b. The samples have lifetime values ranging between 1939 and 2224 μs. The average value is 2075 μs, and the error is within ± 7%. The intrinsic lifetime limit of the wafer used in this study is about 2300 μs, calculated by using the Richter parameterization [31]. Thus, the two-step annealing yields a lifetime close to the

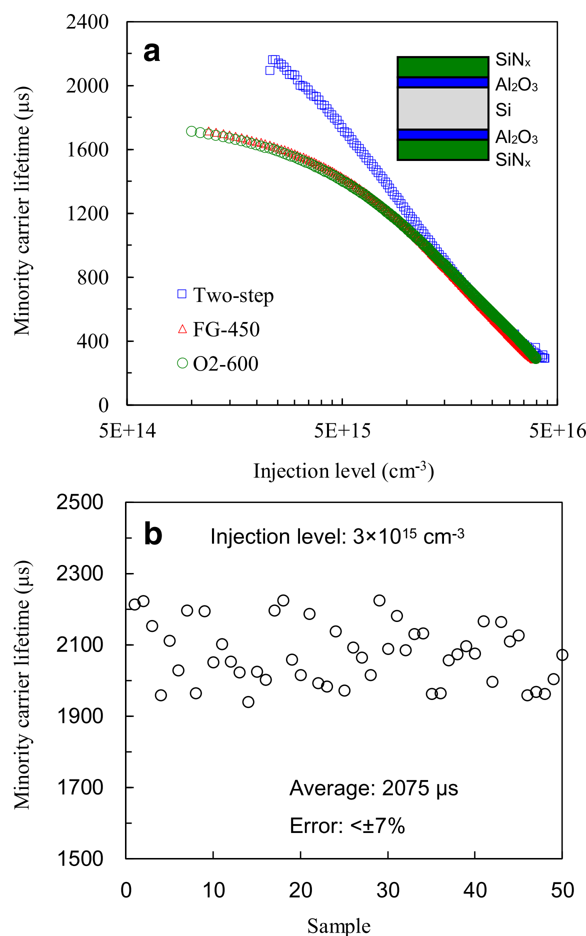

Fig. 5 **a** Injection-level-dependent minority carrier lifetime of SiN_x/Al_2O_3-passivated samples with O_2, FG, and two-step annealing. **b** Lifetime at an injection level of 3×10^{15} cm^{-3} for 50 samples with two-step annealing

lifetime limitation and demonstrates excellent interface passivation. For other ALD, a silicon oxide interfacial layer between Al_2O_3/Si is also found, and the two-step annealing should be able to improve the passivation quality of Si wafers. AlO_x/SiN_x is necessary as the silicon nitride not only enhances passivation but also increases rear reflectance and protects AlO_x from a high-temperature cofiring process for PERC fabrication.

Figure 6 shows the implied open-circuit voltage (V_{oc}) for the SiN_x/Al_2O_3-passivated samples with different annealing processes. For p-type wafers and long diffusion lengths, the implied V_{oc} can be written as

$$\text{implied } V_{oc} = \frac{kT}{q} \ln\left(\frac{\Delta n\,(N_A + \Delta n)}{{n_i}^2}\right) \tag{2}$$

where k is the Boltzmann constant, T is the absolute temperature, n_i is the intrinsic carrier concentration, N_A is the acceptor concentration, and Δn is the excess carrier concentration measured at one-sun light intensity by the WCT-120 Sinton lifetime tester. It can be seen that the O_2- and FG-annealed samples have similar implied V_{oc} values, which are 696 and 697 mV, respectively. The two-step annealing has an implied V_{oc} of 706 mV.

Figure 7 shows the *J-V* characteristics and photovoltaic parameters such as V_{oc}, short-circuit current density (J_{sc}), fill factor (FF), and conversion efficiency (η) of the fabricated PERCs with different annealing processes. The performance of an industrial PERC is also shown for the purpose of comparison. The industry PERC was fabricated under identical conditions but no additional annealing process was used, since the Al_2O_3 layer was annealed during the SiN_x deposition at 400 °C. Note that in this study, during the annealing processes, the front side was placed downward and made contact to a wafer holder. The front SiN_x layer was not exposed to the annealing gases, and thus, the influence of the front SiN_x layer might be insignificant. The industry PERC shows the lowest V_{oc} of 665.4 mV among the others. This could be attributed to its lower wafer lifetime of 797 μs at the injection level of $3 \times 10^{15}\,cm^{-3}$. The V_{oc} value improves to 671.3 mV for O_2 annealing and 672.3 mV for FG annealing. The two-step annealing further increases V_{oc} to 675.5 mV, which is an improvement by about 0.6% compared to one-step annealing, or by 1.5% compared to the industry one. There is no much difference in J_{sc} and FF between the PERCs. The two-step annealing exhibits the best conversion efficiencies of 21.97%, which is 0.36%abs higher than industry PERC. Finally, five PERCs were fabricated for each annealing process. The mean value and distribution range of V_{oc} and FF are shown in Fig. 8a and b, respectively. The PERCs with the two-step annealing show V_{oc} of 675–677.5 mV with a mean value of 676 mV, and FF of 0.813–0.819 with a mean value of 0.816.

Conclusion

The Al_2O_3 films are prepared using atomic layer deposition, followed by O_2, FG, or two-step annealing. Comparing O_2 annealing with FG annealing, the former yields a thicker SiO_x interfacial layer and the higher Q_f density of $-3.9 \times 10^{12}\,cm^{-2}$, indicating a superior field effect passivation. The FG annealing shows the lower D_{it} of $3.7 \times 10^{11}\,eV^{-1}\,cm^{-2}$ resulting from the hydrogenation of the Si interface. The two-step annealing combines the advantages of these two annealing processes and has an

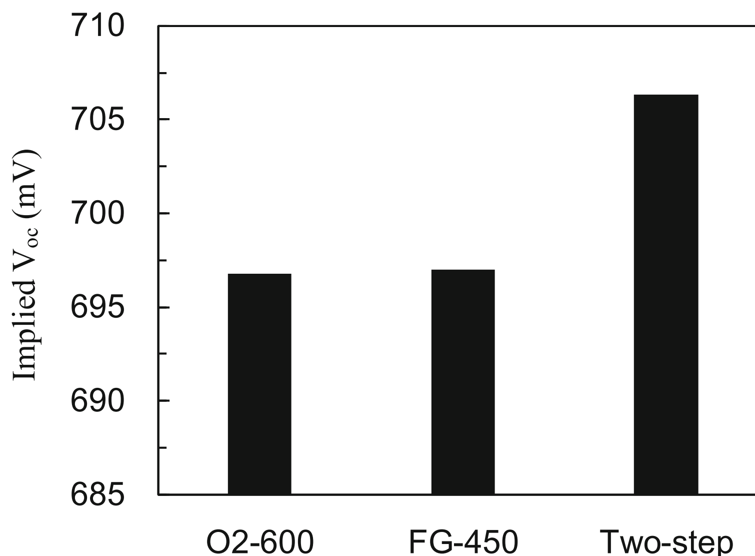

Fig. 6 Implied V_{oc} of the SiN_x/Al_2O_3-passivated samples with O_2, FG, and two-step annealing

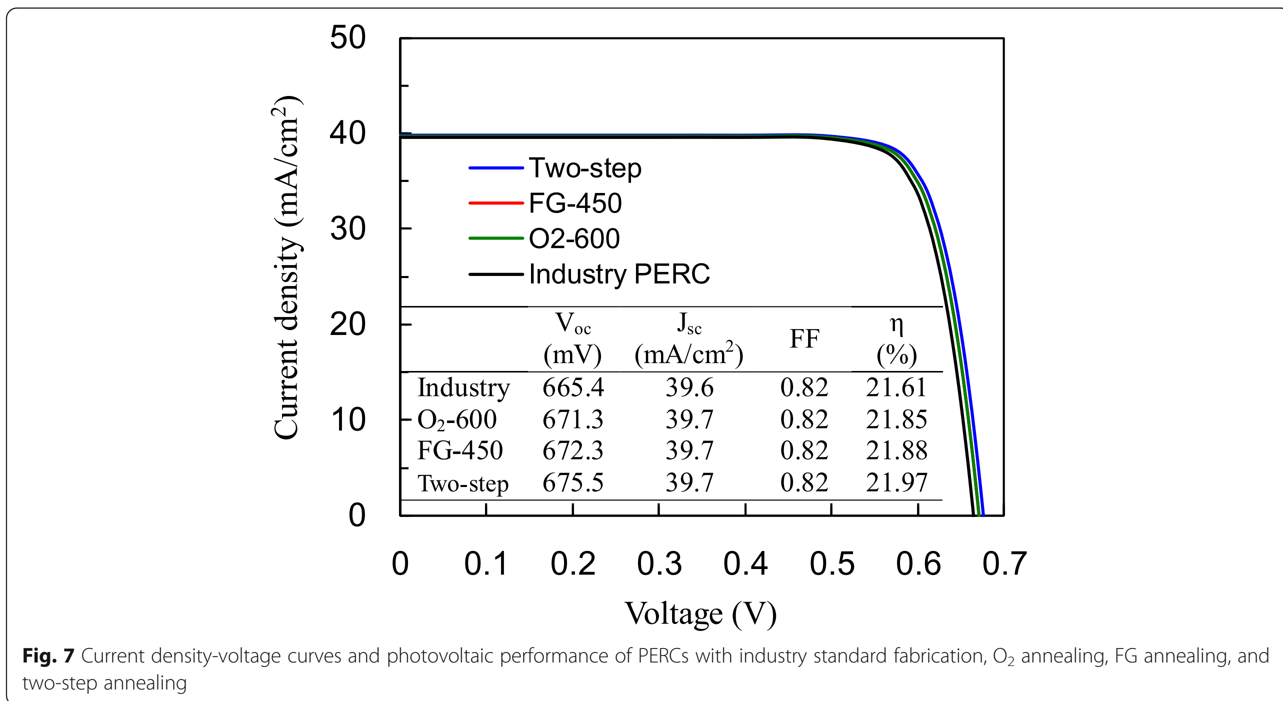

Fig. 7 Current density-voltage curves and photovoltaic performance of PERCs with industry standard fabrication, O_2 annealing, FG annealing, and two-step annealing

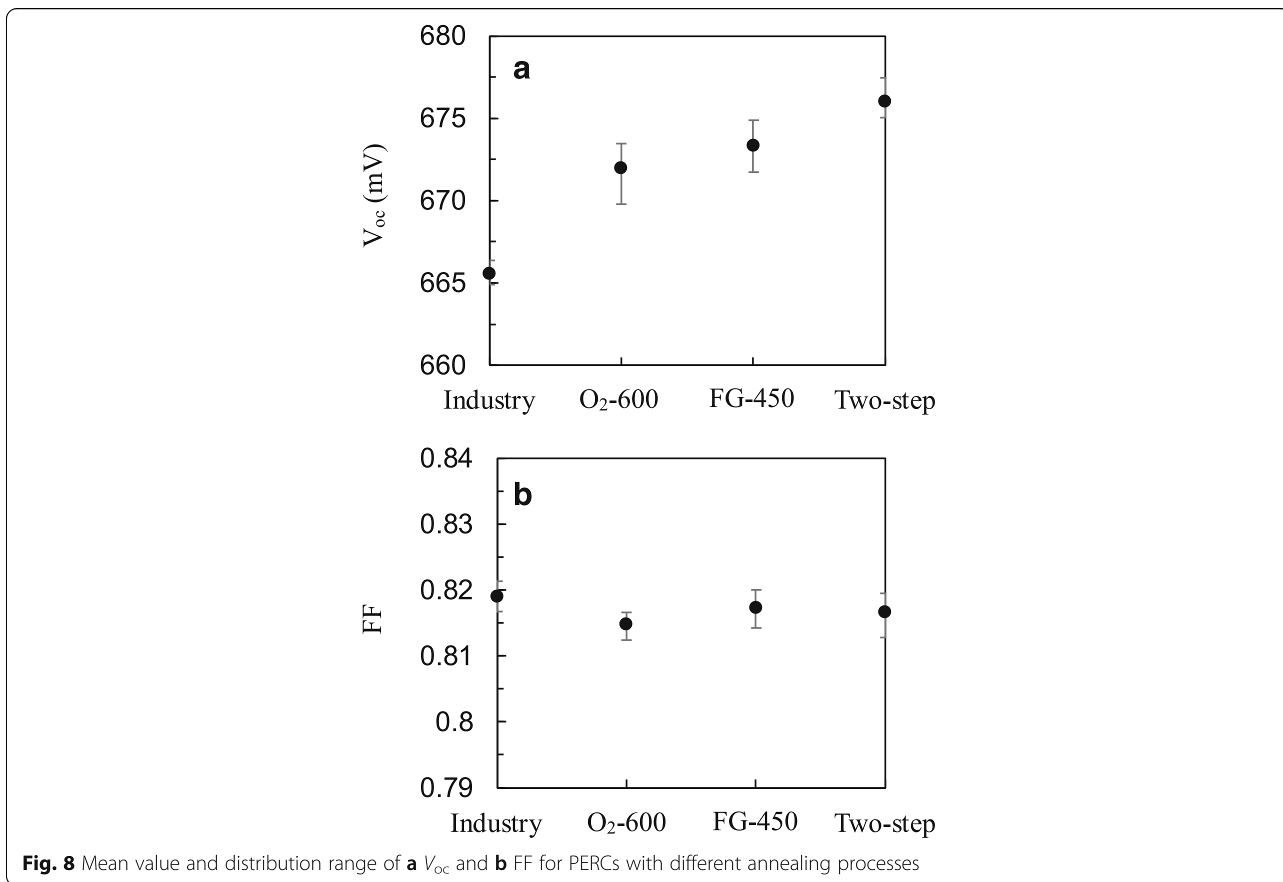

Fig. 8 Mean value and distribution range of **a** V_{oc} and **b** FF for PERCs with different annealing processes

intermediate Q_f and the lowest D_{it} of 3.1 × 10^{11} eV^{-1} cm^2. The SiN_x/Al_2O_3-passivated samples with the two-step annealing demonstrate a minority carrier lifetime of 2072 μs, close to the intrinsic lifetime limit. For the PERC fabricated with the two-step annealing, V_{oc} of 675.5 mV and conversion efficiency of 21.97% can be obtained, which respectively have increases of 10 mV and 0.36%abs as compared to those of the industry PERC.

Abbreviations

Al_2O_3: Aluminum oxide; ALD: Atomic layer deposition; *C-V*: Capacitance-voltage; D_{it}: Interface defect density; FF: Fill factor; FG: Forming gas; J_{sc}: Short-circuit current density; *J-V*: Current density-voltage; MOS: Metal-oxide-semiconductor; NH_3: Ammonia; O_2: Oxygen; PERC: Passivated emitter and rear cell; Q_f: Fixed oxide charge; SiN_x: Silicon nitride; SiO_x: Silicon oxide; TEM: Transmission electron microscope; TMA: Trimethylaluminum; TMS: Tetramethylsilane; V_{oc}: Open-circuit voltage; *η*: Conversion efficiency

Funding

This work is sponsored by the Ministry of Science and Technology of Taiwan (nos. 104-2632-E-212-002-, 104-2622-E-212-005-CC3, 104-2221-E-212-002-MY3). This work is also supported by the National Natural Science Foundation of China (nos. 61474081, 61534005 and 61307115), the Science Technology innovation project of Xiamen (nos. 3502Z201730404) and the Fundamental Research Funds for the Central Universities (nos. 20720150028).

Availability of Data and Materials

All data supporting the conclusions of this article are included within the article.

Authors' Contributions

CHH and SYL designed and performed the experiments. YSC and XYZ performed the measurements. CHH, WYW, SYL, WZZ, SZ, and SYC analyzed the measurement data. CHH and SYL finalized the manuscript. All authors read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

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Received: 3 January 2019 Accepted: 1 April 2019
Published online: 18 April 2019

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