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# Germanium Negative Capacitance Field Effect Transistors: Impacts of Zr Composition in $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$

Yue Peng , Yan Liu\*, Genquan Han\*, Jincheng Zhang and Yue Hao

## Abstract

Germanium (Ge) negative capacitance field-effect transistors (NCFETs) with various Zr compositions in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  ( $x = 0.33, 0.48, \text{ and } 0.67$ ) are fabricated and characterized. For each Zr composition, the NCFET exhibits the sudden drop in some points of subthreshold swing (SS), which is induced by the NC effect. Drive current  $I_{\text{DS}}$  increases with the increase of annealing temperature, which should be due to the reduced source/drain resistance and improved carrier mobility. The steep SS points are repeatable and stable through multiple DC sweeping measurement proving that they are induced by the NC effect. The values of gate voltage  $V_{\text{GS}}$  corresponding to steep SS are consistent and clockwise  $I_{\text{DS}}-V_{\text{GS}}$  are maintained through the multiple DC sweeps. At fixed annealing temperature, NC device with  $\text{Hf}_{0.52}\text{Zr}_{0.48}\text{O}_2$  achieves the higher  $I_{\text{DS}}$  but larger hysteresis compared to the other compositions. NCFET with  $\text{Hf}_{0.67}\text{Zr}_{0.33}\text{O}_2$  can obtain the excellent performance with hysteresis-free curves and high  $I_{\text{DS}}$ .

**Keywords:** Ferroelectric, Negative capacitance, Hysteresis, Subthreshold swing, FET

## Background

The ferroelectric negative capacitance field-effect transistor (NCFET) with a ferroelectric film inserted into gate stack is a promising candidate for the low-power dissipation applications owing to its ability to overcome the fundamental limitation in subthreshold swing (SS) for the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) [1]. The negative capacitance (NC) phenomena in NCFETs have been extensively studied in different channel materials, including silicon (Si) [2, 3], germanium (Ge) [4], germanium-tin (GeSn) [5], III–V [6], and 2D materials [7]. Also, the NC characteristics have been demonstrated in NCFETs with various ferroelectrics, such as  $\text{BiFeO}_3$  [8],  $\text{PbZrTiO}_3$  (PZT) [9], PVDF [10], and  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  [11]. Compared to other ferroelectrics,  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  has the advantage of being compatible with CMOS integration. Experimental studies have shown that the electrical performance of NCFETs can be optimized

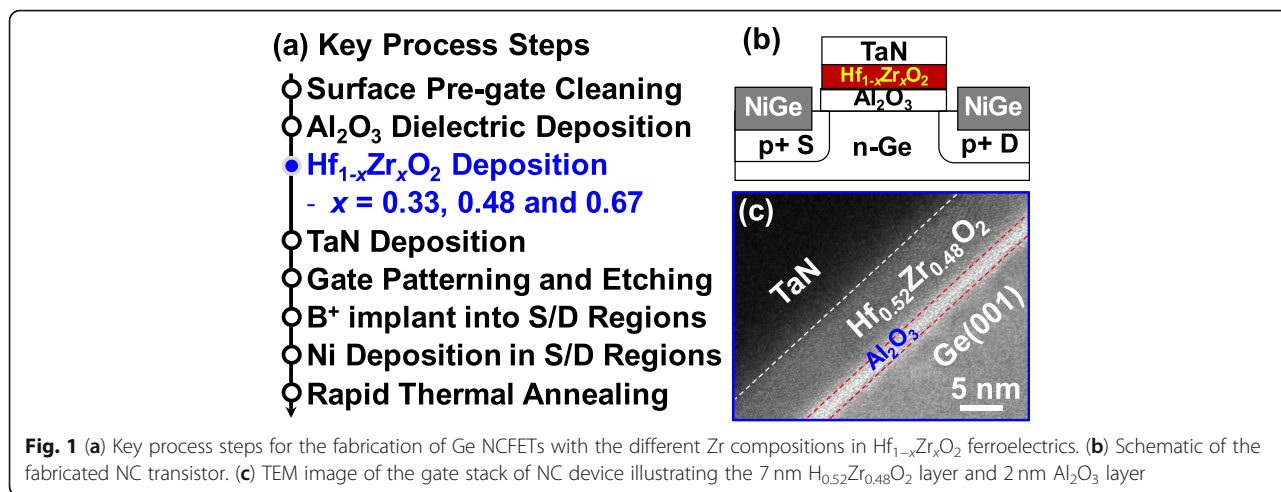
by varying the thickness and area of  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$ , which affects the matching between MOS capacitance ( $C_{\text{MOS}}$ ) and ferroelectric capacitance ( $C_{\text{FE}}$ ) [12, 13]. It is expected that the Zr composition in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  also has a great impact on the performance of NCFETs, because it determines the ferroelectric properties of  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$ . However, there is still a lack of a detailed study on the impacts of Zr composition on the electrical characteristics of NCFETs.

In this paper, we comprehensively study the influences of the annealing temperature and the Zr composition on the performance of Ge NCFET.

## Methods

Key process steps for fabricating Ge p-channel NCFETs with the different Zr compositions in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  are shown in Fig. 1(a). After the pregate cleaning, n-Ge (001) substrates were loaded into the atom layer deposition (ALD) chamber. A thin  $\text{Al}_2\text{O}_3$  (25 cycles) film was deposited, which was followed by the  $\text{O}_3$  passivation. Then, the  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  films ( $x = 0.33, 0.48 \text{ and } 0.67$ ) were

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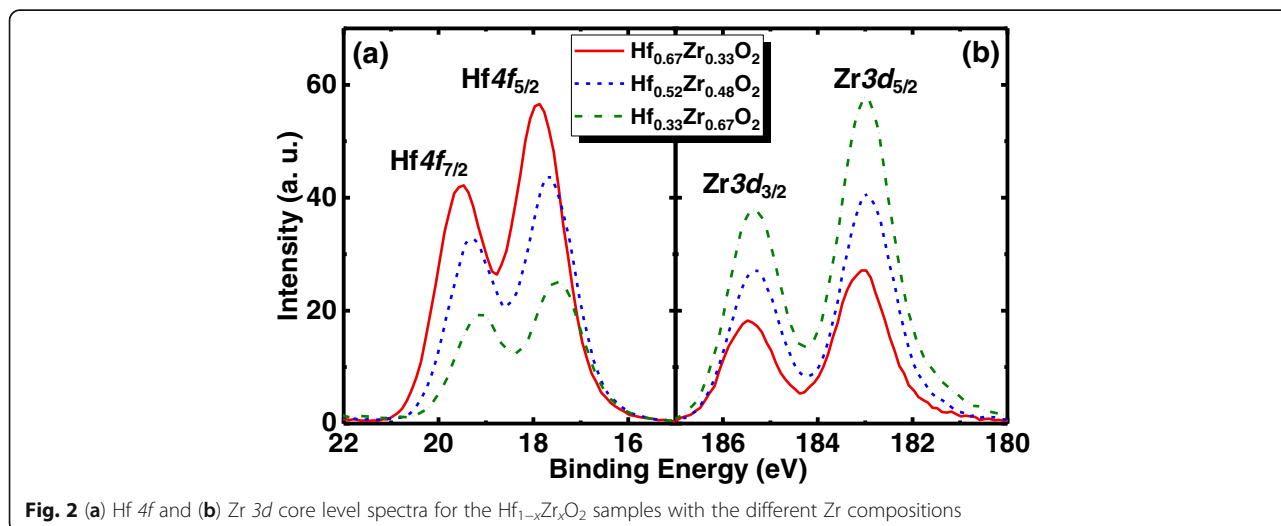
deposited in the same ALD chamber using [(CH<sub>3</sub>)<sub>2</sub>N]<sub>4</sub>Hf (TDMAHf), [(CH<sub>3</sub>)<sub>2</sub>N]<sub>4</sub>Zr (TDMAZr) and H<sub>2</sub>O as the Hf, Zr, and O precursors, respectively. After that, the TaN metal gate was deposited using the reactive sputtering. After gate patterning and etching, boron ions (B<sup>+</sup>) were implanted into source/drain (S/D) regions at an energy of 20 keV and a dose of 1 × 10<sup>15</sup> cm<sup>-2</sup>. Non-self-aligned S/D metals were formed by lift-off process. Finally, rapid thermal annealing (RTA) was carried out at various temperatures for dopant activation, S/D metallization, and crystallization of Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub> film. Ge control pMOSFETs with the Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack was also fabricated.

Figure 1(b) shows the schematic of the fabricated NCFET. High-resolution transmission electron microscope (HRTEM) image in Fig. 1(c) shows the gate stack on Ge channel of device with Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub>

ferroelectric. The thicknesses of Al<sub>2</sub>O<sub>3</sub> and Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub> layers are 2 nm and 7 nm, respectively.

To confirm the stoichiometries of Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub>, the X-ray photoelectron spectroscopy (XPS) measurement was carried out. Figure 2(a) and (b) show the Hf4f and Zr3d photoelectron core level spectra, respectively, for the Hf<sub>0.67</sub>Zr<sub>0.33</sub>O<sub>2</sub>, Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub>, and Hf<sub>0.33</sub>Zr<sub>0.67</sub>O<sub>2</sub> films. The material compositions were calculated based on the area ratio of the peaks and the corresponding sensitivity factors. The two peaks of Zr3d<sub>5/2</sub> and Zr3d<sub>3/2</sub> have a spin-orbital splitting of 2.4 eV, which is consisted with Refs. [14, 15]. With the increment of Zr composition in Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub>, Zr3d, and Hf4f peaks shift to the lower energy direction.

The ferroelectric properties of the Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub> films (x = 0.33, 0.48, and 0.66) were characterized by the polarization P vs. drive voltage V hysteresis loops

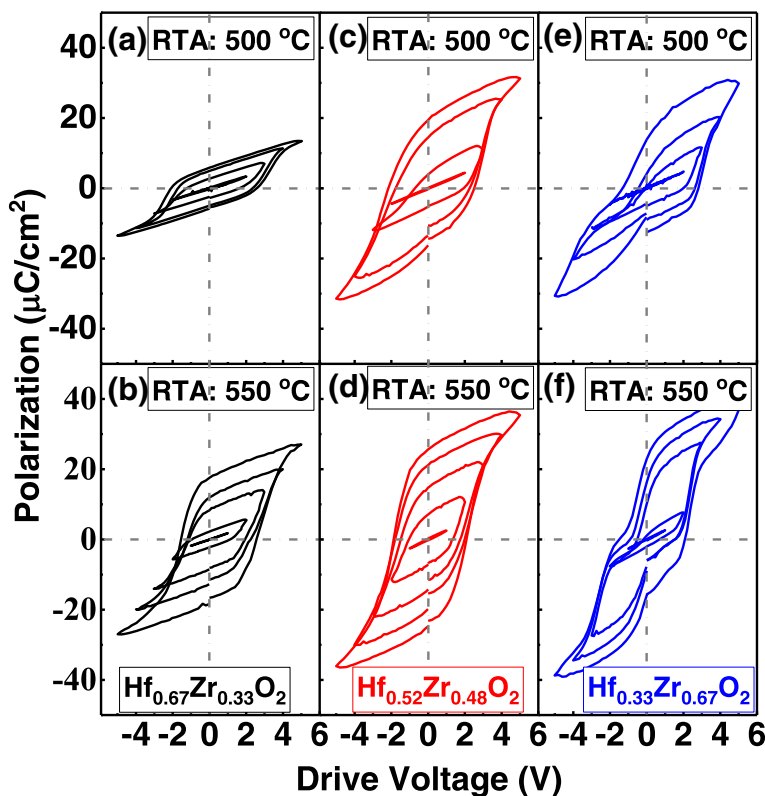


measurement.  $P$ - $V$  loops were recorded on the pristine devices. Figure 3 shows the curves of  $P$  vs.  $V$  for TaN/Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub>(10 nm)/TaN samples in a series of drive voltages. With the post-annealing temperature increases from 500 to 550 °C, the  $P$ - $V$  curves of the Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub> tend to be saturated in a sub-loop state. As the Zr composition increases, the remnant polarization of the film is obviously improved, and the thinning of the hysteresis loop at zero bias is observed, which can be phenomenologically best described as superimposed antiferroelectric-like characteristics [16, 17].

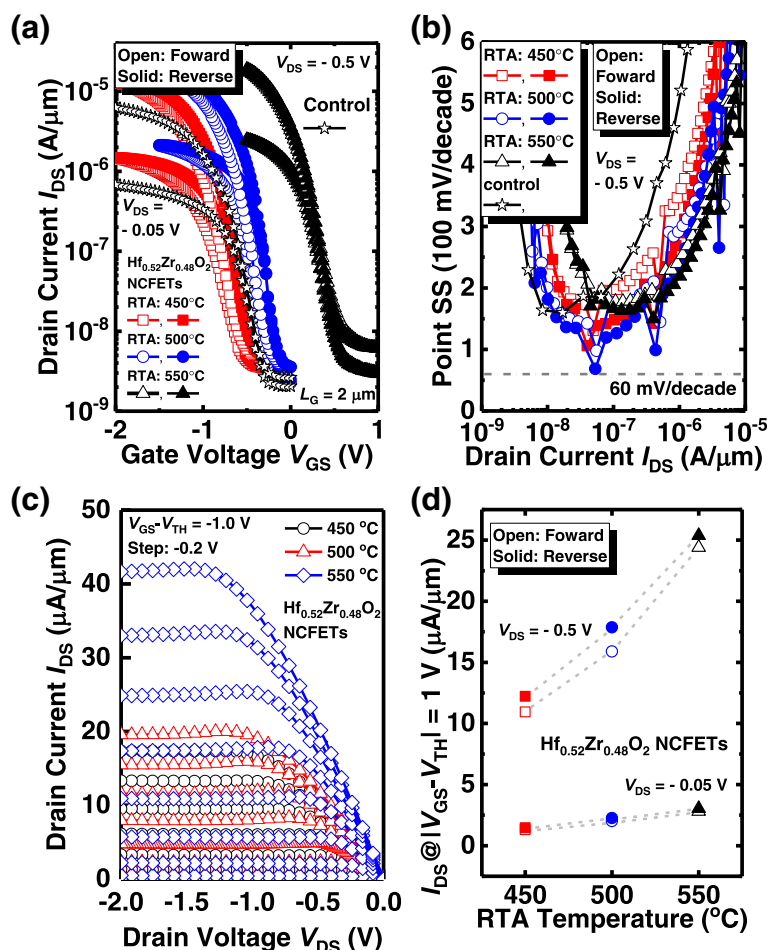
**Results and Discussion**

Figure 4(a) shows the measured transfer characteristics of Ge NCFETs with Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub> ferroelectrics with different annealing temperatures and control device with Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> stack dielectric. The control device was annealed at 500 °C. All the devices have a gate length  $L_G$  of 2 μm. The forward and reverse sweeping are indicated by the open and solid symbols, respectively. The NCFETs have a much higher drive current compared to the control device. It is seen

that, with the annealing temperature increasing from 450 to 550 °C, the threshold voltage  $V_{TH}$  of the NC devices shift to the positive  $V_{GS}$  direction. The NCFETs exhibit a small hysteresis, which becomes negligible with the increasing of RTA temperature. The trapping effect also leads to the hysteresis, but that produces the counterclockwise  $I_{DS}$ - $V_{GS}$  loop, opposite to the results induced by ferroelectric switching [18]. Point SS vs.  $I_{DS}$  curves in Fig. 4(b) show that the NC transistor exhibits the sudden drop in some points of SS, corresponding to the abrupt change of  $I_{DS}$  induced by the NC effect [19]. It is observed that NCFETs achieve the improved SS characteristics compared to the control device. We found that the sudden drop points of the devices are consistent at the different annealing temperatures. The measured  $I_{DS}$ - $V_{DS}$  curves of the NCFETs with Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub> ferroelectric annealed at different temperatures are shown in Fig. 4(c).  $I_{DS}$ - $V_{DS}$  curves of the NC transistor show the obvious NDR phenomenon, which is a typical characteristic of NC transistors [20–23]. Figure 4(d) is the plots of the  $I_{DS}$  of the Ge NCFETs with the Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub> ferroelectric layer annealed at



**Fig. 3** Measured  $P$ - $V$  curves of the Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub> films with different Zr compositions annealed at 500 and 550 °C. (a) and (b) are the Hf<sub>0.67</sub>Zr<sub>0.33</sub>O<sub>2</sub> film annealed at 500 and 550 °C, respectively. (c) and (d) are the Hf<sub>0.52</sub>Zr<sub>0.48</sub>O<sub>2</sub> film annealed at 500 and 550 °C, respectively. (e) and (f) are the Hf<sub>0.33</sub>Zr<sub>0.67</sub>O<sub>2</sub> film annealed at 500 and 550 °C, respectively. With the post annealing temperature increases from 500 to 550 °C, the  $P$ - $V$  curves of the Hf<sub>1-x</sub>Zr<sub>x</sub>O<sub>2</sub> tend to be saturated in a sub-loop state. An evolution ferroelectric to an antiferroelectric-like behavior is observed with the Zr composition increased



**Fig. 4** (a) Measured  $I_{DS}$ - $V_{GS}$  curves for NCFETs with  $Hf_{0.52}Zr_{0.48}O_2$  ferroelectric and control device. (b) Point SS vs.  $I_{DS}$  curves showing that NCFETs have the steeper SS compared to control MOSFET. (c)  $I_{DS}$ - $V_{DS}$  curves for the NCFETs demonstrating the typical NDR phenomena. (d) Comparison of the  $I_{DS}$  for the NCFETs annealed at various temperatures at a gate overdrive of 1 V

450, 500, and 550 °C, respectively, at  $V_{DS} = -0.05$  V and  $-0.5$  V, and  $|V_{GS} - V_{TH}| = 1.0$  V. Here, the  $V_{TH}$  is defined as the  $V_{GS}$  at  $I_{DS}$  of  $10^{-7}$  A/ $\mu$ m.  $I_{DS}$  increases with the increasing of RTA temperature, which is due to the reduced source/drain resistance and improved carrier mobility at the higher annealing temperature.

In addition to the  $Hf_{0.52}Zr_{0.48}O_2$  ferroelectric transistor, we also investigate the electrical characteristics of Ge NC transistors with the  $Hf_{0.33}Zr_{0.67}O_2$  ferroelectric. Figure 5(a) presents the  $I_{DS}$ - $V_{GS}$  characteristics of the devices with  $Hf_{0.33}Zr_{0.67}O_2$  with the different annealing temperatures at  $V_{DS} = -0.05$  V and  $-0.5$  V. Compared to the  $Hf_{0.52}Zr_{0.48}O_2$  NC transistors, even smaller hysteresis is obtained. Similar to the  $Hf_{0.52}Zr_{0.48}O_2$  NC transistors, as the annealing temperature increases from 450 to 550 °C,  $V_{TH}$  of the device increase from  $-0.63$  V to  $0.51$  V in the forward

sweeping at  $V_{DS} = -0.05$  V. Point SS as a function of  $I_{DS}$  characteristics for the  $Hf_{0.33}Zr_{0.67}O_2$  ferroelectric NCFETs are depicted in Fig. 5(b). In addition, devices with 450 °C and 500 °C annealing temperature obtains the more obvious sudden drop in SS in comparison with the 550 °C annealed transistor. The sudden drop points in different annealing temperatures occur at the same gate voltage. Figure 5(c) exhibits forward and reverse  $I_{DS}$  of the  $Hf_{0.33}Zr_{0.67}O_2$  NCFETs at  $V_{DS} = -0.05$  V and  $-0.5$  V, and  $|V_{GS} - V_{TH}| = 1.0$  V. Whether for the forward or reverse sweeping, the  $I_{DS}$  increases with the annealing temperature, which is consistent with the characteristic of the  $Hf_{0.52}Zr_{0.48}O_2$  device.

We also investigate the electrical performance of Ge NCFET with the smaller Zr composition. The transfer characteristics of the  $Hf_{0.67}Zr_{0.33}O_2$  NCFETs annealed at different annealing temperatures are presented in

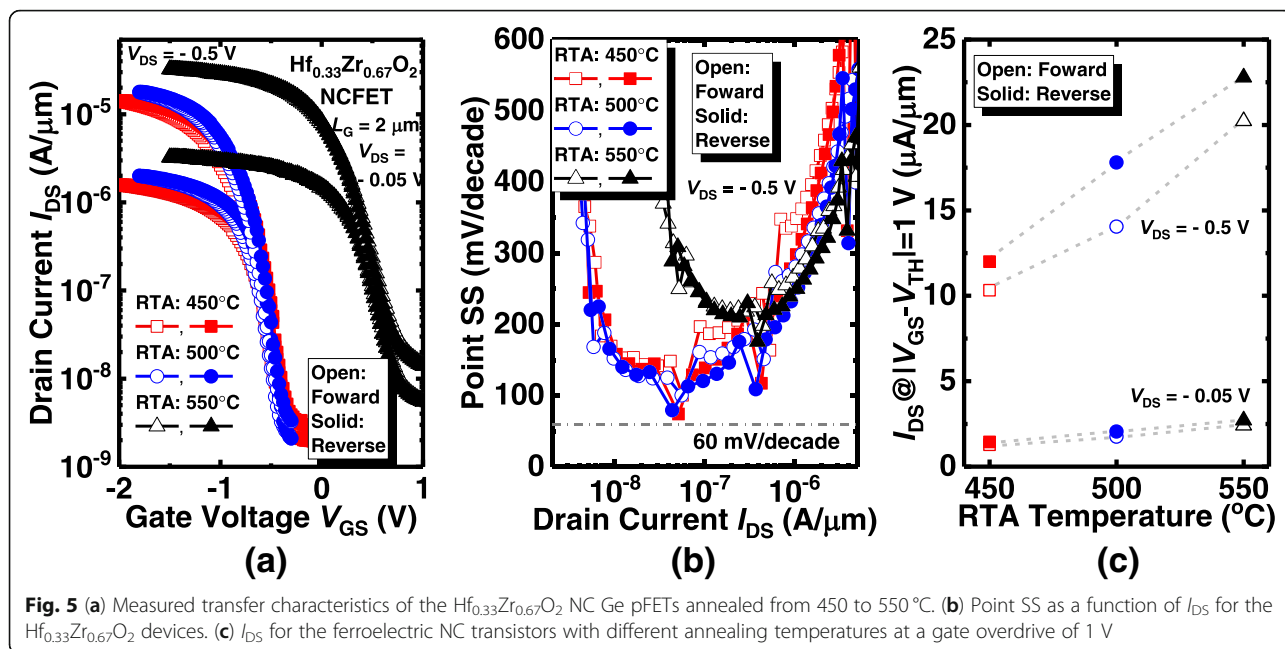
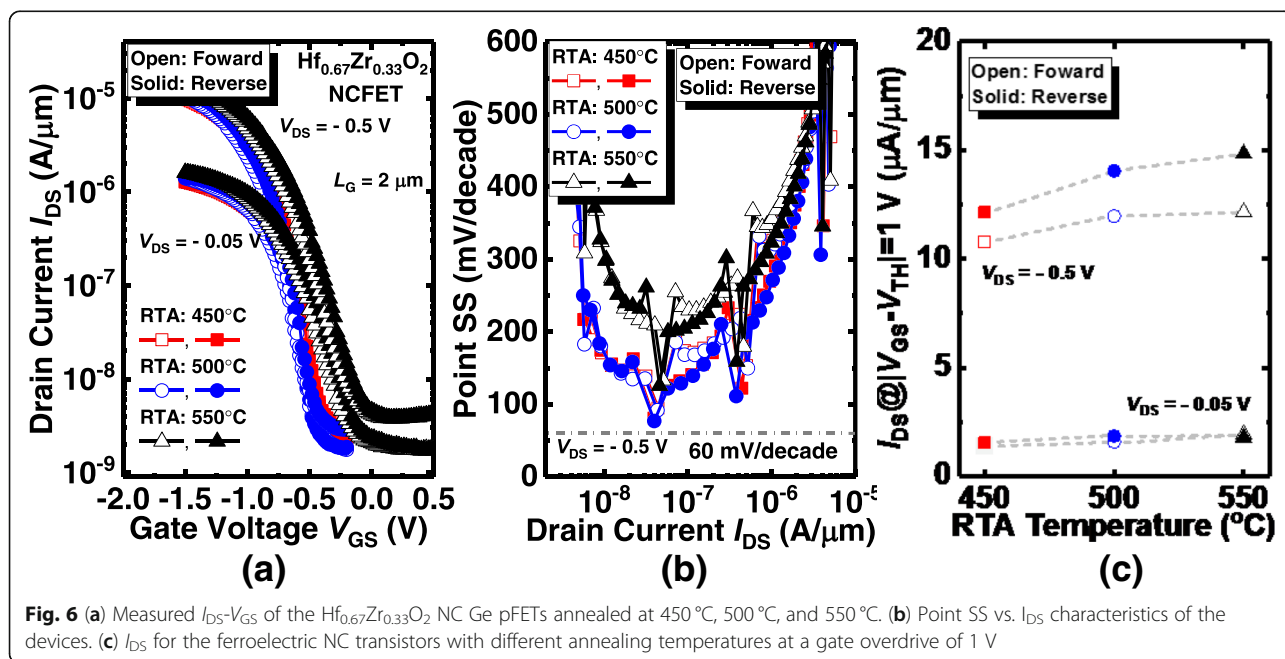
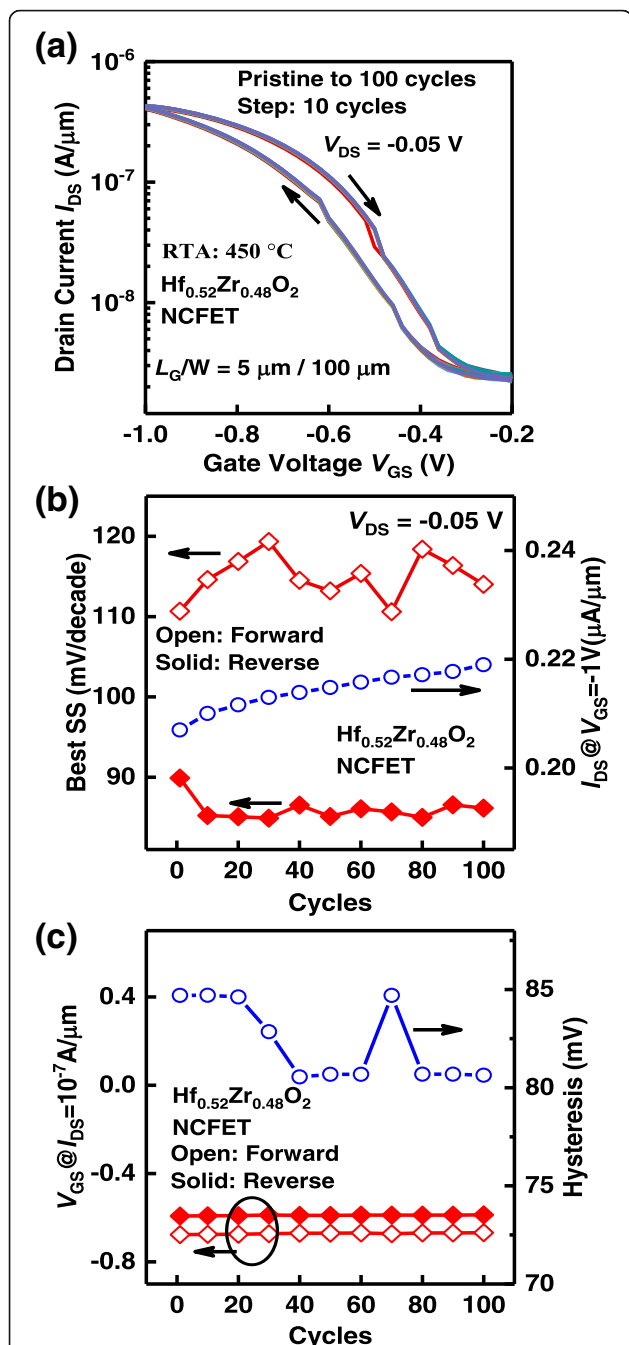


Fig. 6(a). No hysteresis phenomenon is observed. Compared to  $\text{Hf}_{0.33}\text{Zr}_{0.67}\text{O}_2$  and  $\text{Hf}_{0.52}\text{Zr}_{0.48}\text{O}_2$  devices, the  $V_{\text{TH}}$  shift induced by varying annealing temperature is less pronounced in  $\text{Hf}_{0.67}\text{Zr}_{0.33}\text{O}_2$  NCFETs. Point SS vs.  $I_{\text{DS}}$  curves in Fig. 6(b) show that the  $\text{Hf}_{0.67}\text{Zr}_{0.33}\text{O}_2$  NC transistor exhibits the sudden drop in some points of SS of NC transistor at

$V_{\text{DS}} = -0.05$  V. Figure 6(c) presents the  $I_{\text{DS}}$  of  $\text{Hf}_{0.67}\text{Zr}_{0.33}\text{O}_2$  Ge NCFETs annealed at 450 °C, 500 °C, and 550 °C, at  $V_{\text{DS}} = -0.05$  V and  $-0.5$  V, and  $|V_{\text{GS}} - V_{\text{TH}}| = 1.0$  V. Likewise,  $I_{\text{DS}}$  enhances as the RTA temperature increases.

The stability of the NC effect induced by the ferroelectric layer of the  $\text{Hf}_{0.52}\text{Zr}_{0.48}\text{O}_2$  NCFET was





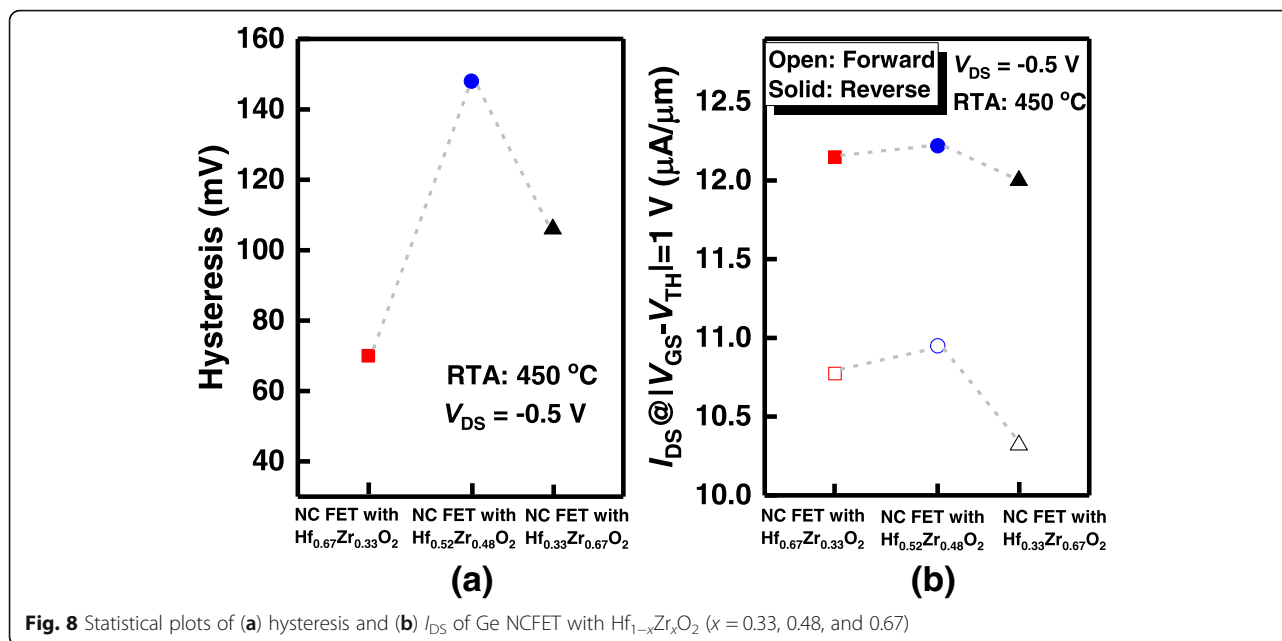
**Fig. 7** (a) Measured  $I_{DS}$ - $V_{GS}$  curves of a  $\text{Hf}_{0.52}\text{Zr}_{0.48}\text{O}_2$  NC Ge pFET over 100 cycles of DC sweeping. (b) Best point SS and  $I_{DS}$  vs. cycle number. (c) Hysteresis characteristics as a function of the number of DC sweeping cycles

verified by multiple DC sweeping measurements. The measured  $I_{DS}$ - $V_{GS}$  curves over 100 cycles of DC sweeping are shown in Fig. 7(a). It can be seen that the values of  $V_{GS}$  corresponding to steep SS are consistent. In addition, the clockwise  $I$ - $V$  loops are maintained through the multiple DC sweeps. The steep SS points are repeatable and stable through multiple DC sweeps, which further proves that they are induced by the NC effect. Figure 7(b) presents the best point SS and drive current across the number of sweeping cycles. Figure 7(c) shows the hysteresis characteristics as a function of the number of DC sweeping cycles. Stable  $I$ - $V$  hysteresis window of  $\sim 82$  mV are seen.

We summarize the hysteresis and drive current characteristics of Ge NCFETs with different Zr compositions in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  in Fig. 8. As shown in Fig. 8(a), the hysteresis values are 70, 148, and 106 mV for devices with  $x = 0.33, 0.48,$  and  $0.67,$  respectively, at a  $V_{DS}$  of  $-0.5$  V. As the composition increases from 0.33 to 0.48, the hysteresis of the NC device increases significantly. With the further increasing of Zr composition, the hysteresis decreases rapidly. The  $I_{DS}$  of NCFETs annealed at 450 °C is plotted in Fig. 8(b), at  $V_{DS} = -0.5$  V and  $V_{GS} - V_{TH} = -1.0$  V. Open and solid represent the forward and reverse sweeping, respectively. The NC device with  $\text{Hf}_{0.52}\text{Zr}_{0.48}\text{O}_2$  achieves the highest  $I_{DS}$ , but its hysteresis is serious. NCFET with  $\text{Hf}_{0.67}\text{Zr}_{0.33}\text{O}_2$  can obtain excellent performance with hysteresis-free curves and high  $I_{DS}$ . As Zr composition increases, the ferroelectric capacitance  $C_{fe}$  ( $= 0.3849 \cdot P_r / (E_c \cdot t_{fe})$ ) [24]) increases with the increasing of  $P_r$  and meanwhile, the MOS capacitance ( $C_{MOS}$ ) rises as well due to the growing permittivity of the HZO film. The  $I_{DS}$  and hysteresis are determined by  $|C_{fe}|$  and  $C_{MOS}$  of the transistor. With Zr composition increasing from 0.33 to 0.48, the increase of  $|C_{fe}|$  is speculated to be slower than does the  $C_{MOS}$ , leading to the widening of the hysteresis. Nevertheless, the larger  $C_{MOS}$  produces a higher  $I_{DS}$ . With the further increase of Zr composition, the increase of  $|C_{fe}|$  is faster than  $C_{MOS}$ , which might provide  $|C_{fe}| \geq C_{MOS}$ , reducing the hysteresis of NCFET.

**Conclusions**

The impacts of the annealing temperature and Zr composition in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  on the electrical performance of the Ge NCFETs are experimentally studied. The stoichiometries and ferroelectric properties of  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  were confirmed by XPS and  $P$ - $V$  measurements, respectively. NCFETs demonstrate the steep point SS and improved  $I_{DS}$  compared to the control device, due to the NC effect.



**Fig. 8** Statistical plots of (a) hysteresis and (b)  $I_{DS}$  of Ge NCFET with  $Hf_{1-x}Zr_xO_2$  ( $x = 0.33, 0.48, \text{ and } 0.67$ )

The  $V_{TH}$  and  $I_{DS}$  of the  $Hf_{1-x}Zr_xO_2$  NCFET are greatly affected by the annealing temperature. Multiple DC sweeping measurements show that the stability of the NC effect induced by the ferroelectric layer is achieved in NCFET.  $Hf_{0.67}Zr_{0.33}O_2$  NCFET can more easily achieve the hysteresis-free characteristics than the devices with higher Zr composition.

#### Abbreviations

Al<sub>2</sub>O<sub>3</sub>: Aluminum oxide; ALD: Atomic layer deposition; BF<sub>2</sub><sup>+</sup>: Boron fluoride ion; DC: Direct current; Ge: Germanium; GeO<sub>x</sub>: Germanium oxide; HF: Hydrofluoric acid; HfO<sub>2</sub>: Hafnium dioxide; HRTEM: High-resolution transmission electron microscope; MOSFETs: Metal-oxide-semiconductor field-effect transistors; NC: Negative capacitance; Ni: Nickel; SS: Subthreshold swing; TaN: Tantalum nitride; TDMAHF: Tetrakis (dimethylamido) hafnium; TDMAZr: Tetrakis (dimethylamido) zirconium

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#### Availability of Data and Materials

The datasets supporting the conclusions of this article are included within the article.

#### Authors' Contributions

YP carried out the experiments and drafted the manuscript. YP and GQH designed the experiments. GQH and YL helped to revise the manuscript. JCZ and YH supported the study. All the authors read and approved the final manuscript.

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#### Competing Interests

The authors declare that they have no competing interests.

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#### References

- Salahuddin S, Datta S (2008) Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett* 8:405–410
- Lee MH, Chen P-G, Liu C, Chu C-Y, Cheng C-C, Xie M-J, Liu S-N, Lee J-W, Huang S-J, Liao M-H, Tang M, Li K-S, Chen M-C (2015) Prospects for ferroelectric HfZrOx FETs with experimentally CET=0.98nm, SSfor=42 mV/dec, SSrev=28 mV/dec, switch-off <0.2 V, and hysteresis-free strategies. In: *IEDM Tech. Dig.*, pp 616–619
- Li K-S, Chen P-G, Lai T-Y, Lin C-H, Cheng C-C, Chen C-C, Wei Y-J, Hou Y-F, Liao M-H, Lee M-H, Chen M-C, Sheih J-M, Yeh W-K, Yang F-L, Salahuddin S, Hu C (2015) Sub-60mV-swing negative-capacitance FinFET without hysteresis. In: *IEDM Tech. Dig.*, pp 620–623
- Zhou J, Han G, Li Q, Peng Y, Lu X, Zhang C, Zhang J, Sun Q-Q, Zhang D-W, Hao Y (2016) Ferroelectric HfZrOx Ge and GeSn pMOSFETs with sub-60 mV/decade subthreshold swing, negligible hysteresis, and improved  $I_{DS}$ . In: *IEDM Tech. Dig.*, pp 395–339
- Zhou J, Han G, Peng Y, Liu Y, Sun Q-Q, Zhang D-W, Hao Y (2017) Ferroelectric negative capacitance GeSn pFETs with sub20 mV/decade subthreshold swing. *IEEE Electron Device Lett* 38:1157–1160
- Luc QH, Fan-Chiang CC, Huynh SH, Huang P, Do HB, Ha MTH, Jin YD, Nguyen TA, Zhang KY, Wang HC, Lin YK, Lin YC, Hu C, Iwai H, Chang EY (2018) First experimental demonstration of negative capacitance InGaAs MOSFETs with Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> ferroelectric gate stack. In: *Symp. VLSI Technol.*, pp 47–48
- Wei M, Chunsheng S, Wonil J, Yuchen C, Muhammad D, AlamPeide A, Ye D (2018) Steep-Slope WSe<sub>2</sub> Negative Capacitance Field-Effect Transistor. *Nano Lett* 18:3682–3687
- Khan AI, Chatterjee K, Duarte JP, Lu Z, Sachid A, Khandelwal S, Ramesh R, Hu C, Salahuddin S (2016) Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor. *IEEE Electron Device Lett*. 37:111–114
- Dasgupta S, Rajashekhar A, Majumdar K, Agrawal N, Razavieh A, Trolrier-Mckinstry S, Datta S (2015) Sub-kT/q switching in strong inversion in PbZr<sub>0.2</sub>

- $_{52}\text{Ti}_{0.48}\text{O}_3$  gated negative capacitance FETs. *IEEE J Exploratory Solid-State Comput Devices Circuits* 1:43–48
10. Rusu A, Salvatore GA, Jiménez D, Ionescu AM (2010) Metal-ferroelectric-metal-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification. In: *IEDM Tech. Dig.*, pp 395–398
  11. Cheng CH, Chin A (2014) Low-voltage steep turn-on pMOSFET using ferroelectric high- $\kappa$  gate dielectric. *IEEE Electron Device Lett* 35:274–276
  12. Li J, Zhou J, Han G, Liu Y, Peng Y, Zhang J, Sun Q-Q, Zhang DW, Hao Y (2018) Negative capacitance Ge PFETs for performance improvement: impact of thickness of HfZrOx. *IEEE Trans Electron Devices* 65:1217–1222
  13. Zhou J, Han G, Li J, Peng Y, Liu Y, Zhang J, Sun Q-Q, Zhang DW, Hao Y (2017) Comparative study of negative capacitance Ge PFETs with HfZrOx partially and fully covering gate region. *IEEE Trans Electron Devices* 64: 4838–4843
  14. Heo S, Tahir D, Chung JG, Lee JC, Kim KH, Lee J, Lee H-I, Park GS, Oh SK, Kang HJ, Choi P, Choi B-D (2015) Band alignment of atomic layer deposited (HfZrO<sub>4</sub>)<sub>1-x</sub>(SiO<sub>2</sub>)<sub>x</sub> gate dielectrics on Si (100). *Appl Phys Lett* 107:182101
  15. Triyoso DH, Hedge RI, Schaeffer JK, Roan D, Tobin PJ, Samavedam SB, White BE Jr, Gregory R, Wang XD (2006) Impact of Zr addition on properties of atomic layer deposited HfO<sub>2</sub>. *Appl Phys Lett* 88:222901
  16. Müller J, Böske TS, Schröder U, Mueller S, Bräuhaus D, Böttger U, Frey L, Mikolajick T (2012) Ferroelectricity in simple binary ZrO<sub>2</sub> and HfO<sub>2</sub>. *Nano Lett* 12:4318–4323
  17. Park MH, Lee YH, Kim HJ, Schenk T, Lee W, Kim KD, Fengler FPG, Mikolajick T, Schroeder U, Hwang CS (2013) Surface and grain boundary energy as the key enabler to ferroelectricity in nanoscale hafnia-zirconia: comparison of model and experiment. *Nanoscale* 28:1–16
  18. Yurchuk E, Müller J, Müller S, Paul J, Pešić M, van Bentum R, Schroeder U, Mikolajick T (2016) Charge-trapping phenomena in HfO<sub>2</sub>-based FeFETtype nonvolatile memories. *IEEE Trans Electron Devices* 63:3501–3507
  19. Peng Y, Xiao W, Han G, Wu J, Liu H, Liu Y, Xu N, King Liu T-J, Hao Y (2018) Nanocrystal-embedded-insulator ferroelectric negative capacitance FETs with sub-kT/q swing. *IEEE Electron Device Lett* 40:9–12
  20. Pahwa G, Dutta T, Agarwal A, Khandelwal S, Salahuddin S, Hu C, Chauhan YS (2016) Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance—part II: model validation. *IEEE Trans Electron Devices* 63:4986–4992
  21. Ota H, Ikegami T, Hattori J, Fukuda K, Migita S, Toriumi A (2016) Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration. In: *IEDM Tech. Dig.*, pp 12.4.1–12.4.4
  22. Seo J, Lee J, Shin M (2017) Analysis of drain-induced barrier rising in short-channel negative-capacitance FETs and its applications. *IEEE Trans Electron Devices* 64:1793–1798
  23. Zhou J, Han G, Li J, Liu Y, Peng Y, Zhang J, Sun Q-Q, Zhang DW, Hao Y (2018) Negative differential resistance in negative capacitance FETs. *IEEE Electron Device Lett* 39:622–625
  24. Lin C-I, Khan AI, Salahuddin S, Hu C (2016) Effects of the variation of ferroelectric properties on negative capacitance FET characteristics. *IEEE Trans Electron Devices* 63:2197–2199

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