

NANO EXPRESS

Open Access



A Nanoscale Low-Power Resistorless Voltage Reference with High PSRR

Zekun Zhou¹, Jianwen Cao¹, Yunkun Wang¹, Yue Shi^{2*}, Zhuo Wang¹ and Bo Zhang¹

Abstract

In this paper, a nano-watt resistorless subthreshold voltage reference with high-power supply rejection ratio (PSRR) is presented. A self-biased MOS voltage divider is proposed to provide bias current for whole voltage reference, which is a positive temperature coefficient (TC) current containing threshold voltage characteristics. By injecting the generated current into a transistor with a different threshold voltage, a delta threshold voltage with a greatly reduced negative TC is realized and temperature-compensated by a generated positive TC item at the same time. Therefore, a temperature-stable voltage reference is achieved in the proposed compacted method with low power consumption and high PSRR. Verification results with 65-nm CMOS technology demonstrate that the minimum supply voltage can be as low as 0.35 V with a 0.00182-mm² active area. The generated reference voltage is 148 mV, with a TC of 28 ppm/°C for the -30 to 80 °C temperature range. The line sensitivity is 1.8 mV/V, and the PSRR without any filtering capacitor at 100 Hz is 53 dB with a 2.28-nW power consumption.

Keywords: Subthreshold, Low-power, High PSRR, Resistorless, Nanoscale

Introduction

Voltage reference is one of the core modules in electronic systems, which is widely used in medical electronics, power managements, wireless environmental sensors, and communication circuits. As the supply voltage of electronic systems continues to decrease with technology improvement, the requirements for a low-power voltage reference with nanoscale technology are critically increasing [1, 2].

Conventional voltage references are based on a band-gap reference (BGR) circuit, which is a weighted sum of V_{BE} and thermal voltage [3, 4]. However, due to the non-linear temperature behavior of V_{BE} , it is essential to use curvature compensation approaches to improve the precision of BGR [5, 6]. Another disadvantage of BGR is the power consumption. The V_{BE} is around 0.7 V without shrinking down with process improvement, which absolutely restricts the supply voltage. These make BGRs unsuitable for low-voltage and nanoscale applications.

In order to achieve low-power operation, MOS-only subthreshold voltage references are gradually adopted

[7–10]. As transistors in a weak inversion region have inherent advantages in low-power applications with quite small current, the power consumption of relative voltage references can be effectively reduced. Besides, since the characteristics of metal-oxide-semiconductor field-effect transistor (MOSFET) are consistent with process improvement, voltage reference based on MOSFET is more adaptable to advanced technologies. In addition, the usage of resistors should also be avoided in low-power applications. Since the current in the voltage reference is usually inversely proportional to resistance value, low-power dissipation means high-ohmic resistors [10], which can induce large noise occupying a large chip area.

Power supply rejection ratio (PSRR) is another important parameter of voltage reference. Conventional solutions to improve PSRR are at the cost of chip area and power consumption, such as additional amplifiers [11], long channel transistors [12], cascode structures, and additional gain stage [13].

In order to overcome the mentioned issues above, a nano-watt MOSFET-based resistorless subthreshold voltage reference with high PSRR is proposed in this brief, which is suitable for advanced technology, such as nanoscale process. A self-biased MOSFET voltage divider for PSRR enhancement is adopted in the proposed voltage

* Correspondence: october@cuit.edu.cn

²College of Communication Engineering, Chengdu University of Information Technology, Chengdu 610225, China

Full list of author information is available at the end of the article

reference, which can generate a positive temperature coefficient (TC) current containing threshold voltage characteristics. The current serves as bias currents for the whole voltage reference. Besides, the threshold voltage embedded in the bias current is reproduced by injecting bias current into MOSFET with different threshold voltages in the paper. With the proposed method, a delta threshold voltage (ΔV_{TH}) with greatly reduced negative TC is obtained. Besides, a weighted proportional to absolute temperature (PTAT) item is also obtained, while a weighted sum of ΔV_{TH} and PTAT voltage is realized at the same time. Due to the mutual TC cancelation of two different threshold voltages, the required PTAT voltage can be greatly reduced for temperature compensation. By this method, a MOSFET-only resistorless voltage reference is achieved by a compacted structure with low power consumption.

Method

As shown in Fig. 1, the proposed voltage reference is composed of a start-up circuit, a self-biased current generator, and a V_{REF} generating circuit. All the n-channel MOSFETs are a medium threshold voltage N-type metal-oxide-semiconductor (mvt NMOS). MP4 is a high threshold voltage transistor P-type metal-oxide-semiconductor (hvt PMOS), and the other p-channel MOSFETs are a medium threshold voltage PMOS (mvt PMOS). All the transistors shown in Fig. 1 operate in the subthreshold region, except those in the start-up circuit.

Start-Up Circuit

The start-up circuit consists of MP5, MP6, and MN4. At the beginning of a power-on stage, the gate potential of MP6 is low and MP6 is turned on. The current generated

by MP6 makes the gate potential of MN1 and MN2 rise, and the whole circuit starts to work. At the same time, MP5 charges the start-up capacitor, MN4. With the charging procedure of MN4, transistor MP6 is gradually turned off, which makes the start-up circuit to be broken away from the core of the proposed voltage reference without additional power dissipation. By this method, the proposed voltage reference can work in a desired operating point while avoiding a degeneration point.

Self-Biased Current Generator

The middle part in Fig. 1 is a self-biased current generator, which is based on a MOSFET-only voltage divider. The bias current with positive TC for the whole voltage reference is generated in this part, which is relevant to the medium threshold voltage of NMOS. The unique characteristic of the presented bias current is adopted to realize the proposed voltage reference in a convenient way, which will be analyzed in the “Method” section.

With regard to voltage current characteristic of a transistor in the subthreshold region, the drain current of the transistor in the subthreshold becomes almost independent of V_{DS} with $V_{DS} > 4V_T$, where $V_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, q is the elementary charge, and T is the absolute temperature. Hence, the current can be expressed as:

$$I_D = SI_{SQ} \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \tag{1}$$

where $S = W/L$ is the aspect ratio, m is the subthreshold slope factor, V_{TH} is the threshold voltage, and I_{SQ} represents the specific current and is presented by:

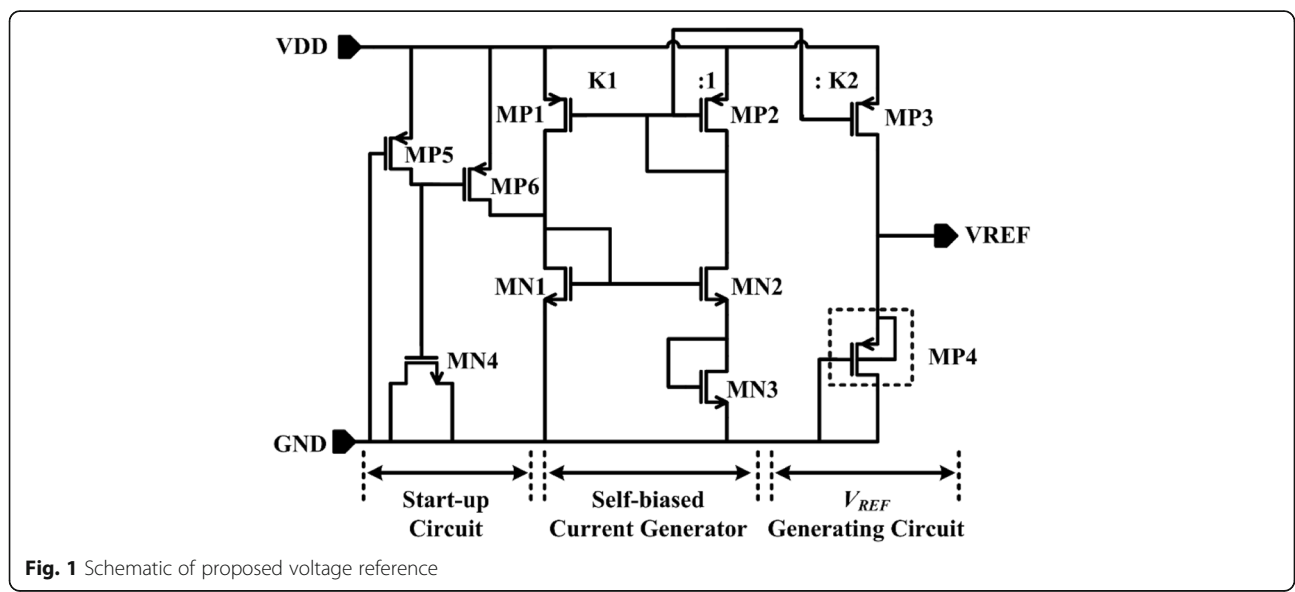


Fig. 1 Schematic of proposed voltage reference

$$I_{SQ} = \mu C_{OX}(m-1)V_T^2 \tag{2}$$

where μ is the carrier mobility and C_{OX} is the oxide capacitance per unit area.

Therefore, the currents through MOSFET-only voltage divider, formed by MN1, MN2, and MN3, can be expressed as follows:

$$I_{D_MN1} = S_{MN1}I_{SQN} \exp\left(\frac{V_{GS_MN1}-V_{THN}}{mV_T}\right) \tag{3}$$

$$I_{D_MN2} = S_{MN2}I_{SQN} \exp\left(\frac{V_{GS_MN2}-V_{THN}}{mV_T}\right) \tag{4}$$

$$I_{D_MN3} = S_{MN3}I_{SQN} \exp\left(\frac{V_{GS_MN3}-V_{THN}}{mV_T}\right) \tag{5}$$

where I_{SQN} is the specific current of NMOS and V_{THN} is the threshold voltage of NMOS.

Since the aspect ratios of MN2 and MN3 are the same and $I_{D_MN2} = I_{D_MN3}$, $V_{GS_MN2} = V_{GS_MN3}$ is guaranteed. This makes $V_{GS_MN1} = 2V_{GS_MN2}$. Besides, the PMOS transistors form the current mirrors and define the current ratios $K_1 = S_{MP1}/S_{MP2}$ and $K_2 = S_{MP3}/S_{MP2}$. The relationship of drain currents between MN1 and MN2 can be expressed as:

$$I_{D_MN1} = K_1 I_{D_MN2} \tag{6}$$

Combined with Eqs. (3)–(6), the V_{GS_MN2} and I_{D_MN2} can be given by:

$$V_{GS_MN2} = mV_T \ln\left(\frac{K_1 S_{MN2}}{S_{MN1}}\right) \tag{7}$$

$$I_{D_MN2} = S_{MN2}I_{SQN} \exp\left(\ln\frac{K_1 S_{MN2}}{S_{MN1}} - \frac{V_{THN}}{mV_T}\right) \tag{8}$$

For the convenience of analysis, Eq. (8) can be abbreviated as:

$$I_{D_MN2} = aT^{2-n_1} \exp\left(b - \frac{V_{THN}}{mV_T}\right) \tag{9}$$

where $a = S_{MN2}\mu_{n0}C_{OX}(m-1)(k/q)^2$ and $b = \ln(K_1 S_{MN2}/S_{MN1})$ are independent of temperature, μ_{n0} is a temperature-independent factor of carrier mobility, and n_1 is the absolute temperature exponent term of carrier mobility, which is usually around 1.5.

As shown in Eq. (9), threshold voltage V_{THN} is complementary to absolute temperature (CTAT), while thermal voltage V_T is proportional to absolute temperature (PTAT). As the temperature increases, $V_{THN}/(mV_T)$ will reduce, so that the positive current characteristics of the bias current will be enhanced.

By this method, a positive TC bias current is achieved by MOSFET-only structure, which carries the characteristics of NMOS threshold voltage.

V_{REF} Generating Circuit

The V_{REF} generating circuit is shown in the right part of Fig. 1, which is only formed by two transistors, MP3 and MP4. Due to the subthreshold region operation, I_{D_MP4} can be written as:

$$I_{D_MP4} = S_{MN4}I_{SQP} \exp\left(\frac{|V_{GS_MP4}| - |V_{THP}|}{mV_T}\right) \tag{10}$$

where I_{SQP} is the specific current of PMOS and V_{THP} is the V_{TH} of PMOS.

Since $I_{D_MP4} = K_2 I_{D_MN2}$, the characteristics of NMOS threshold voltage, V_{THN} , can be transferred to the output node and be superposed with the characteristics of PMOS threshold voltage, V_{THP} . From Eqs. (8) and (10), V_{REF} can be written as:

$$V_{REF} = |V_{THP}| - V_{THN} + mV_T \ln\left(\frac{K_2 S_{MN2} I_{SQn}}{S_{MP4} I_{SQp}}\right) + mV_T \ln\left(\frac{K_1 S_{MN2}}{S_{MN1}}\right) \tag{11}$$

As shown in the first two items of Eq. (11), a delta threshold voltage is realized. Since $V_{TH} = V_{TH0} - \beta T$, where V_{TH0} is the threshold voltage at 0 K and β is the TC of the threshold voltage, the generated delta threshold voltage is a complementary to the absolute temperature (CTAT) voltage with greatly shrunken TC with $|\beta V_{THP}| > \beta V_{THN}$. Besides, two additional PTAT voltages are simultaneously realized and shown in the last two items of Eq. (11), which are adopted to cancel the reduced TC of delta threshold voltage. Therefore, a compacted temperature-stable reference voltage is achieved without a complicated structure, which is stable at $|V_{THP0}| - V_{THN0}$.

Based on the previous analysis, a low-power MOSFET-only voltage reference is realized in this paper which only requires three branches in the core. With the unique characteristics of a self-biased current source, one diode-connected PMOS is adopted to achieve a CTAT voltage with shrunken TC, PTAT voltage generator, and weighted summation at the same time. What is more, the proposed structure is only constructed by MOSFETs, and the generated reference voltage is proportional to the delta threshold voltage. Therefore, the proposed voltage reference is more suitable for low power consumption applications with nanoscale technology, which can be further extended to more advanced technologies.

PSRR of Proposed Voltage Reference

In order to illustrate the PSRR performance, the paths from supply voltage noise to V_{REF} and corresponding equivalent function diagrams are shown in Fig. 2.

Based on Fig. 2, the small-signal model of path 3 is shown in Fig. 3, and the following equation can be obtained:

$$\frac{v_{dd}-v_A}{r_{ds,MP1}} + g_{m,MP1}v_{dd} = \frac{v_A}{r_{ds,MN1}} + g_{m,MN1}v_A \quad (12)$$

From Eq. (12), the expression of the supply noise through path 3 to node A can be given by:

$$Av_{path3} = \frac{v_A}{v_{dd}} = \frac{r_{ds,MN1} + g_{m,MP1}r_{ds,MN1}r_{ds,MP1}}{r_{ds,MP1} + r_{ds,MN1} + g_{m,MN1}r_{ds,MN1}r_{ds,MP1}} \quad (13)$$

The transconductance of the transistor operating in the subthreshold region is $g_m = I_D/mV_T$. Therefore, the

relationship between $g_{m,MP1}$ and $g_{m,MN1}$ with the same current can be given as $g_{m,MP1} = g_{m,MN1}$. Then, Eq. (13) can be simplified as:

$$Av_{path3} \approx 1 \quad (14)$$

Node B also has an effect on node A through path 1, but the effect is opposite to path 3, which can be expressed as:

$$Av_{path1} \approx -1 \quad (15)$$

For $V_A = 2V_{GS,MN2}$, the gain of path 2 is given as:

$$Av_{path2} = -\frac{1}{2}g_{m,MN2} \left(2r_{ds,MN2} \parallel \frac{1}{g_{m,MP2}} \right) \approx -\frac{1}{2} \quad (16)$$

The effect of v_{dd} on node B through path 4 can be written as:

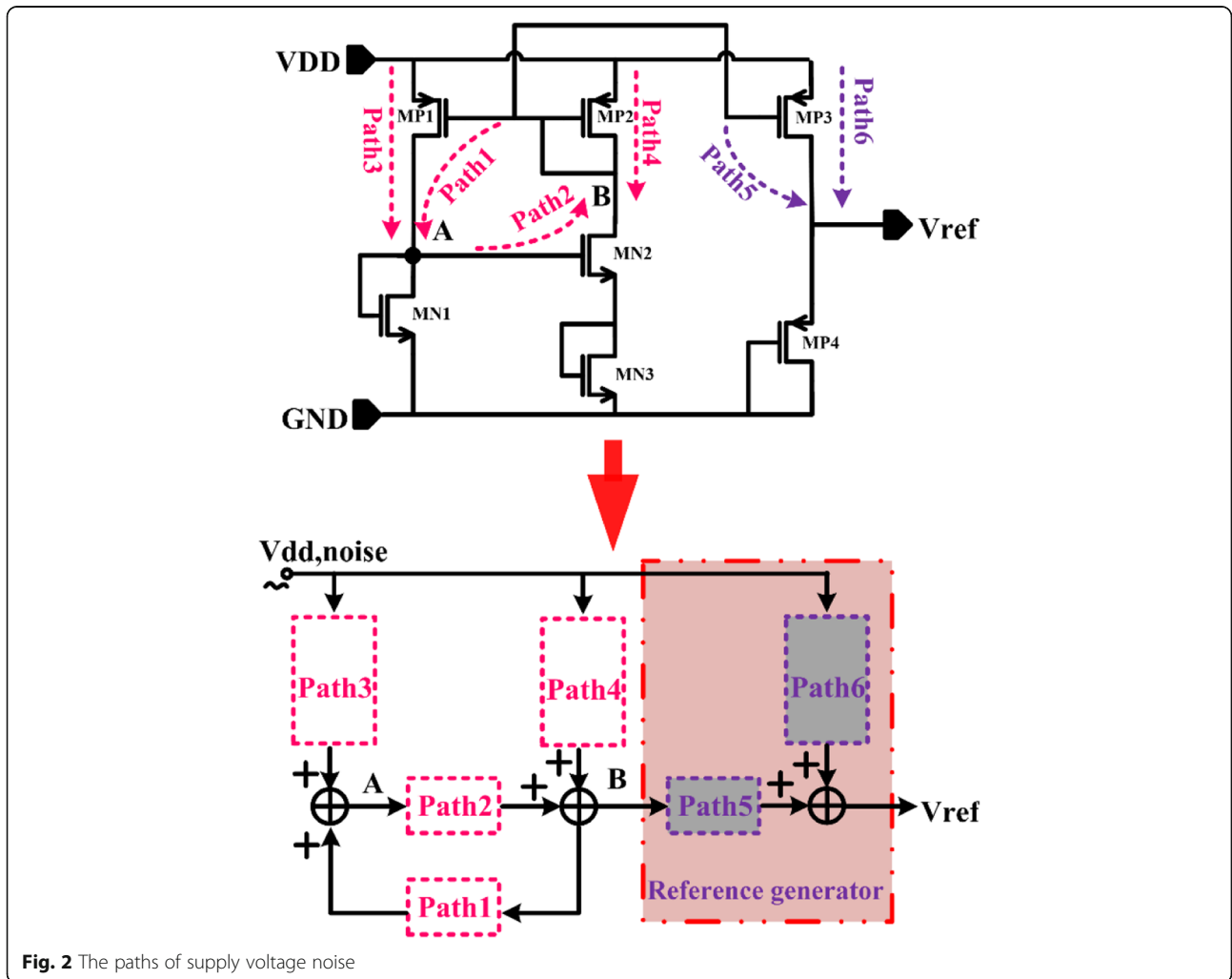
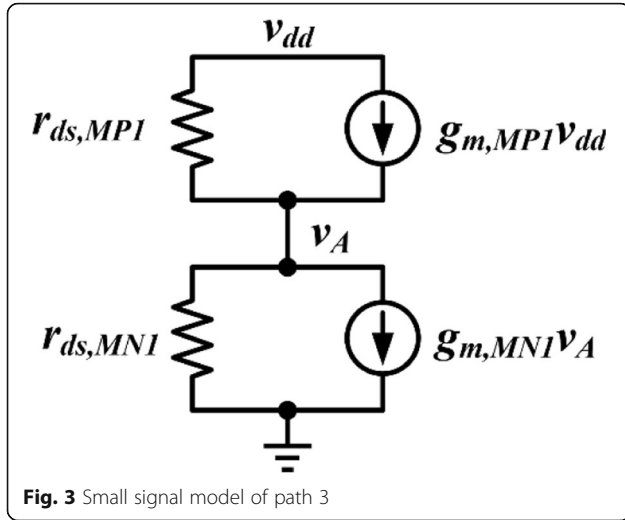


Fig. 2 The paths of supply voltage noise



$$A_{v_{path4}} = \frac{2r_{ds,MN2}}{\left(\frac{1}{g_{m,MP2}}\right) + 2r_{ds,MN2}} = \frac{2g_{m,MP2}r_{ds,MN2}}{1 + 2g_{m,MP2}r_{ds,MN2}} \quad (17)$$

From node A to node B in Fig. 2, two additional equations can be gotten, which are:

$$A_{v_{path4}}v_{dd} + A_{v_{path2}}V_A = V_B \quad (18)$$

$$A_{v_{path3}}v_{dd} + A_{v_{path1}}V_B = V_A \quad (19)$$

According to Eqs.(18) and (19), the noise at V_B can be given by:

$$V_B = \frac{2g_{m,MP2}r_{ds,MN2}-1}{1 + 2g_{m,MP2}r_{ds,MN2}}v_{dd} \approx v_{dd} \quad (20)$$

With the help of the proposed self-biased current source, the output node of the current generator part, B, can track the small-signal variation of the supply voltage, which is beneficial for the PSRR improvement of the whole voltage reference.

With a similar method, the supply noise gains of path 5 and path 6 can be presented by Eqs. (21) and (22), respectively:

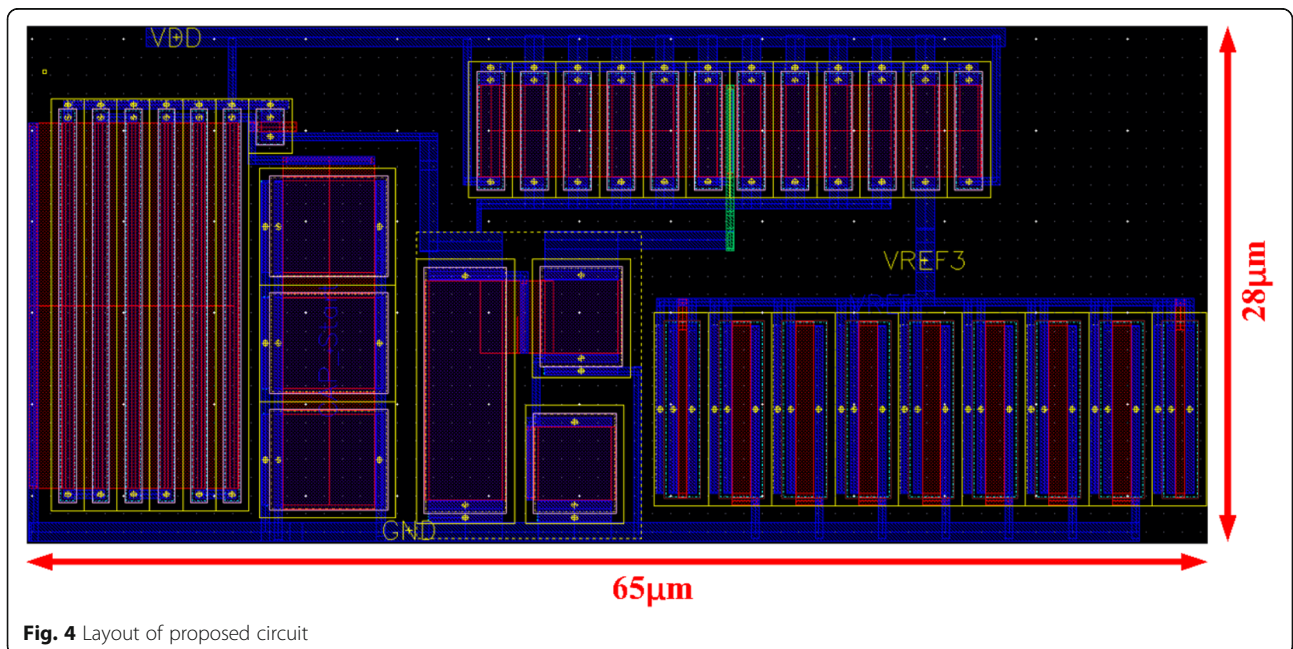
$$A_{v_{path5}} = g_{m,MP3} \left(r_{ds,MP3} \parallel \frac{1}{g_{m,MP4}} \right) \quad (21)$$

$$A_{v_{path6}} \approx 1 \quad (22)$$

Taken into consideration the noise path connection relationship of the reference generator shown in Fig. 2, the effect of the supply noise at the reference voltage, V_{REF} can be determined by path 5 and path 6:

$$\begin{aligned} v_{REF} &= A_{v_{path5}}V_B + A_{v_{path6}}v_{dd} = \frac{1}{1 + g_{m,MP4}r_{ds,MP3}}v_{dd} \\ &= \frac{1}{1 + \frac{\exp(V_{DS,MP3}/V_T)-1}{m}}v_{dd} \end{aligned} \quad (23)$$

For $V_{DS} > 4V_T$, the exponential term in Eq. (23) is very large. This makes the PSRR performance to be greatly



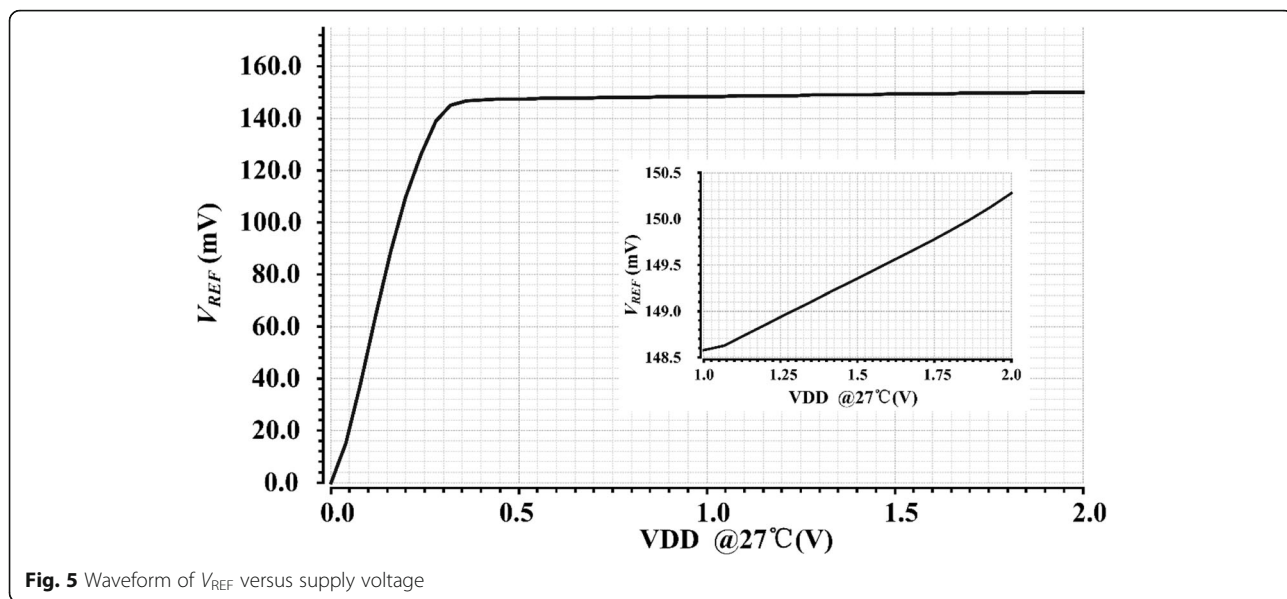


Fig. 5 Waveform of V_{REF} versus supply voltage

enhanced with $V_{DS,MP3}$ increasing. In the proposed design, the minimum $V_{DS,MP3}$ is over 200 mV, which means the change in the supply voltage has little effect on the V_{REF} . Thus, the proposed structure has a good PSRR performance.

Results and Discussion

The voltage reference is implemented in a 65-nm CMOS process, whose layout is shown in Fig. 4 occupying a 0.00182-mm² active area.

Figure 5 shows the line regulation of the proposed voltage reference at 27 °C. As shown in Fig. 5, the minimum supply voltage can be as low as 350 mV, and the generated reference voltage, V_{REF} is around 148 mV. The line sensitivity (LS) is 1.8 mV/V.

The temperature performance of V_{REF} with 350 mV supply voltage is shown in Fig. 6. The TC of V_{REF} is 28 ppm/°C from -30 to 80 °C. V_{REF} shows positive temperature characteristics below -15 °C and above 25 °C,

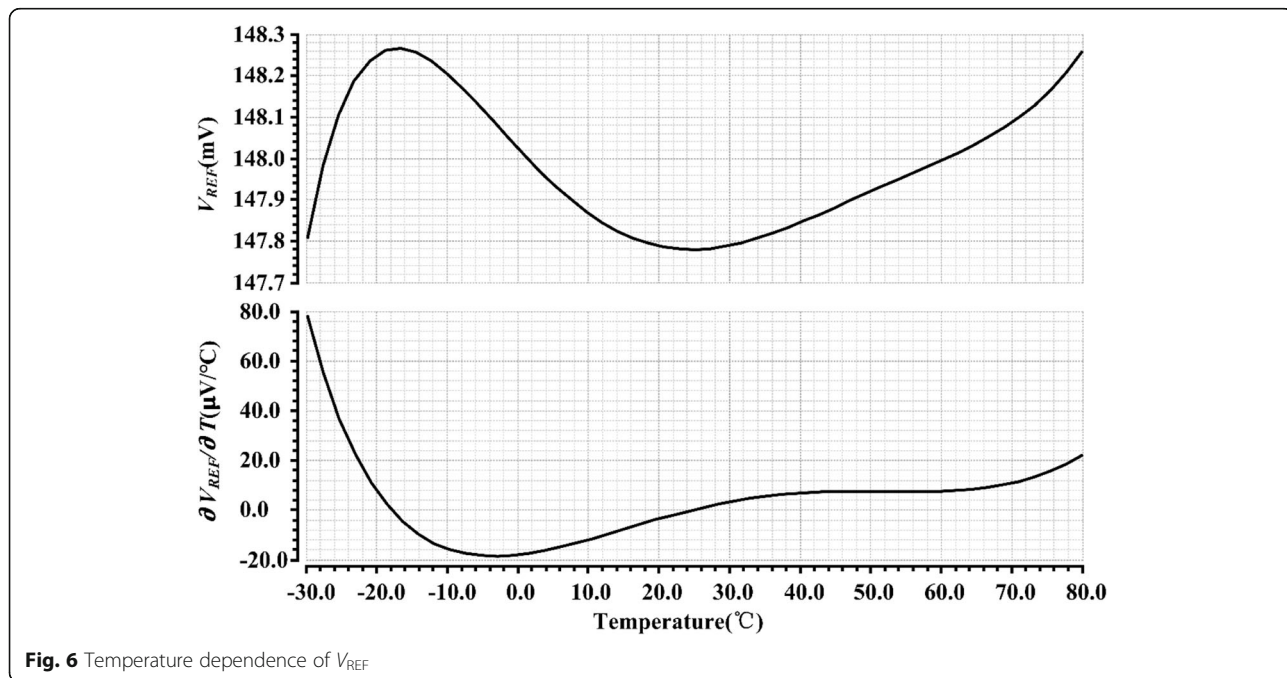


Fig. 6 Temperature dependence of V_{REF}

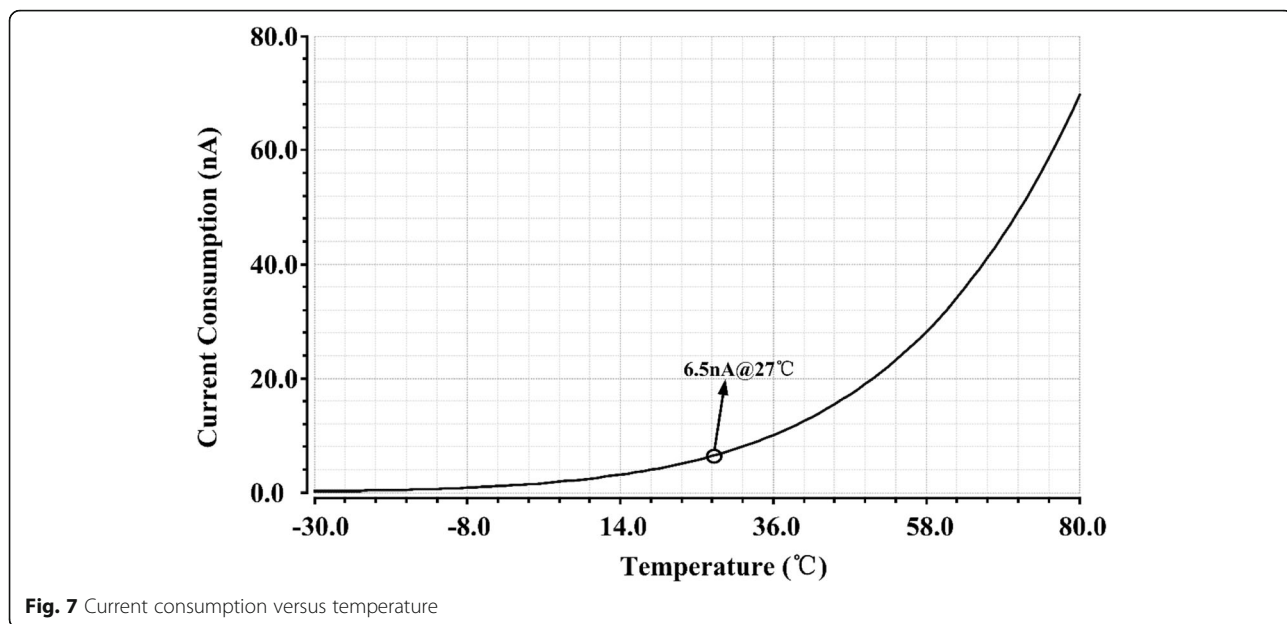


Fig. 7 Current consumption versus temperature

while negative temperature characteristics at medium temperature region.

Figure 7 shows the current consumption versus temperature with 350 mV supply voltage. The current shows a positive TC. The power consumption at room temperature is around 2.28 nW.

Figure 8 shows the result of PSRR at 27 °C with 350 mV supply voltage, where the PSRR without any output filter capacitor is over 53 dB up to 100 Hz. As mentioned above, the PSRR performance can be further improved

with a supply voltage increase, which means the PSRR shown in Fig. 8 is the worst case of the proposed voltage reference.

The distributions of untrimmed V_{REF} at 27 °C with 100 samples is shown in Fig. 9. The mean value and standard deviation of the V_{REF} is 147 mV and 3.97 mV, respectively, which results in a spread (σ/μ) of 2.7%.

Table 1 summarizes the characteristics of the proposed voltage reference and compares it with some previously reported voltage references.

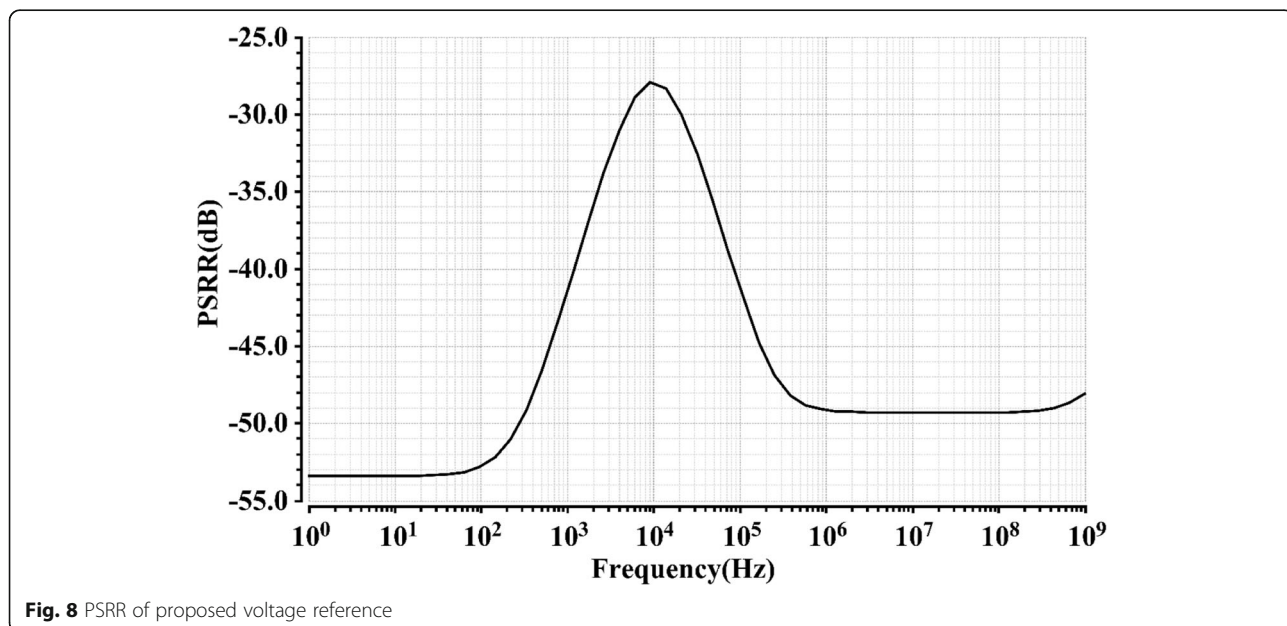
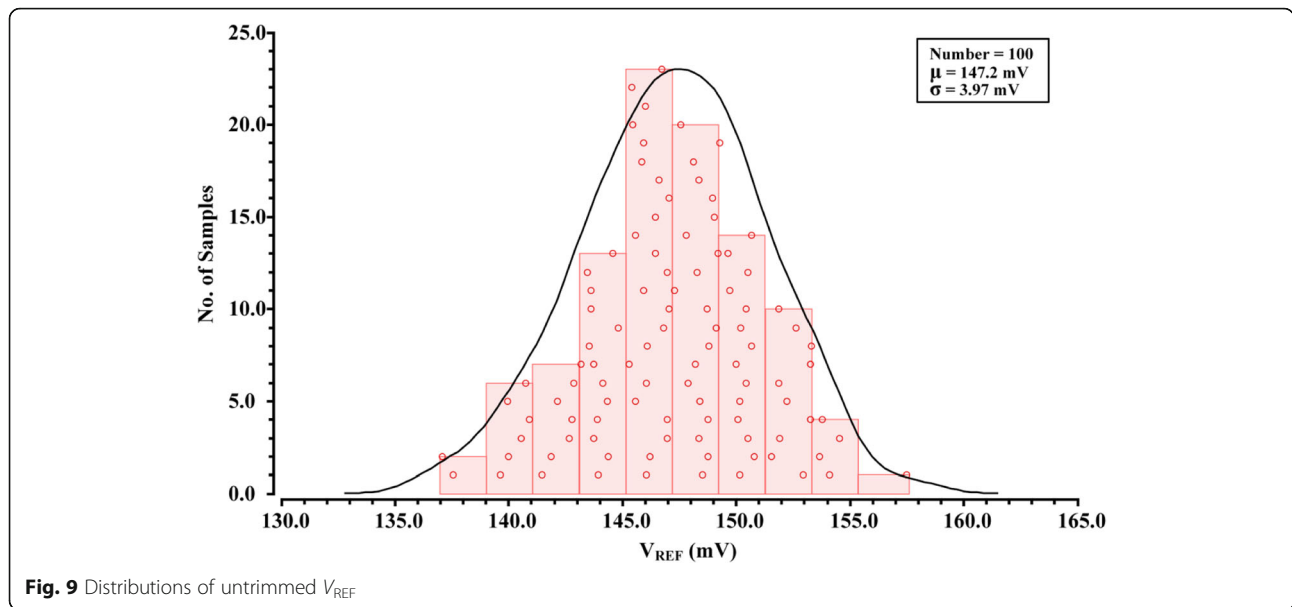


Fig. 8 PSRR of proposed voltage reference



Conclusion

A resistorless low-power voltage reference with high PSRR is presented in this paper, which is suitable for nanoscale applications and can be extended to more advanced process. With the help of self-biased current source based on MOSFET voltage divider, the required CTAT voltage, PTAT voltage, and weighted summation can be simultaneously realized in a compacted structure. What is more, a delta threshold voltage is chosen as the CTAT voltage, which has a greatly reduced negative TC. This also makes the required value of PTAT voltage to be shrunken. Therefore, the supply voltage and current consumption can be brought down. All the parts are only constructed by MOSFETs, which has priority in power-sensitive highly integrated applications, such as SOC.

Table 1 Performance summary and comparison

	This work	[14]	[8]	[9]
Process (nm)	65	130	180	65
Min. VDD (V)	0.35	0.5	1	0.2
Temp. range (°C)	-30 to 80	-40 to 120	-40 to 125	-40 to 85
V_{REF} (mV)	148	216	755	89.73
TC (ppm/°C)	28	192	49.6	790
Power (nW)	2.28	113	23	9.7
PSRR (dB) @100 Hz	-53	-27	-52	-42
LS (%/V)	1.2	13.7	0.524	2.01
Area (mm ²)	0.00182	0.0016	0.0162	0.01

Abbreviations

BGR: Bandgap reference; CTAT: Complementary to absolute temperature; hvt: High threshold voltage; LS: Line sensitivity; mvt: Medium threshold voltage; PSRR: Power supply rejection ratio; PTAT: Proportional to absolute temperature; TC: Temperature coefficient

Acknowledgements

Not applicable.

Funding

This work was supported by the National Science Foundation of China under Grant No. 61674025 and No. 61306035, the Fundamental Research Funds for the Central Universities under Grant No. ZYGX2016J056, and Open Projects of Sichuan Key Laboratory of Meteorological Information and Signal Processing under Grant No. QXXCSYS201504 and No. QXXCSYS201603.

Availability of Data and Materials

All data generated or analyzed during this study are included in this published article.

Authors' Contributions

ZZ proposed the novel structure and was a major contributor in writing the manuscript. JC improved the design of the circuit. YW verified the theory with a simulation. The others authors offered comments and revised the manuscript. All authors read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

Publisher's Note

Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Author details

¹State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, Sichuan, China. ²College of Communication Engineering, Chengdu University of Information Technology, Chengdu 610225, China.

Received: 17 December 2018 Accepted: 14 January 2019

Published online: 24 January 2019

References

1. Zhou Z, Shi Y, Huang Z, Zhu P, Ma Y, Wang Y, Chen Z, Ming X, Zhang B (2012) A 1.6-V 25- μ A 5-ppm/ $^{\circ}$ C curvature compensated bandgap reference. *IEEE Trans. Circuits Syst. I, Reg. Papers* 59(4):677–684. <https://doi.org/10.1109/TCSI.2011.2169732>
2. Ma B, Yu F (2014) A novel 1.2-V 4.5-ppm/ $^{\circ}$ C curvature-compensated CMOS bandgap reference. *IEEE Trans Circuits Syst I, Reg. Papers*. <https://doi.org/10.1109/TCSI.2013.2286032>
3. Banba H, Shiga H, Umezawa A, Miyaba T, Tanzawa T, Atsumi S, Sakui K (1999) A CMOS bandgap reference circuit with sub-1-V operation. *IEEE J Solid State Circuits*. <https://doi.org/10.1109/4.760378>
4. Chahardori M, Atarodi M, Sharifkhani M (2011) A sub 1 V high PSRR CMOS bandgap voltage reference. *Microelectron J*. <https://doi.org/10.1016/j.mejo.2011.06.010>
5. Buck AE, McDonald CL, Lewis SH, Viswanathan TR (2002) A CMOS bandgap reference without resistors. *IEEE J Solid State Circuits*. <https://doi.org/10.1109/4.974548>
6. Andreou CM, Koudounas S, Georgiou J (2012) A novel wide temperature-range, 3.9 ppm/ $^{\circ}$ C CMOS bandgap reference circuit. *IEEE J Solid State Circuits*. <https://doi.org/10.1109/JSSC.2011.2173267>
7. de Oliveira AC, Cordova D, Klimach HD, Bampi S (2017) A 0.45 V, 93 pW temperature-compensated CMOS voltage reference. *Circuits & Systems IEEE*. <https://doi.org/10.1109/LASCAS.2017.7948051>
8. Zhang H, Liu X, Zhang J, Zhang H, Li J, Zhang R, Chen S, Carusone AC et al (2017) *IEEE transactions on Circuits & Systems II express Briefs*. <https://doi.org/10.1109/TCSII.2017.2654441>
9. De Streeel, Guericc, J. De Vos, D. Bol. A Delta V_T 0.2V to 1V 0.01mm² 9.7nW Voltage Reference in 65nm LP/GP CMOS. *Soi-3d-subthreshold Microelectronics Technology Unified Conference IEEE*. 2015; doi: 10.1109/S3S.2015.7333486.
10. Zhou Z-k, Shi Y, Gou C, Wang X, Wu G, Feng J-f, Wang Z, Zhang B (2016) A resistorless low-power voltage reference. *IEEE Transactions on Circuits & Systems II Express Briefs*. <https://doi.org/10.1109/TCSII.2016.2530096>
11. Hoon SK, Chen J, Maloberti F (2002) An improved bandgap reference with high power supply rejection. in *Proc IEEE Int Symp Circuits Syst*. <https://doi.org/10.1109/ISCAS.2002.1010833>
12. Tham K-M, Nagaraj K (1995) A low supply voltage high PSRR voltage reference in CMOS process. *IEEE J Solid State Circuits*. <https://doi.org/10.1109/4.384173>
13. Li W, Yao R, Guo L (2009) A low power CMOS bandgap voltage reference with enhanced power supply rejection. *Proc IEEE 8th Int.Conf. ASIC* doi: 10.1109/ASICON.2009.5351450
14. Campana RV, Klimach H, Bampi S (2016) 0.5 V supply resistorless voltage reference for low voltage applications. *Integrated circuits and systems design*. *IEEE*. <https://doi.org/10.1145/2800986.2800987>

Submit your manuscript to a SpringerOpen[®] journal and benefit from:

- Convenient online submission
- Rigorous peer review
- Open access: articles freely available online
- High visibility within the field
- Retaining the copyright to your article

Submit your next manuscript at ► springeropen.com