High mobility Ge pMOSFETs with amorphous Si passivation: impact of surface orientation

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Abstract

We report the amorphous Si passivation of Ge pMOSFETs fabricated on (001)-, (011)-, and (111)-orientated surfaces for advanced CMOS and thin film transistor applications. Amorphous Si passivation of Ge is carried out by magnetron sputtering at room temperature. With the fixed thickness of Si t_{Si}, (001)-oriented Ge pMOSFETs achieve the higher on-state current I_{ON} and effective hole mobility μ_{eff} compared to the devices on other orientations. At an inversion charge density Q_{inv} of 3.5×10^{12} cm^{-2}, Ge(001) transistors with 0.9 nm t_{Si} demonstrate a peak μ_{eff} of 278 cm^2/V × s, which is 2.97 times higher than the Si universal mobility. With the decreasing of t_{Si}, I_{ON} of Ge transistors increases due to the reduction of capacitive effective thickness, but subthreshold swing and leakage floor characteristics are degraded attributed to the increasing of midgap D_{it}.

Keywords: Germanium, MOSFET, Amorphous Si passivation, Mobility, Surface orientation

Background

Germanium (Ge) has been attracting tremendous research interests for advanced CMOS and thin film transistor applications due to its higher hole mobility and lower thermal budget processing compared to Si [1–6]. To achieve the high channel mobility, the surface passivation process leading to a high interface quality is required before gate stack formation. Several surface passivation techniques have been developed to deliver the carrier mobility benefits in Ge metal-oxide-semiconductor field-effect transistors (MOSFETs) [1, 2, 7–10]. Among these techniques, a silicon (Si) cap passivated on Ge has been the hotspot in recent years, due to its advantages of effective suppressing of interface states and good thermal stability and reliability [11]. Formation of Si passivation cap has been widely studied using chemical vapor deposition (CVD) with precursors of SiH$_4$ [1], Si$_2$H$_6$ [4], Si$_3$H$_8$ [12], and E-beam evaporation [13]. Although CVD method could provide the more uniform passivation layer over physical vapor deposition (PVD), its passivation rate has the strong correlation in channel surface orientation and the process
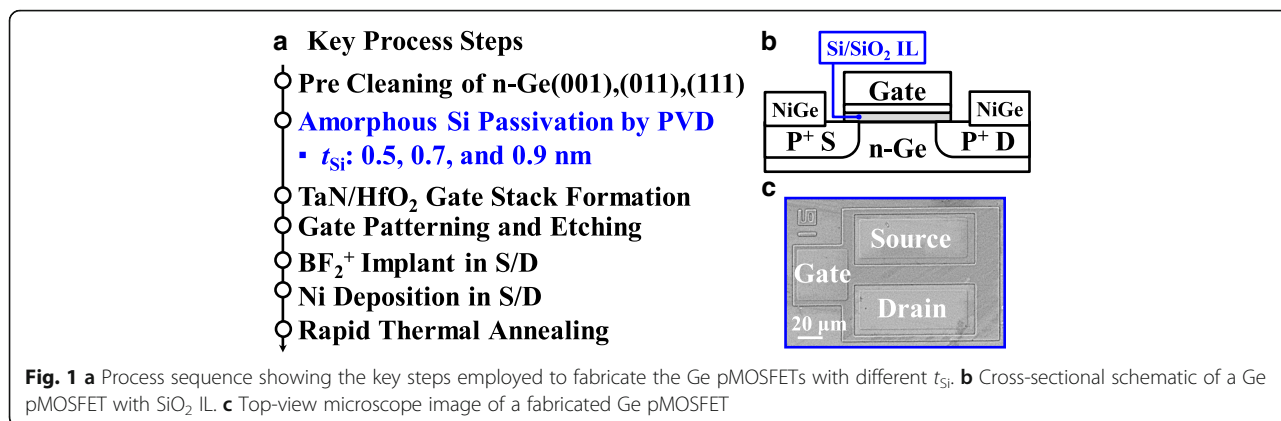
temperature. PVD technique could provide the improved passivation rate even at room temperature, which has the advantages of low thermal budget and low cost, making it more suitable for the thin film transistors and back-end-of-line 3D integration applications. In this letter, we fabricated high mobility Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces utilizing amorphous Si passivation by magnetron sputtering. Significantly improved effective hole mobility μ_{eff} is achieved in Ge transistors compared to the Si universal mobility. Impacts of surface orientation and thickness of amorphous Si t_{Si} on the boosting effect of amorphous Si passivation on μ_{eff} are studied.

Methods

Figure 1a shows the key process steps for fabricating Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces. After pre-gate cleaning in diluted HF (1:50) solution, ultrathin amorphous Si passivation layer was deposited on n-Ge substrates by magnetron sputtering at a target power of 50 W. Three passivation durations of 60 s, 80 s, and 100 s were used corresponding to the deposition of 0.5, 0.7, and 0.9 nm t_{si}, respectively. After that, a 5-nm thick HfO$_2$ gate dielectric was deposited at 250 °C by atomic layer deposition using TDMAHf and H$_2$O as precursors of Hf and O, respectively. A 50-nm

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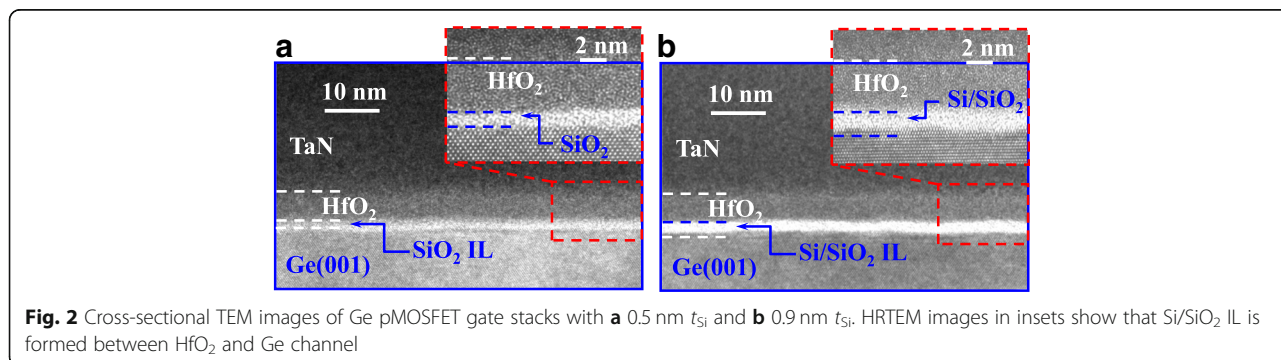Full list of author information is available at the end of the article

a Key Process Steps

- Pre Cleaning of n-Ge(001),(011),(111)
- Amorphous Si Passivation by PVD
  - t_{Si}: 0.5, 0.7, and 0.9 nm
- TaN/HfO$_2$ Gate Stack Formation
- Gate Patterning and Etching
- BF$_2^+$ Implant in S/D
- Ni Deposition in S/D
- Rapid Thermal Annealing

Fig. 1 a Process sequence showing the key steps employed to fabricate the Ge pMOSFETs with different t_{Si}. **b** Cross-sectional schematic of a Ge pMOSFET with SiO$_2$ IL. **c** Top-view microscope image of a fabricated Ge pMOSFET

TaN gate electrode was deposited by reactive sputtering. Next, the gate electrode was patterned and etched, which was followed by BF$_2^+$ implantation into source/drain (S/D) regions at 30 KeV with a dose of 1×10^{15} cm^{-2}. Non-self-aligned S/D metals of 15-nm nickel were formed by lift-off process. Finally, rapid thermal annealing at 400 °C was carried out for dopant activation and S/D metallization. Figure 1b shows the cross-sectional schematic of the Ge pMOSFET with Si/SiO$_2$ interfacial layer (IL). Figure 1c shows top-view microscope image of a fabricated Ge pMOSFET.
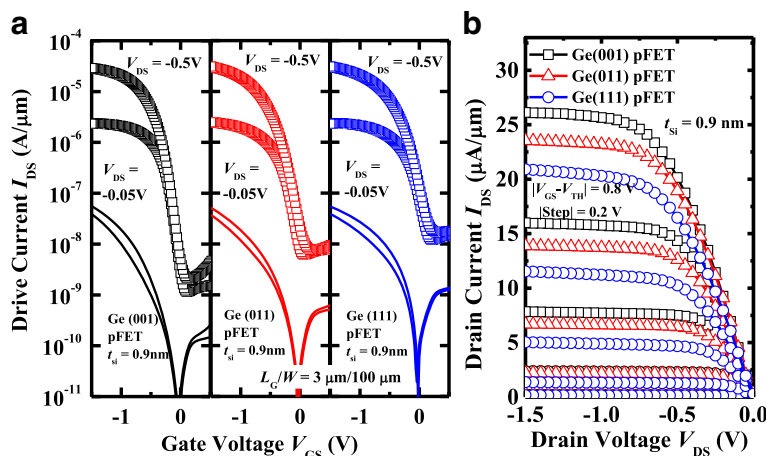
Figure 2a, b shows the transmission electron microscope (TEM) images of the high-κ/metal gate stack with SiO$_2$/Si interfacial layer (IL) on Ge(001) channel with t_{Si} of 0.5 and 0.9 nm, respectively. Insets show the high-resolution TEM (HRTEM) images of the samples. For the device with a t_{Si} of 0.5 nm, amorphous Si layer was completely oxidized, while for the device with 0.9 nm t_{Si}, about two Si monolayers remained after the subsequent annealing steps.

Results and discussion

Figure 3a plots the measured I_{DS}-V_{GS} and I_G-V_{GS} curves of the typical Ge pMOSFETs on (001)-, (011)-, and (111)-oriented surfaces with 0.9 nm t_{Si}, which show the excellent transfer characteristics. All transistors have a

gate length L_G of 3 μm and a gate width W of 100 μm. The channel direction is [110] for all the orientations. The I_{DS}-V_{DS} curves of the devices measured at different gate overdrive V_{GS}-V_{TH} are shown in Fig. 3b. Here, threshold voltage V_{TH} is defined as the V_{GS} at I_{DS} of 10^{-7} A/μm. It is observed that Ge(001) pMOSFET achieves the higher drive current I_{ON} compared to the transistors on (011) and (111) surfaces at the fixed V_{GS}-V_{TH}. Later, we will show that this is attributed to the fact that Ge(001) pMOSFETs have a higher effective hole mobility μ_{eff} in comparison with the devices on the other two surface orientations. We perform a comprehensive comparison of electrical performance for the devices with the fixed t_{Si} of 0.9 nm, including I_{ON}, leakage floor I_{leak}, subthreshold swing (SS), and V_{TH} characteristics. I_{leak} is defined as the minimum I_{DS} at V_{DS} of -0.05 V. Figure 4a presents the statistical plot of the I_{ON} for Ge pMOSFETs on various orientations, and I_{ON} was defined as I_{DS} at a V_{DS} of -0.5 V and a V_{GS}-V_{TH} of -0.8 V. All the transistors in this plot have the L_G of 3 μm and W of 100 μm. (001)-oriented devices exhibit the improved mean I_{ON} as compared to those on (011) and (111) orientations, which is attributed to the higher μ_{eff}. Figure 4b compares the I_{leak} for the devices, showing that Ge(001) transistors have the lowest I_{leak} of them, and Ge(011) pMOSFETs have the lower I_{leak} than

Fig. 2 Cross-sectional TEM images of Ge pMOSFET gate stacks with **a** 0.5 nm t_{Si} and **b** 0.9 nm t_{Si}. HRTEM images in insets show that Si/SiO$_2$ IL is formed between HfO$_2$ and Ge channel

Fig. 3 a Measured I_{DS}-V_{GS} and I_G-V_{GS} curves of (001)-, (011)-, and (111)-oriented Ge pMOSFETs with 0.9 nm t_{Si} showing the excellent transfer characteristics. **b** I_{DS}-V_{DS} curves measured at different V_{GS}-V_{TH} for the devices

(111)-oriented devices. It should be noted that the I_{leak} is determined by the reverse current of the p^+/n junction in drain region, which is affected by the background n-type doping concentration in Ge substrate and activation of the implanted p^+ dopants. The n-type doping concentrations in the wafers with various orientations are not exactly the same. The surface orientation affects the dopant activation rate and recrystallization quality of S/D regions. Furthermore, although the I_G is lower than I_{DS} before the turn-on of the transistors, it would influence the I_{leak}. Similarly, (001)-oriented Ge pMOSFETs demonstrate the improved SS characteristics in comparison with other two orientations, which is due to that transistors on (001) surface have the lower midgap density of interface state D_{it} compared to the other devices. Figure 4d shows that the devices on different orientations have the different V_{TH}. Based on the results in Fig. 4, it is concluded that, with the fixed t_{Si} of 0.9 nm, (001)-oriented Ge pMOSFETs obtain the best electrical characteristics.

The thicknesses of Si/SiO$_2$ IL in transistors with 0.9 nm t_{Si} on different surface orientations are studied by using inversion capacitance C_{inv} versus V_{GS} measurement, as shown in Fig. 5. Forward and reverse sweeping measurements exhibit the negligibly small hysteresis in the devices. The transistors exhibit the similar magnitude of C_{inv}, ~ 1.56 μF/cm^2, corresponding to the capacitive effective thickness (CET) of 2.2 nm. Figure 5b show the statistical results of saturated C_{inv} for the devices, which demonstrate the very small difference in C_{inv} in the transistors on different surface orientations. This indicates that the passivation rate of amorphous Si by magnetron sputtering is independent of the surface orientation. The rule of left-right shifts of the C_{inv}-V_{GS} curves is well consistent with that of V_{TH} for the devices in Fig. 4d, which might be

induced by the slightly different doping concentration in different orientation substrates.

Figure 6 compares the mobility characteristics of the transistors with 0.9 nm t_{Si} on various surface orientations. The μ_{eff} was extracted using a total resistance slope-based method [14]. Ge(001) pMOSFETs exhibit the much higher channel mobility compared to the devices on (011) and (111) orientations. Transistors on (001) substrate achieve a peak μ_{eff} of 278 cm^2/V·s at an inversion charge density Q_{inv} of ~ 3.5×10^{12} cm^{-2}, which is 2.97 times higher than the Si universal mobility. Surface roughness at the Si/Ge interface and density of interface states (D_{it}) can affect μ_{eff} of the devices at high inversion carrier density. It is unlikely that the commercially purchased Ge wafers with various surface orientations have the obvious difference in surface roughness. Therefore, it is speculated that the mobility enhancement in (001)-oriented devices is mainly due to reduced carrier scattering contributed by interface states. In this work, we evaluate the midgap D_{it} of the devices, and with the fixed t_{Si} of 0.9 nm, the (001)-oriented Ge pMOSFETs indeed have the lower midgap D_{it} compared to the other orientations.

The impact of t_{Si} on the electrical performance of Ge pMOSFETs is also investigated. Figure 7a, b present the measured I_{DS}-V_{GS} and I_{DS}-V_{DS} curves, respectively, of the (111)-oriented Ge pMOSFETs with t_{Si} of 0.5, 0.7, and 0.9 nm at a V_{DS} of − 0.05 and − 0.5 V. The transistors have a L_G of 1.5 μm. It is observed that Ge pMOSFETs with 0.9 nm t_{Si} exhibit improved transfer characteristics compared to the devices with thinner t_{Si}, but I_{ON} of the device decreases with the increasing of t_{Si}. At V_{DS} of − 1.5 V and V_{GS}-V_{TH} of − 0.8 V, Ge(111) pMOSFET with 0.5 nm t_{Si} demonstrates a 32% improvement in I_{ON} compared to the device with 0.9
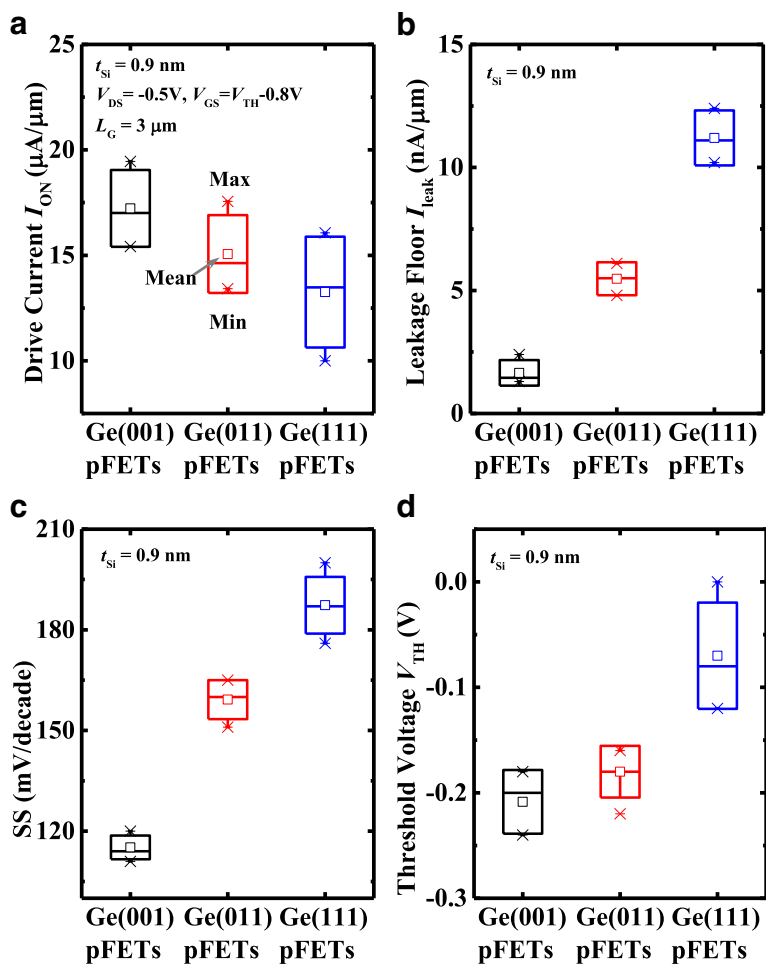
Fig. 4 Comparison of **a** I_{ON}, **b** I_{leak}, **c** SS, and **d** V_{TH} for (001)-, (011)-, and (111)-oriented Ge pMOSFETs with a t_{Si} of 0.9 nm
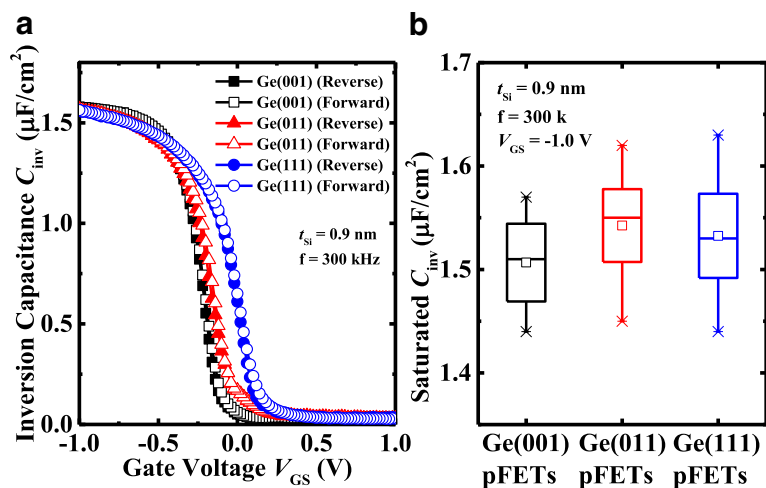

Fig. 5 a Comparison of inversion C_{inv}-V_{GS} curves among the Ge pMOSFETs with 0.9 nm t_{Si} on different orientations. Both forward and reverse sweeping are shown. **b** Statistical plots for the saturated C_{inv} of the devices showing the negligible differences in C_{inv} in the inversion regime
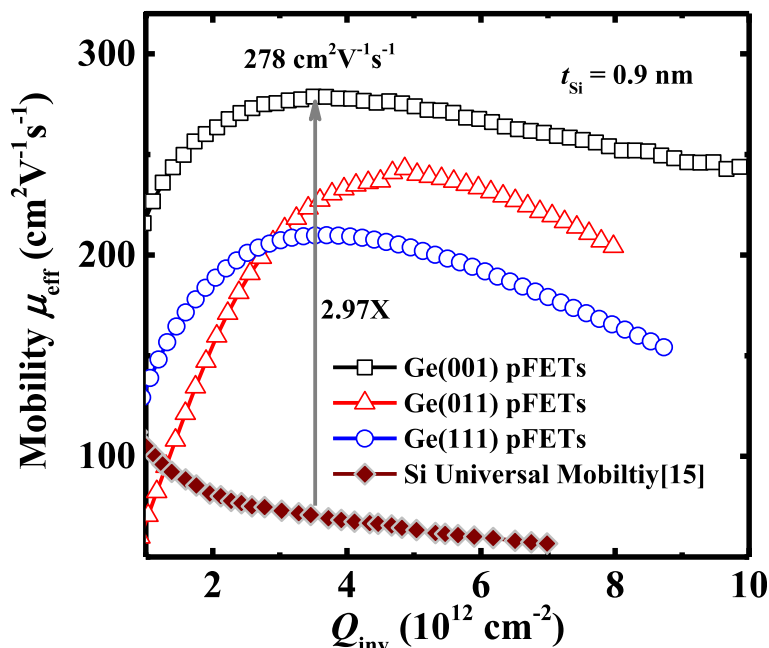
Fig. 6 Plot of μ_{eff} versus Q_{inv} for Ge pMOSFETs with 0.9 nm t_{Si} on (001)-, (011)-, and (111)-oriented substrates. Ge(001) pMOSFETs achieve the 2.97 times enhancement in μ_{eff} at a Q_{inv} of 3.5×10^{12} cm^{-2} as compared to the Si universal mobility. The μ_{eff} was extracted using a total resistance slope-based method [17]

nm t_{Si}. Figure 8 plots the statistical results of I_{ON}, I_{leak}, SS, and V_{TH} of the Ge pMOSFETs on (111)-orientation with different t_{Si}. From Fig. 8a, we see that transistors with 0.5 nm t_{Si} achieve the improved I_{ON} in comparison with the devices with thicker t_{Si}, which is due to the transistor with 0.5 nm t_{Si} that has a smaller CET, leading to a higher C_{inv}. It is noticed that I_{leak} decreases with the increasing of t_{Si} (Fig. 8b), and transistors with 0.5 nm t_{Si} has the inferior SS characteristics

to those of the devices with 0.7 and 0.9 nm amorphous Si passivation layer (Fig. 8c). This might be due to those transistors with 0.5 nm t_{Si} having a higher midgap D_{it}. The relation between SS and midgap D_{it} of Ge pMOS-FET can be expressed by SS = $\ln(10) \cdot (kT/q) \cdot [1 + (C_{it} + C_d)/C_{ox}]$, where C_{ox}, C_d, and C_{it} are oxide capacitance, depletion-layer capacitance, and capacitance from interface traps, respectively. C_{it} can be calculated by $q \times D_{it}$, were D_{it} is the interface trap density. Although transistor
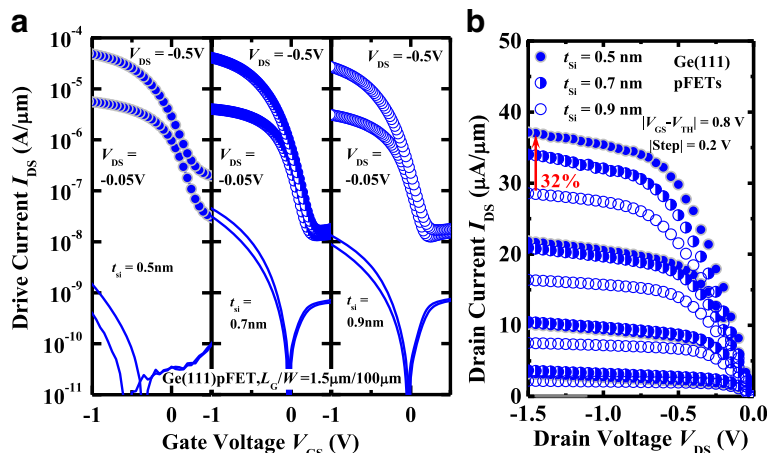
Fig. 7 a I_{DS}-V_{GS} and I_G-V_{GS} and **b** I_{DS}-V_{DS} curves of Ge(111) pMOSFETs with various t_{Si}. Transistor with 0.5 nm t_{Si} exhibits a 32% improvement in I_{ON} compared to the device with 0.9 nm t_{Si} at V_{DS} of − 1.5 V and V_{GS}-V_{TH} of − 0.8 V
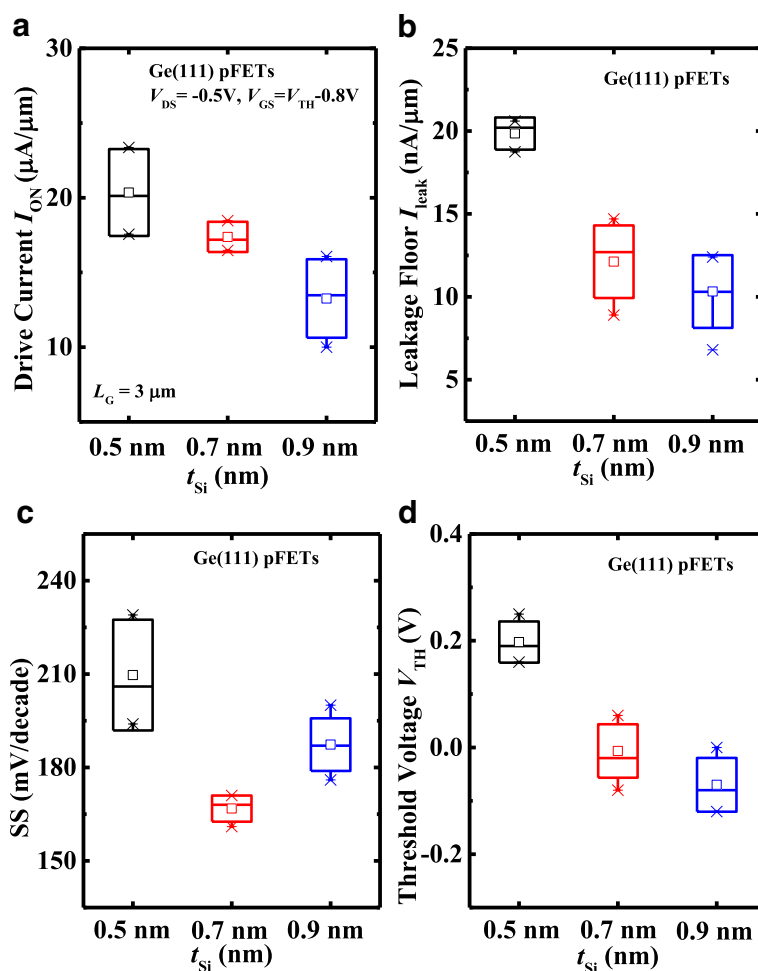
Fig. 8 Comparison of **a** I_{ON}, **b** I_{leak}, **c** SS, and **d** V_{TH} for (111)-oriented Ge pMOSFETs with 0.5, 0.7, and 0.9 nm t_{Si} showing that transistors with 0.5 nm t_{Si} have the better I_{ON}, but worse SS and I_{leak} characteristics in comparison with devices with thicker t_{Si}

with 0.5 nm t_{Si} has the larger C_{ox} compared to the other two devices, its higher midgap D_{it} can lead to the inferior SS to the devices with the thicker t_{Si}. The surface passivation will also affect the I_{leak} from drain to source. With the sweeping of V_{GS} from position to negative, the channel transfers from accumulation mode to inversion mode. However, if the D_{it} is high, some points in channel surface are pinned by the interface traps, and the leakage paths can be formed, increasing I_{leak} from drain to source. As shown in Fig. 8d, Ge(111) pMOSFETs show the shift of V_{TH} to negative V_{GS} direction with the increasing of t_{Si}, which is attributed to the increased CET. In addition, the density of traps in the lower bandgap half seems to increase for the thinner t_{Si}, which might lead to the shift of V_{TH} [2].

Figure 9a shows the C_{inv} as a function of V_{GS} curves for the Ge pMOSFETs on (111)-oriented surface with t_{Si} of 0.5, 0.7, and 0.9 nm measured at a frequency of 300 kHz. The CET values in inversion regions are extracted to be 1.8, 1.9, and 2.2 nm for the devices with 0.5, 0.7,

and 0.9 nm t_{si}, respectively. μ_{eff} as a function of Q_{inv} characteristics of the devices are extracted and shown in Fig. 9b. The (111)-oriented Ge pMOSFET with 0.7 nm t_{si} achieves the highest peak mobility of 229 cm^2/V s, which is 2.27 times higher compared to the Si universal mobility. It should be noted that the devices with 0.5 nm t_{Si} exhibit a significantly improved μ_{eff} over the transistors with thicker t_{Si} at high Q_{inv} (e.g. 10^{13} cm^{-2}). This also leads to the higher I_{ON} at high V_{GS}-V_{TH} in the devices with 0.5 nm t_{Si} compared to the devices with 0.7 and 0.9 nm t_{Si}. The μ_{eff} at high Q_{inv} decreases as t_{Si} increases from 0.5 nm to 0.7~0.9 nm, which is attributed to the fact that the larger surface roughness leads to the stronger surface roughness scattering of the carriers. During the passivation of Ge surface using magnetron sputtering at room temperature, the diffusion of surface atoms is greatly suppressed. So with the increasing of t_{Si}, the surface roughness is larger, which can be observed from the HRTEM images in Fig. 2.
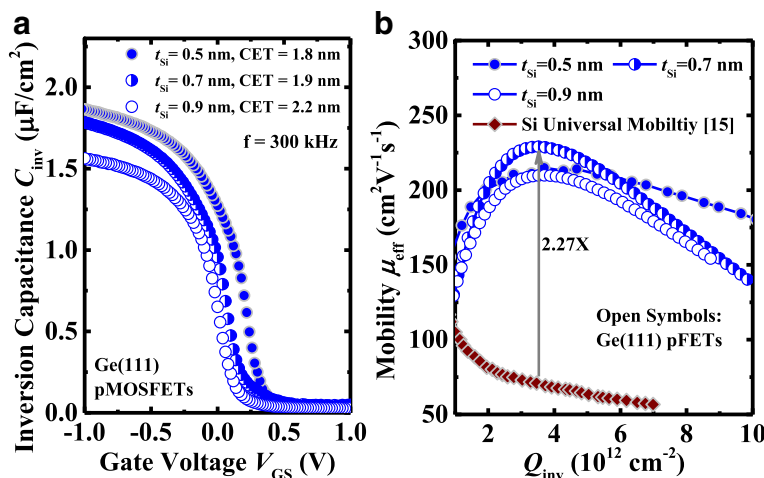
Fig. 9 a C_{inv}-V_G characteristics measured at 300 kHz for (111)-oriented devices with 0.5, 0.7, and 0.9 nm t_{Si}. **b** μ_{eff} as a function of Q_{inv} for Ge pMOSFETs [17]

In Fig. 10, we benchmark the μ_{eff} of the Ge pMOS-FETs in this work with those of the reported relaxed Ge transistors with Si by E-beam evaporation, SiH_4, Si_2H_6, and Si_3H_8 passivation. Compared to the amorphous Si by E-beam evaporation in Ref. [15], Ge pMOSFETs in this work exhibit the significantly improved μ_{eff}. It is seen that, at the similar CET, Ge pMOSFETs utilizing amorphous Si passivation by magnetron sputtering have the lower μ_{eff} in comparison with the devices with Si_2H_6 passivation. The process of passivation using amorphous Si needs to be further optimized to enhance the carrier mobility.
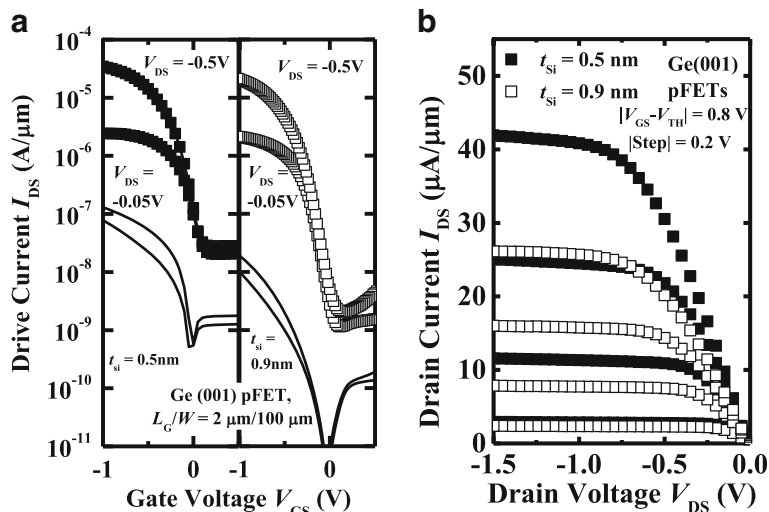
Ge pMOSFETs with the different t_{Si} on (001)-oriented surface are also characterized. Figure 11a, b illustrate the measured I_{DS}-V_{GS} and I_{DS}-V_{DS} curves, respectively, of a pair of Ge(001) pMOSFETs with 0.5 and 0.9 nm t_{Si}. Similar to the (111)-oriented devices, Ge(001) pMOSFET with 0.5 nm t_{Si} obtains the improvement in I_{ON} but the degradation in I_{leak} compared to the transistor with 0.9 nm t_{Si}.

The midgap D_{it} characteristics of Ge pMOSFETs are studied by the method in [16], and values of D_{it} are calculated by $D_{it} = [SSlog(e)/(kT/q) - 1]C_G/q$, [16] where q is the electron charge, k is Boltzmann's constant, T is the absolute temperature, and C_G is the measured gate capacitance per unit area. Figure 12 shows D_{it} as a function of the thickness of amorphous Si with various Ge surface orientations. For (111)-oriented surface, a device with 0.7-nm t_{Si} has the lowest D_{it} value. With the 0.9 nm t_{Si}, (001)-oriented device has the lower D_{it} compared to the transistors on other orientations.
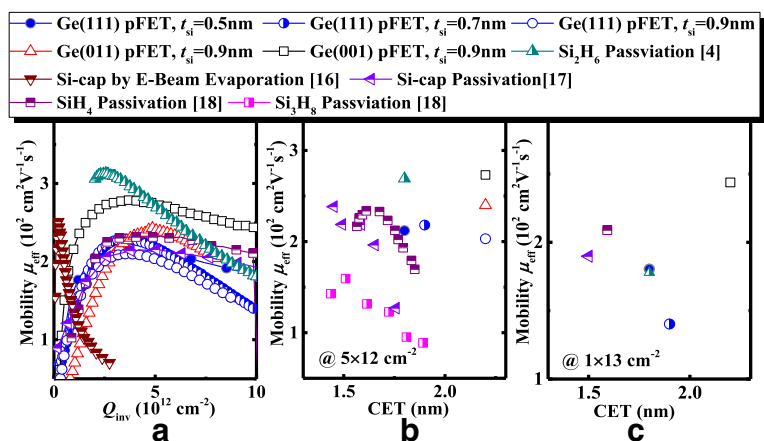
Fig. 10 a μ_{eff} for the Ge pMOSFETs in this work vs. the published results for relaxed Ge pMOSFETs. **b, c** Benchmarking of μ_{eff} extracted at $Q_{inv} = 5 \times 10^{12}$ and 1×10^{13} cm^{-2}, respectively, of the Ge pMOSFETs with the different CET values [18, 19]

**Fig. 11 a** Measured I_{DS}-V_{GS} and I_G-V_{GS} curves of (001)-oriented Ge pMOSFETs with 0.5 and 0.9 nm t_{Si}. **b** I_{DS}-V_{GS} curves of the devices

Finally, we compare the key electrical characteristics of Ge pMOSFETs on the different orientations in Table 1. With a fixed t_{Si}, Ge(001) pMOSFET has the improved electrical performance compared to the other two orientations. The drive current can be enhanced by reducing the t_{Si} from 0.9 nm to 0.5 nm, which is due to that the thinner t_{Si} provides a significantly reduced CET without causing degradation in μ_{eff}.

Conclusions

Ge pMOSFET passivated by amorphous Si are demonstrated on (001)-, (011)-, and (111)-oriented substrate. With a t_{Si} of 0.9 nm, the improved I_{ON} and SS characteristics are obtained in (001)-oriented Ge pMOSFETs in comparison with the devices on (011) and (111) orientations, due to the higher μ_{eff} and lower midgap D_{it}. Ge(001) pMOSFETs with 0.9 nm t_{Si} achieve a peak
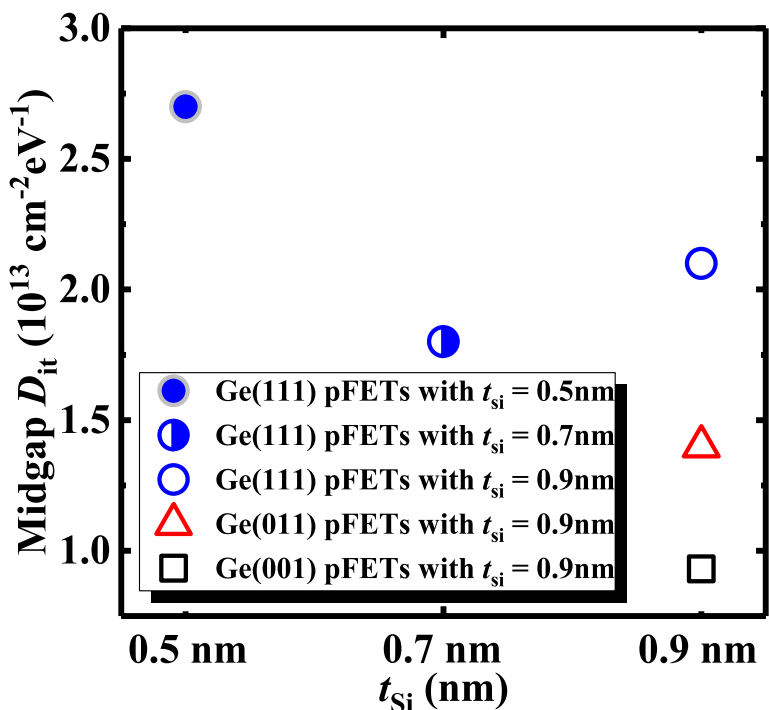
Fig. 12 D_{it} versus the thickness of amorphous Si with various Ge surface orientations

Table 1 Key electrical performance of Ge pMOSFETs on the different orientations

Substrate orientation	t_{Si} (nm)	CET (nm)	Midgap D_{it} ($cm^{-2} eV^{-1}$)	SS (mV/decade)	$I_{ON}@V_{DS} = -0.5$ V, V_{GS}-$V_{TH} = -0.8$ V ($L_G = 3$ μm) (μA/μm)	I_{leak} (nA/μm)	$\mu_{eff}@$ $Q_{inv} = 5 \times 10^{12}$ cm^{-2} ($cm^2/V \times s$)
(001)	0.9	2.2	9.3×10^{12}	115	17.2	1.6	273
(011)	0.9	2.2	1.4×10^{13}	159	15.1	5.5	240
(111)	0.9	2.2	2.1×10^{13}	187	13.2	10.7	203
(111)	0.7	1.9	1.8×10^{13}	166	17.3	12.3	218
(111)	0.5	1.8	2.7×10^{13}	209	20.3	19.8	212

mobility of $278 \, cm^2/V$ s at a Q_{inv} of $3.5 \times 10^{12} \, cm^{-2}$, which is 2.97 times higher than the Si universal mobility. It is demonstrated that I_{ON} of the devices is improved with the decreasing of t_{Si} due to the reduction of CET. But Ge pMOSFETs with thicker t_{Si} exhibit the superior subthreshold swing and leakage floor, owing to that midgap D_{it} can be reduced by increasing t_{Si}.

Abbreviations
ALD: Atomic layer deposition; BF_2^+: Boron fluoride ion; CET: Capacitive effective thickness; Ge: Germanium; GeO_x: Germanium oxide; HF: Hydrofluoric acid; HfO_2: Hafnium dioxide; HRTEM: High-resolution transmission electron microscope; IL: Interfacial layer; MOSFETs: Metal-oxide-semiconductor field-effect transistors; Ni: Nickel; Si: Silicon; SS: Subthreshold swing; TaN: Tantalum nitride; TDMAHf: Tetrakis (dimethylamido) hafnium

Authors' contributions
HL carried out the experiments and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. XST and JCY helped to carry out the measurements. YH provided constructive advice in the drafting. All the authors read and approved the final manuscript.

Competing interests
The authors declare that they have no competing interests.

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References
1. Wu N, Zhang Q, Zhu C, Chan DSH, Du A, Balasubramanian N, Li MF, Chin A, Sin JKO, Kwong DL (2004) A TaN-HfO₂-Ge pMOSFETs with novel SiH₄ surface passivation. IEEE Electron Device Lett 25:631–633
2. Mitard J, Jaeger BD, Leys FE, Hellings G, Martens K, Eneman G, Brunco DP, Loo R, Lin JC, Shamiryan D, Vandeweyer T, Winderickx G, Vrancken E, Yu CH, Meyer KD, Caymax M, Pantisano L, Meuris M, Heyns M (2008) Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability. In: IEDM Tech Dig, pp 873–876 https://doi.org/10.1109/IEDM.2008.4796837
3. Vincent B, Loo R, Vandervorst W, Delmotte J, Douhard B, Valev VK, Vanbel M, Verbiest T, Rip J, Brijs B, Conard T, Claypool C, Takeuchi S, Zaima S, Mitard J, Jaeger BD, Dekoster J, Caymax M (2011) Si passivation for Ge pMOSFETs: impact of Si cap growth conditions. Solid State Electron 60:116–121
4. Liu Y, Yan J, Han GQ, Wang HJ, Liu MS, Zhang CF, Cheng BW, Hao Y (2014) Strained Ge₀.₉₆Sn₀.₀₄ P-channel MOSFETs with in situ low temperature Si₂H₆ surface passivation. In: ISTDM Tech Dig, pp 107–108 https://doi.org/10.1109/ISTDM.2014.6874637
5. Liao CY, Chen SH, Huang WH, Shen CH, Shieh JM, Cheng HC (2018) High-performance recessed-channel germanium thin-film transistors via excimer laser crystallization. IEEE Electron Device Lett 39:367–370
6. Sadoh T, Kamizuru H, Kenjo A, Miyao M (2006) Low-temperature formation (< 500 °C) of poly-Ge thin-film transistor with NiGe Schottky source/drain. Appl Phys Lett 89:192–114
7. Xie R, Phung TH, He W, Sun Z, Yu M, Cheng Z, Zhu C (2008) High mobility high-k/Ge pMOSFETs with 1 nm EOT-new concept on interface engineering and interface characterization. In: IEDM Tech Dig, pp 1–4 https://doi.org/10.1109/IEDM.2008.4796703
8. Takagi S, Noguchi M, Kim M, Kim SH, Chang CY, Yokoyama M, Nishi K, Zhang R, Ke M, Takenaka M (2016) III-V/Ge MOS device technologies for low power integrated systems. Solid State Electron 125:82–102
9. Kuzum D, Pethe AJ, Krishnamohan T, Saraswat KC (2009) Ge (100) and (111) N-and P-FETs with high mobility and low-T mobility characterization. IEEE Trans Electron Devices 56:648–655
10. Hashemi P, Hoyt JL (2012) High hole-mobility strained-Ge/Si₀.₆Ge₀.₄ p-MOSFETs with high-K metal gate: role of strained-Si cap thickness. IEEE Electron Device Lett 33:173–175
11. Kaczer B, Franco J, Mitard J, Roussel PJ, Veloso A, Groeseneken G (2009) Improvement in NBTI reliability of Si-passivated Ge/high-k/metal-gate pFETs. Microelectronic Eng 86:1582–1584
12. Mitard J, Martens K, Jaeger BD, Franco J, Shea C, Plourde C, Leys FE, Loo R, Hellings G, Eneman G, Wang WE, Lin JC, Kaczer B, DeMeyer K, Hoffmann T, DeGendt S, Caymax M, Meuris M, Heyns MM (2009) Impact of epi-Si growth temperature on Ge-pFET performance. In: European Solid State Device Research Conference, pp 411–414 https://doi.org/10.1109/ESSDERC.2009.5331351
13. Chen WB, Chin A (2010) High performance of Ge nMOSFETs using SiO₂ interfacial layer and TiLaO gate dielectric. IEEE Electron Device Lett 31:80–82
14. Niu G, Cressler JD, Mathew SJ, Subbanna S (1999) A total resistance slope-based effective channel mobility extraction method for deep submicrometer CMOS technology. IEEE Trans Electron Devices 46:1912–1914
15. Lee CH, Nishimura T, Tabata T, Wang SK, Nagashio K, Kita K, Toriumi A (2010) Ge MOSFETs performance: impact of Ge interface passivation. In: IEDM Tech Dig, pp 416–419 https://doi.org/10.1109/IEDM.2010.5703384
16. Greve DW (1998) Field effect devices and application: devices for portable, low-power, and imaging systems, 1st edn. Prentice-Hall, Englewood
17. Takagi S, Twase M, Toriumi A (1998) On the universality of inversion-layer mobility in n-and p-channel MOSFETs. In: IEDM Tech Dig, pp 398–401 https://doi.org/10.1109/IEDM.1988.32840

18. Pillarisetty R, Chu-Kung B, Corcoran S, Dewey G, Kavalieros J, Kennel H, Kotlyar R, Le V, Lionberger D, Metz M, Mukherjee N, Nah J, Rachmady W, Radosavljevic M, Shah U, Taft S, Then H, Zelick N, Chau R (2010) High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (V_{cc} = 0.5 V) III-V CMOS architecture. In: IEDM Tech. Dig, pp 150–153 https://doi.org/10.1109/IEDM.2010.5703312
19. Mitard J, Witters L, Vincent B, Franco J, Eavia P, Hikavyy A, Eneman G, Loo R, Brunco DP, Kabir N, Bender H, Sebaai F, Vos R, Mertens P, Milenin A, Vecchio E, Ragnarsson L-Å, Collaert N, Thean A (2013) First demonstration of strained Ge-in-STI IFQW pFETs featuring raised SiGe75% S/D, replacement metal gate and germanided local interconnects. In: VLSIT Dig, pp T20–T21