Wang et al. Nanoscale Research Letters (2017) 12:306
DOI 10.1186/s11671-017-2080-2

Nanoscale Research Letters

NANO EXPRESS Open Access

pMOSFETs Featuring ALD W Filling Metal Using SiH_4 and B_2H_6 Precursors in 22 nm Node CMOS Technology

Guilei Wang[1,2*], Jun Luo[1,2], Jinbiao Liu[1], Tao Yang[1], Yefeng Xu[1], Junfeng Li[1], Huaxiang Yin[1,2], Jiang Yan[1], Huilong Zhu[1], Chao Zhao[1,2*], Tianchun Ye[1,2] and Henry H. Radamson[1,2,3]

Abstract

In this paper, pMOSFETs featuring atomic layer deposition (ALD) tungsten (W) using SiH_4 and B_2H_6 precursors in 22 nm node CMOS technology were investigated. It is found that, in terms of threshold voltage, driving capability, carrier mobility, and the control of short-channel effects, the performance of devices featuring ALD W using SiH_4 is superior to that of devices featuring ALD W using B_2H_6. This disparity in device performance results from different metal gate-induced strain from ALD W using SiH_4 and B_2H_6 precursors, i.e. tensile stresses for SiH_4 (~2.4 GPa) and for B_2H_6 (~0.9 GPa).

Keywords: ALD W, High-*k* and metal gate (HKMG), Nano-beam diffraction (NBD), Threshold voltage (V_t), Mobility

Background

As continuous downscaling of complementary metal-oxide semiconductor (CMOS) into sub 20 nm nodes, strain engineering is utilized as an important technique to boost device performance [1]. There are a number of ways to exert strain to the channel, such as integrating SiGe or SiC as stressor material in source and drain region [2–6], stress memorization technology (SMT) [7], dual stress liners (DSL) [8], and metal gate stress technology (MGS). Among these techniques, MGS is attracting tremendous attention because of its easy integration with the state-of-the-art high-*k* and metal gate (HKMG)-last integration scheme and its effectiveness in inducing strain to the channel [9]. Initially, Intel utilized Al and TiN material as the filling metal in the gate region to induce compressive strain to enhance the performance of in 45 nm node n-MOSFET transistors [10]. However, as the aspect ratio of dummy gate trench became larger in 22 nm and beyond nodes, filling the trench without voids or seams by conventional Al metal confronted overwhelming challenge. Consequently, thanks to a good step coverage and conformity W metal using atomic layer deposition (ALD) emerges as a competitive candidate in filling the dummy gate trench [1, 11]. ALD W process was firstly developed by using precursors, Si_2H_6 and WF_6 at 325 °C [12].

At this time, B-doped W metal layers using B_2H_6 and WF_6 precursors have been systematically investigated by Kim et al. [13]. Later, more detailed studies about ALD W using SiH_4 or B_2H_6 have been performed in terms of trench filling capability, threshold voltage vulnerability, and film adhesion during chemical mechanical polishing (CMP) [14–16]. However, ALD W as gate filling metal in real transistors and its impact on the channel stress is not systematically studied yet.

This work presents pMOSFETs of 25-nm gate length with HKMG-last and ALD W using SiH_4 or B_2H_6 precursors as the gate filling metal. The effect of induced strain by metal gate on the performance of pMOSFETs featuring ALD W filling metal is also investigated. In this case, the impact of ALD W metal gate film stress modulation mechanism for device electrical performance could be discussed. This study can provide a foundation for ALD W film materials, which is very valuable for advanced transistor.

* Correspondence: wangguilei@ime.ac.cn; zhaochao@ime.ac.cn
[1]Key laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China
Full list of author information is available at the end of the article

Methods

The fabrication process flow of pMOSFETs is summarized in Fig. 1. The original material was 8-in. p-type (100) Si wafers. After the formation of N-well and shallow trench isolation (STI), dummy poly-Si gate of approximately 25-nm gate length was deposited and patterned by electron beam lithography (EBL). Followed by sequential spacer formation, Ni-Pt (5%) self-aligned silicidation, and the deposition of pre-metal dielectric, CMP to open the poly-Si dummy gate was performed. Upon removing the dummy gate by tetramethylammonium hydroxide (TMAH) and interfacial oxide layer by diluted HF, a 20-Å-thick HfO_2 was deposited by ALD. Metal stack, i.e. ALD TiN/PVD Ti/CVD TiN, was then deposited as work function metals for pMOSFETs. Afterwards, 750-Å-thick ALD W films using SiH_4 or B_2H_6 precursors were deposited to fill the gate trench. The ALD W films were deposited in Applied Centura iSPIRIT tungsten WxZ ALD chamber at 300 °C. The whole device fabrication was finished by metallization and forming gas annealing (FGA) at 425 °C.

At first, a few test samples were grown on blanket wafers containing two layers of TiN (10 nm)/SiO_2 (300 nm)—followed by 75-nm ALD W film. The induced stress by ALD W films was evaluated by the difference in the radius of the wafer curvature. The difference in the radius of curvature before and after ALD W film deposition was carefully determined by laser reflection. X-ray diffraction (XRD) was performed to identify the phase of ALD W films. Cross-sectional transmission electron microscopy (TEM) images of fabricated pMOSFETs with ALD W as gate filling metal are also displayed in Fig. 1. The electrical characterization was carried out using a HP4156C precision semiconductor parameter analyser.

Nano-beam diffraction (NBD) technique in TEM was applied to provide advanced nano-scale information. These analyses were performed in combination with True Crystal Strain Analysis package program to find out the strain distribution along a vertical line starting from the channel region down to the areas deeper in the transistor body. The distributions of strain induced from W gate in the Si channel were studied using technology computer-aided design (TCAD) simulations.

Results and Discussion

In Fig. 2, the XRD spectra of ALD W using SiH_4 and B_2H_6 and calculated stress data on blanket substrates are shown. It is seen that the ALD W using SiH_4 has a higher tensile stress (~2.4 GPa) due to its polycrystalline phase whereas ALD W using B_2H_6 has a lower tensile stress (~0.9 GPa) due to its amorphous phase [17, 18]. Meanwhile, if these ALD W films with tensile stress are filled in the gate trench in a transistor structure, compressive strain along the channel direction will be induced. The ALD W filled at two sidewalls and at the bottom of gate trench tends to shrink and to "squeeze" two bottom corners, giving rise to compressive strain to the channel [19]. Consequently, enhanced hole mobility as well as improved electrical performance of as-fabricated pMOSFETs is realized, as will be elucidated later.

The stress in the channel region was also measured directly on the transistor structures using NBD technique. Figure 3 shows the three sets of NBD images from device cross section including metal gate, channel,

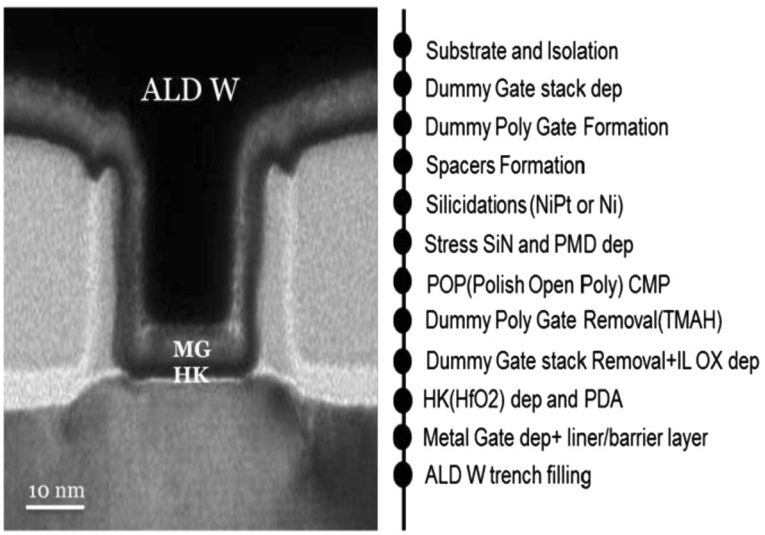

Fig. 1 The fabrication process flow of pMOSFETs using HKMG-last integration scheme. Cross-sectional scanning electron microscopy images of fabricated pMOSFETs are also shown

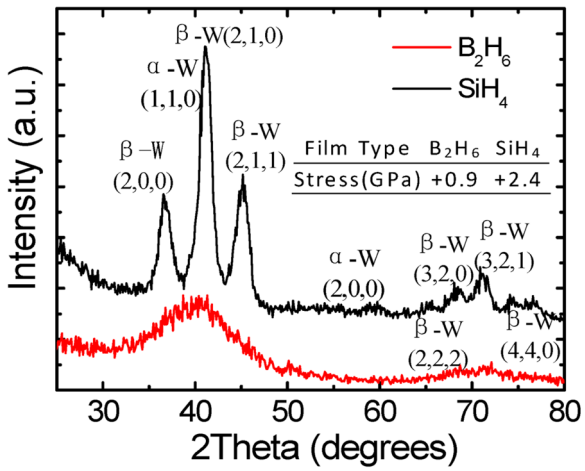

Fig. 2 XRD spectra of ALD W using SiH_4 and B_2H_6 and calculated stress data on blank substrate

and reference regions of transistors where gate formed by ALD W using SiH_4 and B_2H_6. The diffraction images from the metal gate materials show that Airy rings indicate polycrystalline material in agreement with XRD results. Meanwhile, ALD W using B_2H_6 has a pattern with weak intensity which is a sign of poor polycrystalline likely an amorphous phase.

In order to study the strain force from the W gate to Si channel, NBD analysis was performed and compared with a crystal part deep inside the transistor structure as a reference point. The idea behind NBD analysis is that the strain force causes a distortion of Si lattice constant or the change of interplanar distance of (220) planes. Therefore, a comparison between the measured and theoretically calculated data may reveal the stress amount. In this analysis, the software True Crystal program was applied to determine the lattice distortion. Later, the strain amount (σ) is converted into the stress (ε) by applying $\varepsilon = \sigma / E$ where E is Young's modulus. It is worth mentioning here that the source of strain is W gate but the strain in the Si channel is important. In this case, the applied E value for Si <100> direction (~200 GPa for a load amount of 15 mN) was used [20]. The estimated stress values were ~1 GPa for ALD W using SiH_4 and ~0.5 GPa for ALD W using B_2H_6. The latter stress value is lower than the blanket samples measured by laser. A plausible reason may relate to strain relaxation during processing or sample preparation for TEM. But regardless to these reasons, the amount of stress in ALD W using SiH_4 is almost double compared to ALD W using B_2H_6.

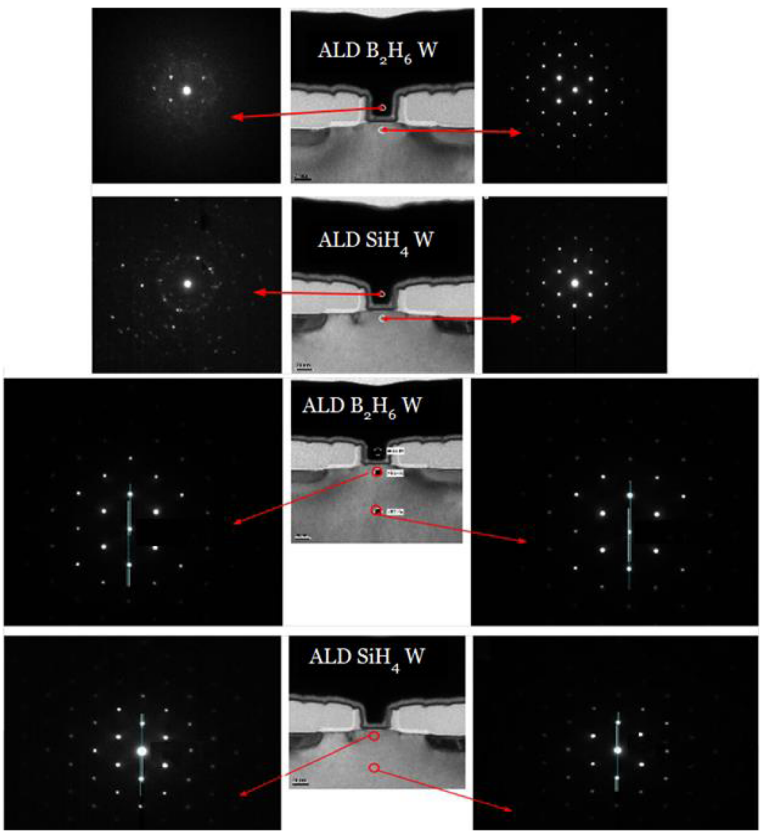

Fig. 3 NBD images from metal gate, channel, and the reference regions of the transistors

TCAD simulation was performed to compare the strain effect by two ALD W metal electrodes filling in the trench, as shown in Fig. 4. The actual simulation parameters included the dimensions of pMOSFETs. The input parameters were 25 and 50 nm for the gate length and height, respectively. The other key process parameters were set according to the real device structure. The simulation results of stress profiles showed that the tensile ALD W using SiH_4 has a higher strain in the channel region for high-*k* and metal gate-last pMOSFETs. It was seen that the channel strain profile is non-uniformly distributed in the channel region with compressive stress amount of ~0.7 and ~1.3 GPa for ALD W metal electrodes (ME) using B_2H_6 and SiH_4, respectively.

For fabricated pMOSFETs with different ALD W as gate filling metal, the I_d-V_g and I_d-V_d characteristics are shown in Fig. 5. In the inset of Fig. 5a, basic device parameters are summarized. It is seen that the electrical performance of devices filled with different ALD W shows obvious deviations. Approximately 7% improvement of I_{on} can be accomplished for pMOSFETs filled with ALD W using SiH_4 (703 μA/μm at $V_{ds} = V_{gs} = -1.0$ V), as compared to devices filled with ALD W using B_2H_6 (580 μA/μm at $V_{ds} = V_{gs} = -1.0$ V). The threshold voltage (V_t), drain-induced barrier lowering (DIBL), and subthreshold swing (SS) for devices filled with ALD W using SiH_4 are smaller, i.e. −0.20 V, 98 mV/V, and 88 mV/dec,

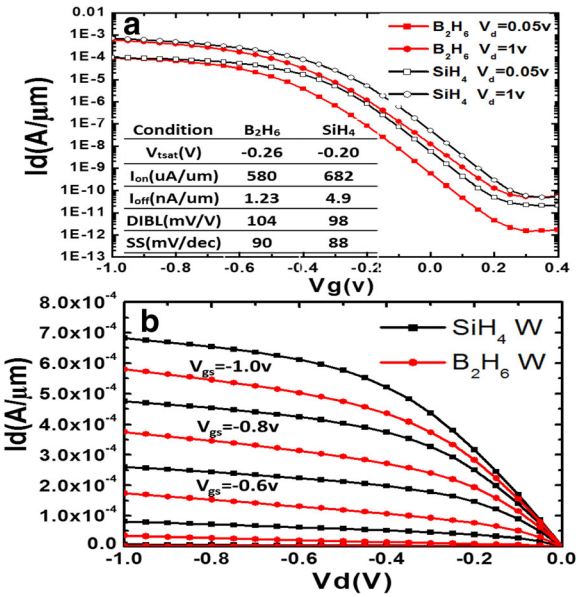

Fig. 5 **a** I_d-V_g and **b** I_d-V_d characteristics of fabricated pMOSFETs with ALD W as gate filling metal. Basic device parameters are extracted and shown in the *inset* of **a**

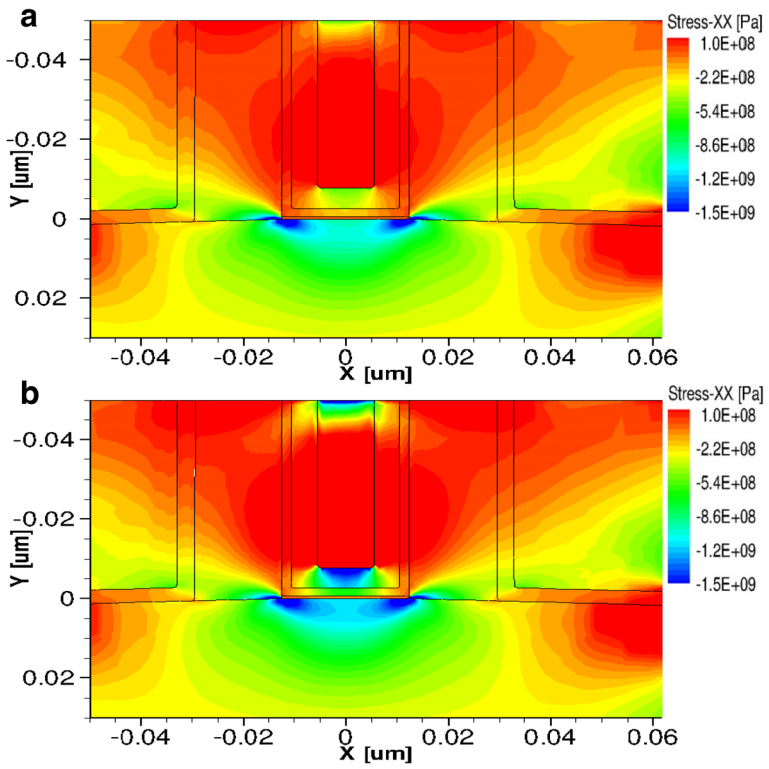

Fig. 4 The TCAD simulation of strain distribution in the channel by **a** tensile ALD W using B_2H_6 and **b** tensile ALD W using SiH_4 filled in the trench

respectively, than those for devices filled with ALD W using B_2H_6, i.e. –0.26 V, 104 mV/V, and 90 mV/dec, respectively. The superior driving capability and improved short-channel effect immunity as well as less negative V_t value for devices filled with ALD W using SiH_4 than using B_2H_6 can be attributed to the strain effect. According to the deformation potential theory, the strain-induced bandgap narrowing, electron affinity, and density of states are the mainly reason for the V_t shift of MOSFETs [21]. The value of V_t shift depends on the amount of stress applied along the channel direction, especially for the channel compressed by a high stress [22]. It is worth noting that the shift of V_t to positive direction with large stress is consistent with previous work [23].

In Fig. 6a, the mobility of pMOSFETs filled with different ALD W versus effective electrical field is shown. The figure shows that the mobility of devices filled with ALD W using SiH_4 is 1.3 times larger than that using B_2H_6, which is also in good accordance with the larger stress in Fig. 2 as well as superior driving capability in Fig. 5. Compared to devices filled with ALD W using B_2H_6, the 30% improvement on mobility for devices filled with ALD W using SiH_4, however, does not lead to equivalent improvement on I_{on}. This can be described by the presence of the parasitic series resistance which counteracts the improvement on mobility for devices [24]. In Fig. 6b, the V_t roll-off characteristics of fabricated pMOSFETs as the shrinkage of gate length is displayed. For devices of all gate lengths filled with ALD W using SiH_4, apart from lower V_t value, they show a better short-channel effect (SCE) immunity than devices filled with ALD W using B_2H_6. The V_t roll-off for the former is less significant than that for the latter. For the former devices with larger strain, less variation of bandgap reduction and stress-induced conduction band offset as the shrinkage of gate length could account for the less significant V_t roll-off [25].

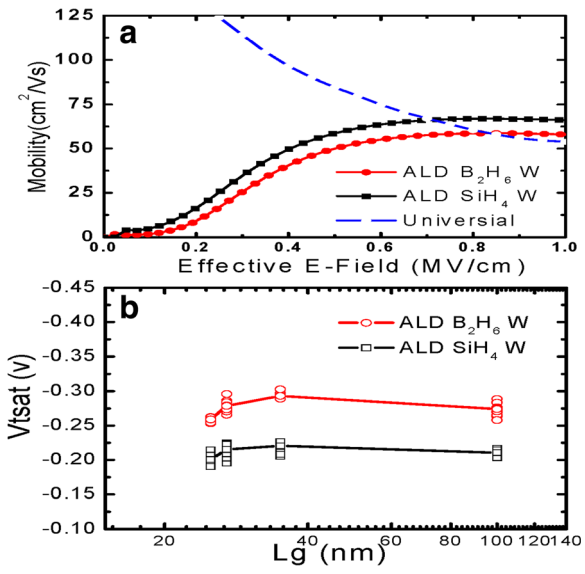

Fig. 6 **a** Extracted carrier mobility and **b** V_t roll-off characteristics ($V_d = -1$ V) for pMOSFETs filled with ALD W using SiH_4 and B_2H_6

Conclusions

In summary, we investigated pMOSFETs featuring ALD W filling metal using SiH_4 and B_2H_6 precursors. It was found that, compared to devices filled by ALD W using B_2H_6, devices filled by ALD W using SiH_4 show higher drive capability and better control of short-channel effects. The on-current, DIBL, and SS for the latter are 703 μA/μm ($V_{ds} = V_{gs} = -1.0$ V), 98 mV/V, and 88 mV/dec, respectively. The superior device performance for devices filled by ALD W using SiH_4 results from large compressive stress applied to the channel. Due to large stress as well as excellent trench filling capability of ALD W using SiH_4, this technique, therefore, can be adopted extensively in the 22-nm and beyond node CMOS technology in the future.

Abbreviations

ALD: Atomic layer deposition; DIBL: Drain-induced barrier lowering; DSL: Dual stress liners; EBL: Electron beam lithography; HKMG: High-*k* and metal gate; MGS: Metal gate stress technology; NBD: Nano-beam diffraction; pMOSFET: p-channel metal-oxide-semiconductor field-effect transistor; SCE: Short-channel effect; SMT: Stress memorization technology; STI: Shallow trench isolation; TEM: Transmission electron microscopy; TMAH: Tetramethylammonium hydroxide; XRD: X-ray diffraction

Acknowledgements

This work was financially supported by "National S&T Major Project 02" (project nos. 2009ZX02035-007 and 2011ZX02103-003), "National Key Research and Development Program of China" (2016YFA0301701), and the Youth Innovation Promotion Association of CAS under Grant No. 2016112 which are acknowledged.

Authors' Contributions

GW contributed to the experiment design and carried out the ALD W film growth and writing the article. CZ contributed to the film characterization and participated in the XRD analysis. JL, JBL, TY, and YX contributed to the transistor fabrication and process integration. JL and HY contributed to the analysis of device electric data. JY and HZ were involved in the discussions of this research. CZ, TY, and HR made the coordination of the project. All authors read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

Publisher's Note

Author details

[1]Key laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, People's Republic of China. [2]University of Chinese Academy of Sciences, Beijing 100049, People's Republic of China. [3]KTH Royal Institute of Technology, Brinellv. 8 10044, Stockholm, Sweden.

Received: 2 January 2017 Accepted: 12 April 2017
Published online: 26 April 2017

References

1. Nainani A, Gupta S, Moroz V, Choi M, Kim Y, Cho Y (2012) Is strain engineering scalable in FinFET era?: teaching the old dog some new tricks. In: International Electron Devices Meeting in 2012. IEDM'12, IEEE pp 18–3
2. Wang GH, Toh EH, Hoe KM, Tripathy S, Balakumar S, Lo GQ et al (2006) Strained silicon-germanium-on-insulator n-MOSFETs featuring lattice mismatched source/drain stressor and high-stress silicon nitride liner, in Electron Devices Meeting, 2006. IEDM'06. IEEE pp. 1–4
3. Radamson HH, Kolahdouz M (2015) Selective epitaxy growth of $Si_{1-x}Gex$ layers for MOSFETs and FinFET. J Mater Sci Mater Electron 26:4584–4603
4. Wang GL, Moeen M, Abedin A, Kolahdouz M, Luo J, Qin CL, Zhu HL, Yan J, Yin HZ, Li JF, Zhao C, Radamson HH (2013) Optimization of SiGe selective epitaxy for source/drain engineering in 22 nm node complementary metal-oxide semiconductor (CMOS). J Appl Phys 114:123511
5. Wang GL, Abedin A, Moeen M, Kolahdouz M, Luo J, Guo YL, Chen T, Yin HX, Zhu HL, Li JF, Zhao C, Radamson HH (2015) Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology. Solid State Electron 103:222–228
6. Hållstedt J, Kolahdouz M, Ghandi R, Radamson HH, Wise R (2008) Pattern dependency in selective epitaxy of B-doped SiGe layers for advanced metal oxide semiconductor field effect transistors[J]. J Appl Phys 103(5):054907
7. Ota K, Sugihara K, Sayama H, Uchida T, Oda H, Eimori T et al (2002) Novel locally strained channel technique for high performance 55nm CMOS. In: International Electron Devices Meeting in 2002. IEDM'02, IEEE pp 27–30
8. Yang H, Malik R, Narasimha S, Li Y, Divakaruni R, Agnello P et al (2004) Dual stress liner for high performance sub-45nm gate length SOI CMOS manufacturing. In: International Electron Devices Meeting in 2004. IEDM'04, IEEE pp 1075–1077
9. Kang C, Choi R, Song S, Choi K, Ju B, Hussain M et al (2006) A novel electrode-induced strain engineering for high performance SOI FinFET utilizing Si (1hannel for Both N and PMOSFETs. In: International Electron Devices Meeting, 2006. IEDM'06, IEEE pp 1–4
10. Auth C, Cappellani A, Chun J-S, Dalis A, Davis A, Ghani T et al (2008) 45nm high-k+ metal gate strain-enhanced transistors. In: VLSI Technology 2008 Symposium., pp 128–129
11. Auth C, Allen C, Blattner A, Bergstrom D, Brazier M, Bost M et al (2012) A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. In: VLSI Technology (VLSIT) 2012 Symposium., pp 131–132
12. Klaus J, Ferro S, George S (2000) Atomic layer deposition of tungsten using sequential surface chemistry with a sacrificial stripping reaction. Thin Solid Films 360:145–153
13. Kim S-H, Kwak N, Kim J, Sohn H (2006) A comparative study of the atomic-layer-deposited tungsten thin films as nucleation layers for W-plug deposition. J Electrochem Soc 153:G887–G893
14. Wang G, Xu Q, Yang T, Xiang J, Xu J, Gao J et al (2014) Application of atomic layer deposition tungsten (ALD W) as gate filling metal for 22 nm and beyond nodes CMOS technology. ECS J Solid State Sci Technol 3:P82–P85
15. Yang T, Wang G, Xu Q, Lu Y, Yu J, Cui H et al (2013) ALD W CMP for HKMG. ECS Trans 58:49–52
16. Xu Q, Luo J, Wang G, Yang T, Li J, Ye T et al (2015) Application of ALD W films as gate filling metal in 22 nm HKMG-last integration: evaluation and improvement of the adhesion in CMP process [J]. Microelectron Eng 137:43–46
17. Radamson HH, Hallstedt J (2005) Application of high-resolution X-ray diffraction for detecting defects in SiGe(C) materials. J Phys Condens Matter 17:S2315
18. Hansson GV, Radamsson H, Ni W-X (1995) Strain and relaxation in Si-MBE structures studied by reciprocal space mapping using high resolution X-ray diffraction[J]. J Mater Sci Mater Electron 6(5):292–297
19. Matsuki T, Mise N, Inumiya S, Eimori T, Nara Y (2007) Impact of gate metal-induced stress on performance modulation in gate-last metal–oxide–semiconductor field-effect transistors. Jpn J Appl Phys 46:3181
20. Bhushan B, Li X (1997) Micromechanical and tribological characterization of doped single-crystal silicon and polysilicon films for microelectromechanical systems devices [J]. J Mater Res 12(01):54–63
21. Lim J-S, Thompson SE, Fossum JG (2004) Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. Electron Device Letters IEEE 25:731–733
22. Thompson S, Sun G, Wu K, Lim J, Nishida T (2004) Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs. In: Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International, IEEE pp 221–224
23. Loo R, Sorada H, Inoue A, Lee B, Hyun S, Jakschik S et al (2007) Selective epitaxial Si/SiGe growth for VT shift adjustment in high k pMOS devices. Semiconductor Science and Technology 22:S110
24. Ng KK, Lynch W (1987) The impact of intrinsic series resistance on MOSFET scaling. Electron Devices IEEE Transactions 34:503–511
25. Claeys C, Simoen E, Put S, Giusi G, Crupi F (2008) Impact strain engineering on gate stack quality and reliability. Solid State Electron 52:1115–1126