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Novel design of combinational and sequential logical structures in quantum dot cellular automata

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Abstract

Quantum dot cellular automata (QCA) is a emerging nanotechnology that promises smaller size and lower power consumption, with faster speed compared to the transistor-based technology. In this paper, we have proposed novel 8-into-3 bit simple encoder, 4-into-2 bit priority encoder, scan flip-flop, and pseudo-random bit sequence generator designs in QCA. These circuits are useful components for the design of many logical and functional circuits. Simulation results of the proposed QCA circuits are obtained by using the QCA designer tool. The correctness of the proposed circuits is hence confirmed.

Keywords: Quantum dot cellular automata, Priority encoder, Simple encoder, Scan flip-flop, Pseudo-random bit sequence generator

Background

Complementary metal-oxide-semiconductor (CMOS) technology is in rampant use in current-day semiconductor fabrication. But there is a paradox in CMOS that power consumed increases with increase in speed. But some applications require more speed and less power. New technologies like carbon nanofield effect transistor and quantum dot cellular automata (QCA) have the capability to provide more integration and speed along with less power consumption and high parallel processing [1,2]. An encoder is a digital circuit that has two n input lines and n output lines. Corresponding to the input value, binary codes are generated by output lines [3]. A priority encoder is an encoder circuit named so because it carries out the priority function, i.e., in case more than one inputs are equal to 1 and at the same time, precedence will be given to the input having the highest priority. Scan flip-flop contains a multiplexer (MUX) to select either a normal operation with data input or scan operation with scan input [4]. It has a control input to select

either data or scan input. It is bigger than normal flip-flop (as MUX is included here). It adds nearly 20% to 30% of area per flip-flop. This paper deals with the QCA implementation of some of these combinational and sequential circuits.

QCA basics

QCA cells

The principle of quantum dot cellular automata was first proposed by Prof. CS Lent [1]. In order to implement a system that encodes information in the form of electron position, it becomes necessary to construct a vessel in which an electron can be trapped and 'counted' as present or absent.

As shown in Figure 1, a quantum dot does just this by establishing a region of low potential surrounded by a ring of high potential. In ordinary form, this technology is based on bi-stable QCA cell's interaction. The cell is constructed from four quantum dots and charged with two free electrons, which are able to tunnel between adjacent dots [5]. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Figure 1. These two arrangements are denoted as cell polarization. By using cell polarization to

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Figure 1 QCA cells.
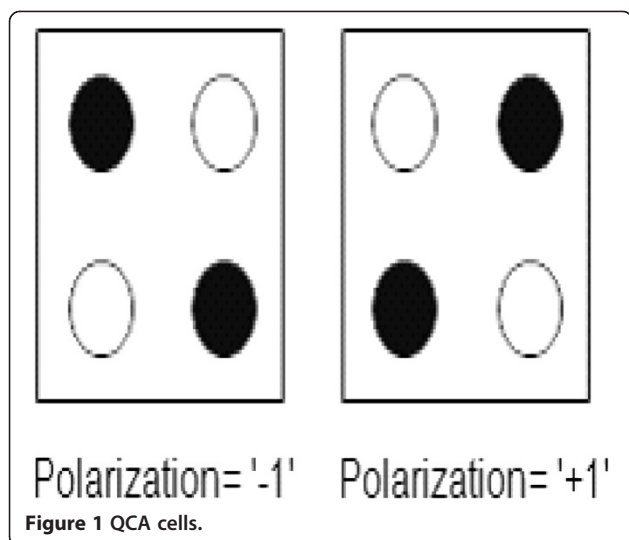
represent logic '1' and to represent logic '0', binary information is encoded in the charge configuration of the QCA cell.

QCA wires

Other important component in QCA designing is the wire. In a QCA wire, the propagation of binary signal takes place from input to output due to the electrostatic interactions between cells. Since the polarization of each cell tends to align with that of its neighbors, a linear arrangement of standard cells is used to transmit binary information from one point to another [6,7]. In this wire, all free cells align in the same direction as the driving cell (input cell), so the information contained in the state of the input is transmitted down the wire. Besides, the separation between dots and cells is a key parameter giving Coulombic effect in QCA application in conventional form.

A QCA wire is shown in Figure 2. Moreover, in a QCA wire, all of the computational power is provided by the Coulomb interaction between cells in absence of electrical current flow between cells and hence no power dissipation. Similar to the binary wire, there is another type of wire that is used to transfer data from one place to another. This is called inversion chain. In an inversion

chain all the QCA cells are 45° rotated from the normal QCA cells. Each cell of the chain inverts the signal due to Coulombic forces between the electrons. Hence, depending on the number of cells between input and output, the output can be same or the inverted value of the input [8]. For wire crossover, it uses a total of three layers for designing crossovers as shown in Figure 3. The multilayer crossover appears conceptually simple but there are questions about its realization, since it requires two overlapping active layers.

QCA clock zones

QCA circuits require a clock to function properly. QCA clocks change the tunneling barrier between quantum dot so as to facilitate the movement of electrons within a cell and allow them to change their configuration in a predefined manner [9]. There are two types of switching of tunneling barrier possible, which are adiabatic and abrupt. In adiabatic switching the tunneling barriers among the dots are raised slowly to bring the cell in a fixed polarization. Similarly, the barriers are lowered slowly to make electrons free to move among the quantum dots. Adiabatic switching is preferred over abrupt switching because it ensures that at every point of time during the operation, the circuit will remain in a ground (stable) state and will not move to an excited state permanently [10,11]. In this work we have used adiabatic switching in clocks. There are four QCA clocks, namely, clock 0, clock 1, clock 2, and clock 3 as shown in Figure 4. Each clock has four parts which are high level, falling edge, low level, and rising edge.

These phases are named *hold*, *release*, *relax*, and *switch*, respectively. Figure 4 shows the four phases of clock. The main function of QCA clocks is to ensure the proper transfer of the data from one place to another in a circuit [12]. During the *hold* state the tunneling barrier of the quantum dots is high; hence, electrons are highly localized and have a fixed polarization. During the release state, the tunneling barrier is decreased and electrons slowly become free to move. In the relax state electrons are completely free to tunnel among quantum dots and do not have any influence on the neighboring cells. In the switch state the tunneling

Figure 2 QCA wire.

Figure 3 Multilayer crossover.
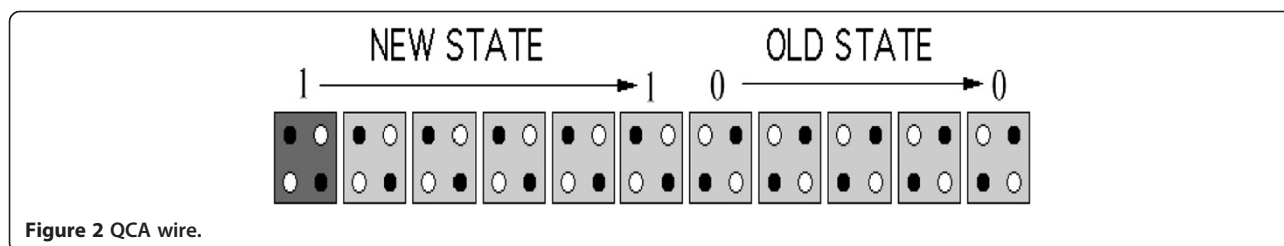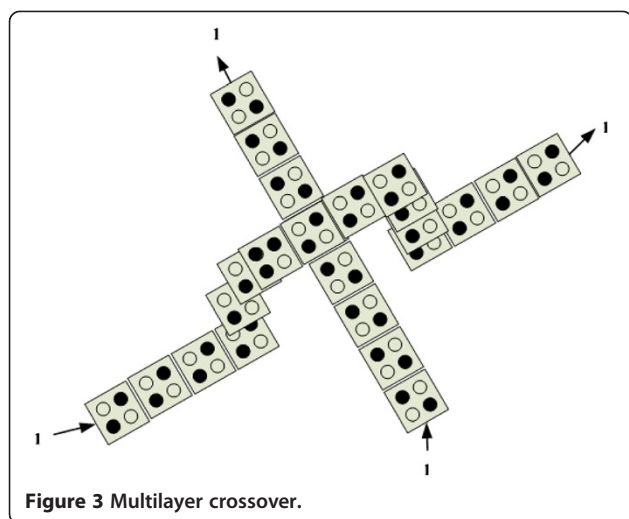
barrier is slowly raised constraining the electrons to the most stable state [13,14].

Majority gate and inverters

Any QCA circuit can be efficiently built using only majority gates and inverters. Figure 5 shows a majority gate with three inputs, i.e., A, B, and C, and output M (A, B, and C). A majority gate performs following function: Maj (A, B, C) = AB + BC + CA. AND and OR gates can be constructed using the majority gate easily by assigning one of the inputs to the majority gate as 0 and 1, respectively [15]. Figure 6 shows the QCA layout of inverter.

Proposed designs
The 8-3bit simple encoder

Figure 7 shows the QCA design of 8:3 bit simple encoder where D0 to D7 are inputs and Y0, Y1, and Y2 are


Figure 5 Majority gate.
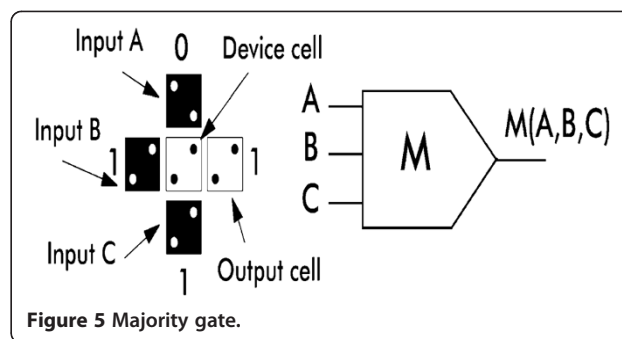
outputs, respectively. Figure 8 shows the simulation result of proposed circuit.

The 4–2 bit priority encoder

Priority encoders are used in a number of computer systems as well as other applications. For example, when several processes, modules, or units request a single hardware (or software) resource, a decision has to be made to allow a single request to use such a resource. The priority encoder implements a fixed selection function where the resource is granted to the request with the highest priority. The basic function of a 4-bit *priority encoder* is to convert the 4-bit input into a binary representation. If the input *n* is high, all lower inputs ($n - 1 \ldots 0$) are ignored. In Figure 9, D1, D2, D3, and D4 are four inputs respectively, and Y1, Y2, and V are outputs. Figure 10 shows the simulation result of the proposed circuit.

Scan flip-flop

Flip-flops and latches are fundamental building blocks of sequential digital circuits. Due to significant inter- and intra-die process variations, it is necessary to

Figure 4 Clocking scheme.

Figure 6 QCA inverter.
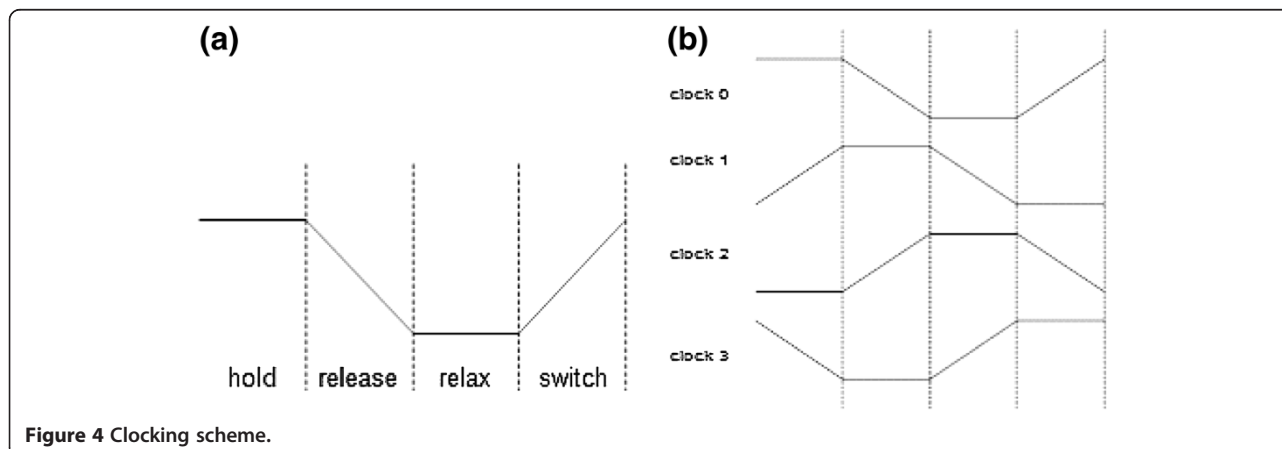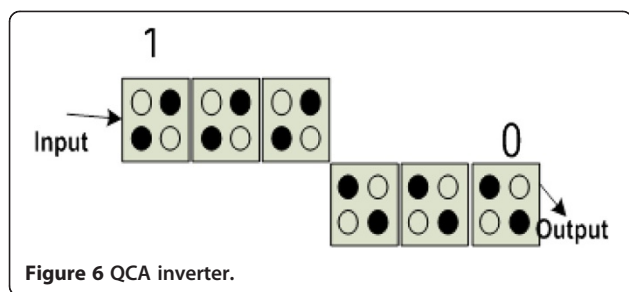
ensure correct logical and temporal functionality, so we need to carry out both functional as well as timing checks on the fabricated design [16]. Figure 11 shows the block diagram of a scan flip-flop, along with the D

flip-flop it replaces. It consists of a multiplexer and a D flip-flop. A and B are the inputs of the multiplexer and S acts as a select signal. The S signal is low during normal operation of the scan flip-flop. In scan mode SE is high. Now the D input of the flip-flop is driven by the scan-in signal B. They are very similar to the flip-flops with an additional enable pin, enabling them to function both as an ordinary (operating mode) flip-flop as well as the scan flip-flop(testing mode). They are used during testing and are much preferred over built-in self-test units. Figure 12 shows the QCA layout of scan flip-flop where A and B are input to MUX and S is select pin. The output of MUX is input to D flip-flop and Q is the output. Figure 13 shows the simulation result of proposed design.
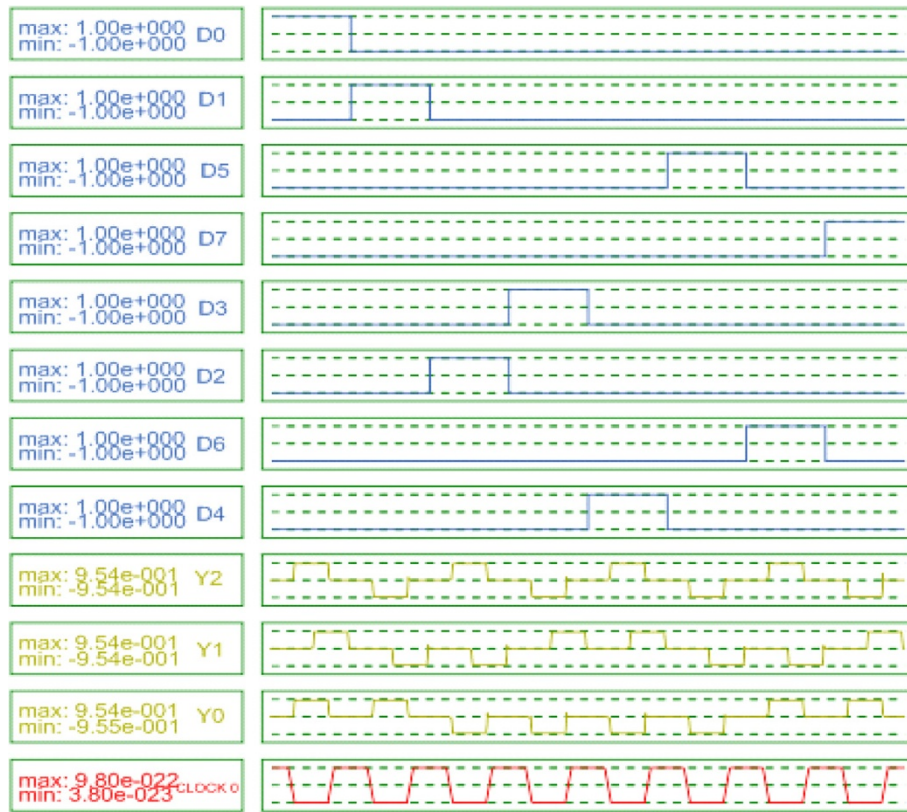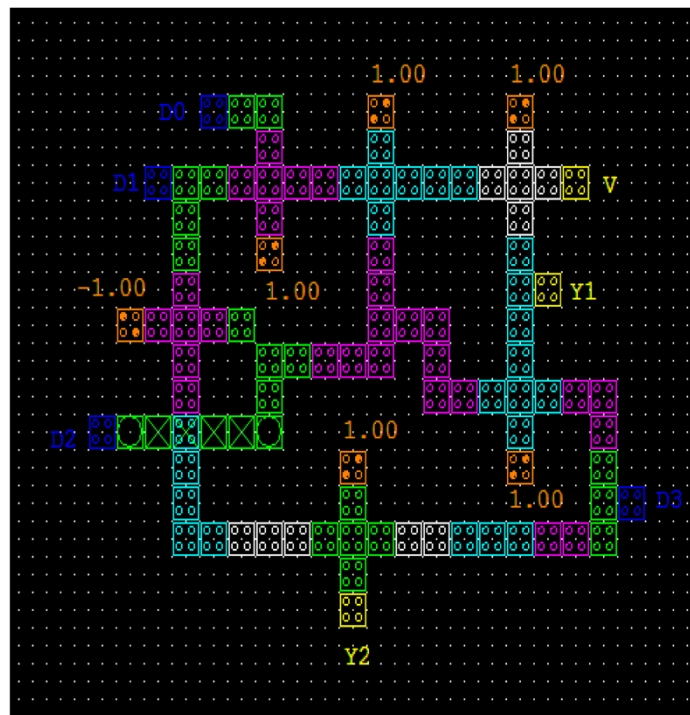

Figure 7 QCA layout of 8–3 bit simple encoder.
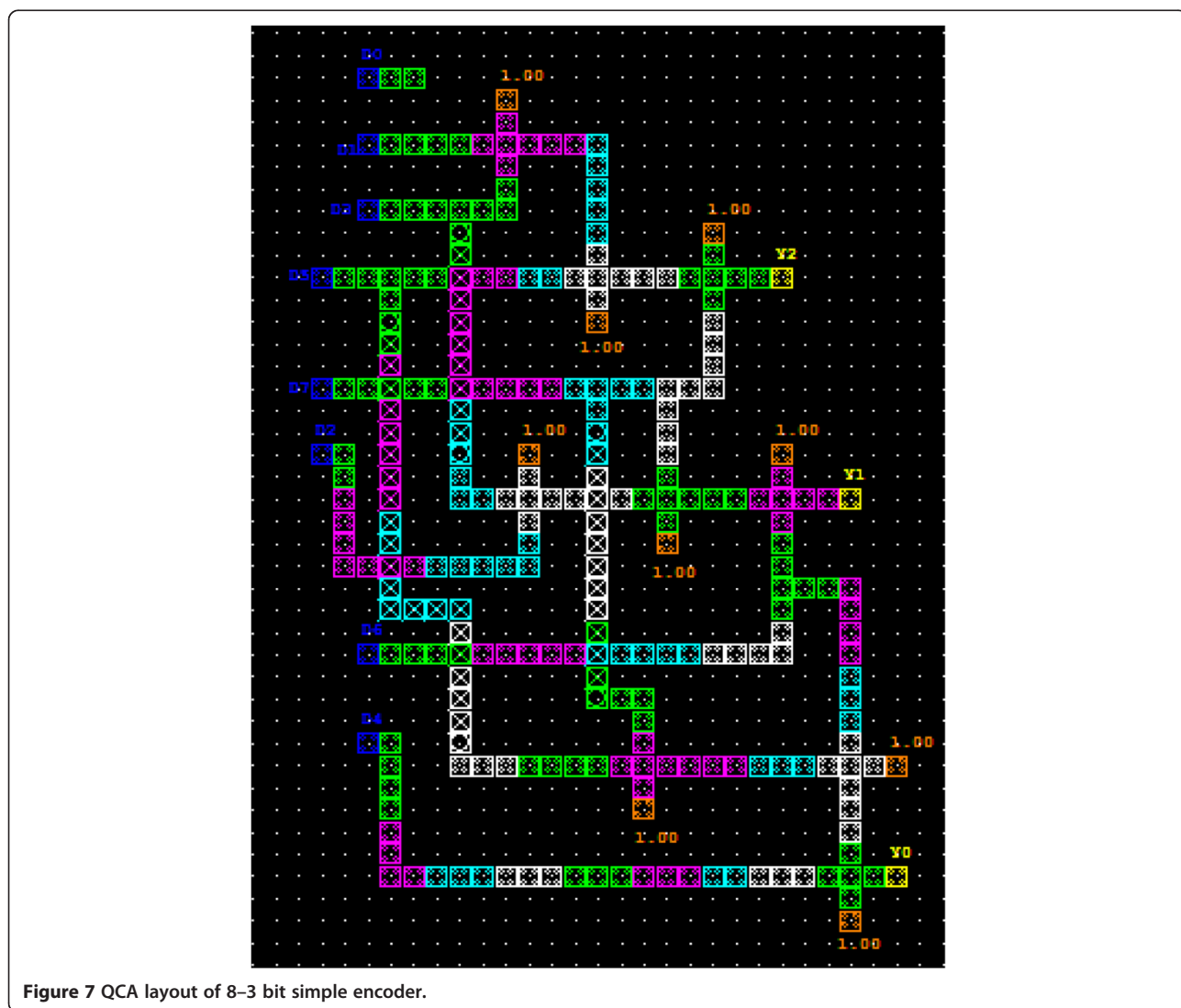
Figure 8 Simulation result of 8-3bit simple encoder.

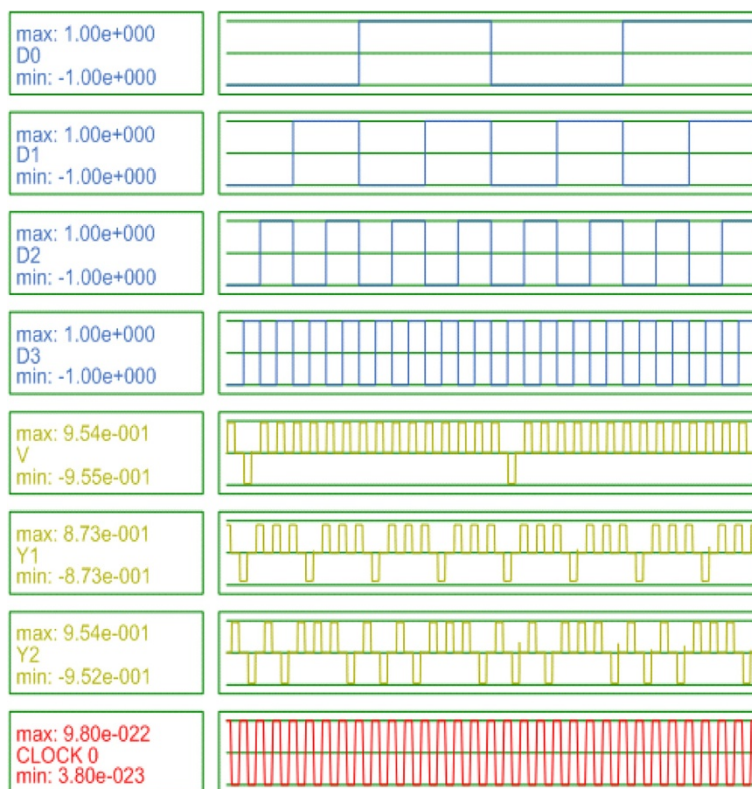**Figure 9 QCA layout of 4–2 bit priority encoder.**

Figure 10 Simulation result of 4–2 bit priority encoder.

The 3-bit PRBS generator

An N-bit pseudo-random binary sequence (PRBS) is a binary sequence and random in a sense that the value of any element is independent of all other elements' values, similar to real random sequences, and pseudo because it starts to repeat itself after every N elements. PRBS can be used for supplying known binary sequences which are used as test signals for making bit error measurement.
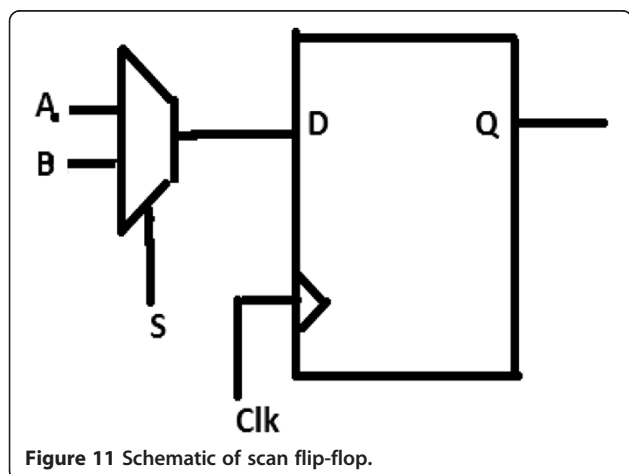

Figure 11 Schematic of scan flip-flop.

Figure 14 shows the QCA design of proposed PRBS generator.

Results and discussion

Circuits use lesser number of cells compared to traditional circuits and are more densely packed. These circuit designs have been simulated using QCA designer and the results are shown. Ninety QCA cells are used to design a scan flip-flop with area of 0.19 μm^2 whereas the 4–2 bit priority encoder, which contains 100 cells, has an area of 0.13 μm^2. Some of the larger and complex circuits such as 8–3 bit encoder have 281 cells with total area of 0.06 μm^2, and PRBS generator has 381 cells and area 0.61 μm^2. These and some more basic circuit designs can be clubbed together to create more complex circuit designs such as arithmetic logic unit or ALU, field programmable gate array or FPGA. In extension to this work, a fault-tolerant majority gate can be used and hence making the circuit more suitable for physical implementation.

Conclusions

This paper has demonstrated the design of a QCA 4:2 bit priority encoder and 8:3 bit simple encoder, scan flip-
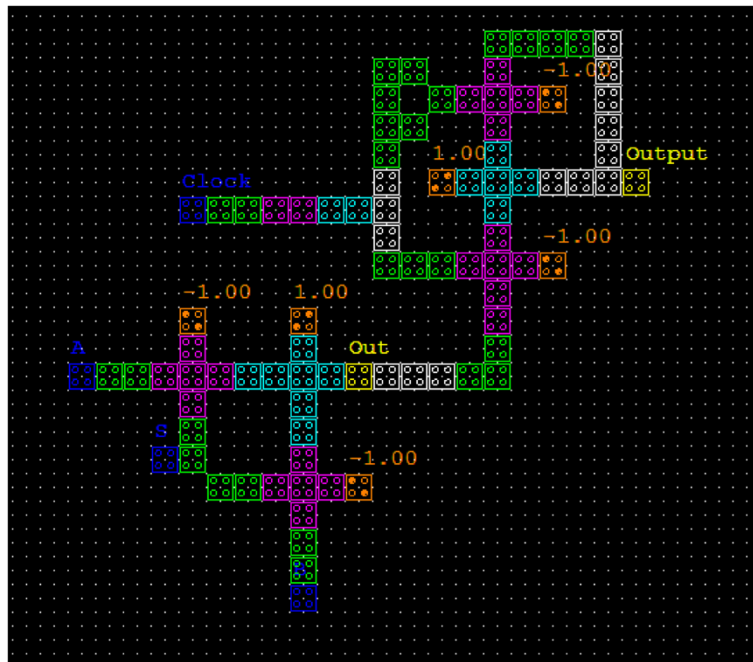
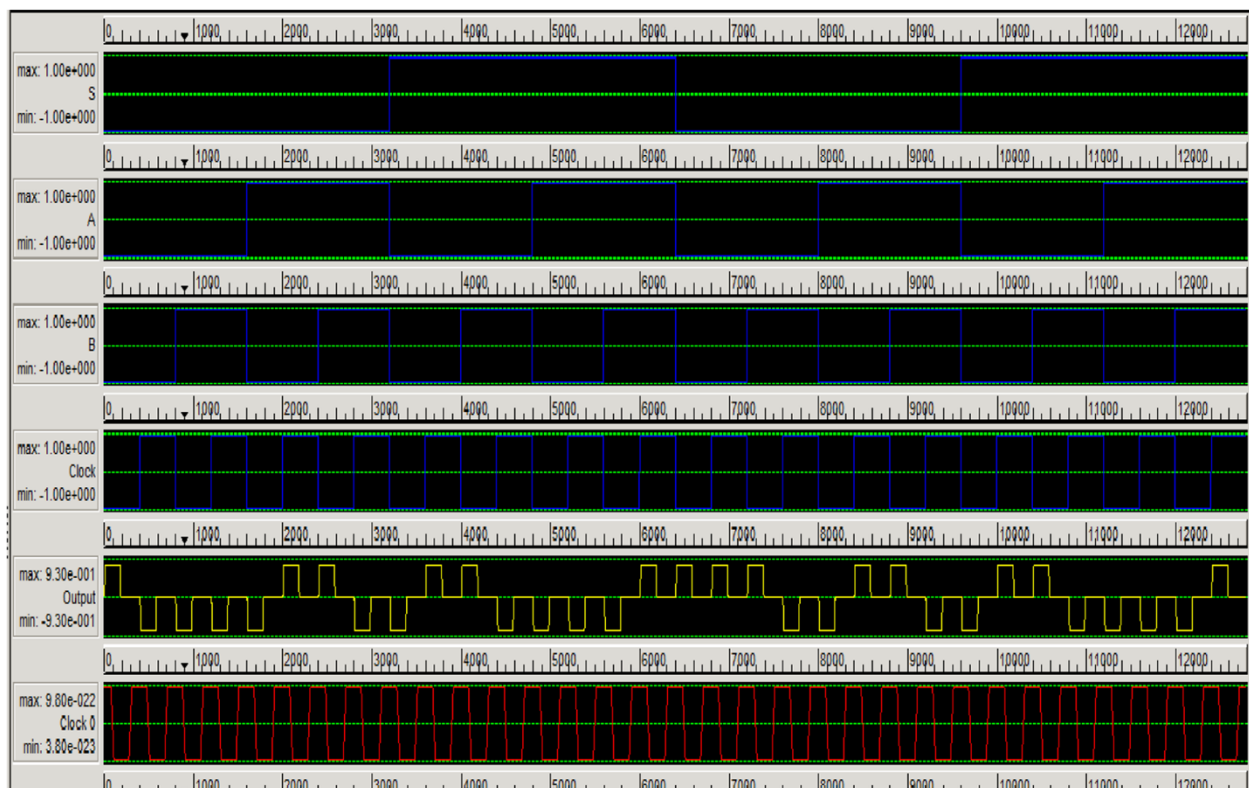**Figure 12 QCA layout of scan flip-flop.**

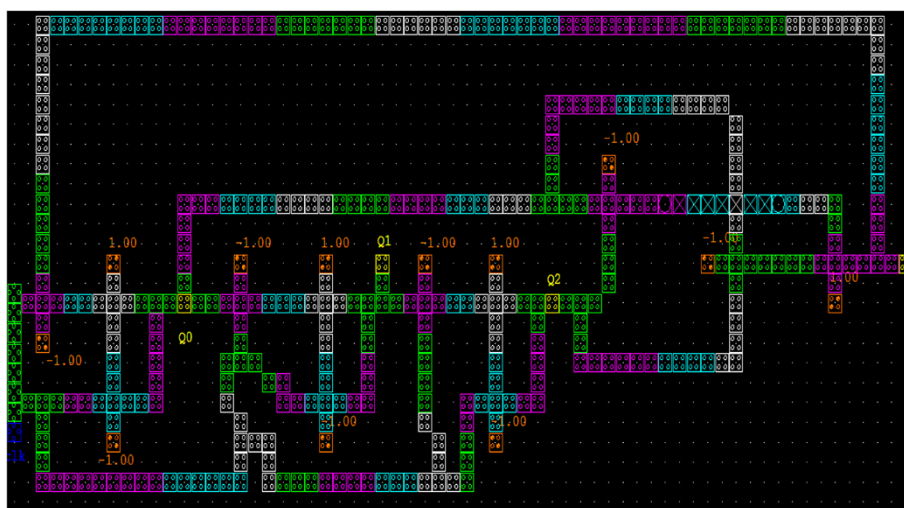**Figure 13 Simulation result of scan flip-flop.**

Figure 14 QCA layout of 3 bit PRBS.

flop, and PRBS. The proposed designs are significantly smaller than the same circuits using CMOS technology. The sizes of layouts are measured on the basis of size of QCA cells. All designs are carefully clocked and were functionally verified using QCA designer. Finally, in Table 1, designs are compared according to number of cells, area, and delay.

Methods

First of all, the logic behind any proposed circuit is deduced and then the circuit diagram is drawn at gate level. The gate level circuit is converted to QCA layout using majority gates, inverters, etc. as described in the above sections and then these designs are simulated in QCA designer which is the product of an ongoing research effort by the Walus Group at the University of British Columbia to create a design and simulation tool for QCA. The designer tool allows the designer to layout a QCA design and simulates it quickly. QCA designer has provided a new platform for developers; results from simulations, using this tool, have been published by many international groups [11-16]. Results obtained by this tool are then compared to theoretical values to verify the correctness of the circuit.

Table 1 Comparison of proposed designs

Design	Number of cells	Area (in µm^2)	Delay
8-3 bit simple encoder	281	$0.22 \times 0.30 = 0.06$	2.25
4-2 bit priority encoder	100	$0.32 \times 0.42 = 0.13$	1.25
Scan flip-flop	90	$0.46 \times 0.41 = 0.19$	2
PRBS generator	381	$1.28 \times 0.478 = 0.61$	4.5

Authors' contributions
SK designed the logic of proposed circuits and SG simulated them on QCA designer, and both of them drafted the manuscript. BG verified the simulation result. AKS helped in literature study and in modifying the manuscript. All authors read and approved the final manuscript.

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BG is a professor in the Department of EE, IIT Kanpur. His interest lies in spintronics and semiconductor device modeling. SG and SK are third year undergraduate students in the Department of EE, IIT Kanpur. AS is pursuing his Ph.D. degree under Prof. BG at the Department of EE, IIT Kanpur. His research interests include spintronics and device modeling.

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