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High-accuracy function synthesizer circuit with applications in signal processing

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Abstract

An original low-voltage current-mode high-accuracy function synthesizer circuit will be presented, allowing to implement a multitude of continuous mathematical functions. The dynamic range is strongly extended as a result of the superior-order approximation of the implemented functions. The current-mode operation and the independence of the circuit performances on technological parameters are responsible for an additional improvement of structure accuracy. The advantages of reduced design costs per function represent an immediate consequence of the multiple functions realized by the proposed structure. The approximation error of the original function synthesizer circuit is 0.3% for an extended range of the input signal. The function synthesizer is designed for implementing in 0.18 μm CMOS technology and it is supplied at 1 V. An original application of the proposed function synthesizer circuit is represented by a new fourth-order approximation exponential function generator, having a dynamic range of approximately 33 dB, for an error smaller than 1 dB.

Keywords: Signal synthesizing, Approximation error, Exponential function generator, Current-mode operation, Continuous mathematical function, CMOS analog designs

Introduction

Analog signal processing represents an important area of analog integrated circuits analysis and design, with a multitude of applications in many domains. Multiplier and exponential circuits are useful in telecommunication circuits [1-4], medical equipments [5,6], hearing devices [7,8], or disk drives [9,10]. Squaring circuits represent the core for implementing any continuous function, using the limited Taylor series expansion. The Euclidean distance function is very important in instrumentation circuits [11,12], communication [1,2], neural networks [13,14], display systems [15,16], or classification algorithms [17], being also useful for vector quantization or nearest neighbor classification [18,19].

The main problem in designing analog signal processing structures is how to implement with minimal effort a large number of nonlinear mathematical functions [3]. The requirements for an analog signal processing structure are mainly related to the circuit accuracy, to the possibility of achieving a multitude of circuit functions with reasonable design costs and to the controllability of the implemented function. In this context, analog processing performed in focal-plane Vision Systems-on-Chip [20] can represent an interesting choice. Important functions from the perspective of their applications are multiplying/dividing [21-30], exponential [31-34], squaring/square-rooting [30,35-41], or Euclidean distance [42,43] functions.

In bipolar technology, the multiplying/dividing function can easily be obtained from the logarithmical characteristic of the bipolar transistor. Important errors still remain because of the nonzero values of the base currents and of the temperature dependence of the bipolar transistor parameters (the thermal voltage is linearly increasing with temperature and the saturation current has an exponential dependence on temperature). In order to achieve a low-power operation of complementary metal oxide semiconductor (CMOS) designs, the subthreshold biasing of metal oxide semiconductor (MOS) transistors is an interesting choice. Based on the logarithmical law of a MOS transistor in weak inversion, the implementation of a CMOS Multiplier/Divider circuit becomes very simple (even with respect to the bipolar version). In consequence, the result will be smaller silicon area consumption, the circuit being also compatible with low-power very large-scale integration (VLSI) designs. For obtaining an important increasing

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of the circuit frequency response, the multiplying/dividing function can be achieved by employing the square law model of MOS transistors biased in saturation.

The exponential function is available in bipolar technology using the exponential characteristic of the bipolar transistor. In CMOS technology, the exponential law can directly be implemented exploiting the weak inversion operation of the MOS transistor. In order to obtain the exponential function using the squaring characteristic of the MOS transistor in saturation (for improving the circuit frequency response), the classical method is to approximate the exponential function with its *n*th-order expansion (the polynomial series). The approximation error will be proportional with the number of terms neglected in the expansion.

There are many possibilities of implementing squaring and square-rooting functions using the quadratic characteristic of the MOS transistor biased in saturation. The main goals of this class of circuits are the silicon-occupied area, the independence of the output current on the technological parameters and on temperature and the small sensitivity to the multitude of second-order effects.

The classical approach in analog signal processing circuits is to implement, for each circuit function, a class of computational structures. The proposed method for obtaining a multitude of continuous mathematical functions is to design a complex computational structure, named function synthesizer circuit that is able to generate these functions approximating them using an original superior-order approximation function. The accuracy of computation is correlated with the order of approximation. In conclusion, a tradeoff between the complexity of the structure and its intrinsic accuracy must be made. The advantages of the proposed method are mainly related to the possibility of strongly reduce the power consumption and circuit complexity per implemented function.

It exists in literature a relatively small number of function synthesizer circuits implemented in CMOS technology [4,33,44-46], these applications being dedicated to the realization of a limited number of mathematical functions. In [44], the approximation of the implemented function can be obtained by adding the weighted output currents of a number of basic building blocks, built around a basic current squarer, and a constant current, the circuit presenting the disadvantage of a relatively large complexity. The circuit proposed in [45] is based on approximating the required function using the first three terms of its Taylor series expansion. The approximations can be implemented by adding the output currents of a weighted current square, a weighted current amplifier (or attenuator), and a constant current. The errors are mainly caused by the small value (two) of the approximation order and, in consequence, they are relatively large. Additionally, from the same reason, the range of the input signal is strongly restricted. A structure for synthesis of analog exponential functions, based on approximating the exponential function using rational functions, is proposed in [46]. The circuit presents the important limitations of realizing only the exponential function and of an implementation in bipolar technology.

The article is multidisciplinary, starting from a rigorous mathematical analysis and continuing with original implementations of the proposed electronic computational circuits. A new implementation of a current-mode function synthesizer circuit with an extended capability of generating continuous mathematical functions will be presented. The proposed structure is based on a fourth-order original approximation function, having the important advantages of an improved accuracy and of reconfiguration capability.

Main text

Fundamental methodology

In order to implement an improved accuracy analog function synthesizer circuit, the proposed method is to use a general continuous approximation function, $g(x)$, having a Taylor series that can be made to fourth-order match a multitude of continuous mathematical functions, $f(x)$.

$$g(x) = \frac{1 + a_O x}{1 + a_1 x} + \frac{a_2 x}{1 + x} + a_3 x + a_4 \tag{1}$$

$a_O \ldots a_4$ represent constant coefficients, having values imposed by the necessity that the Taylor series of $g(x)$ function to be identical (in a fourth-order approximation) with the Taylor series of $f(x)$ function, that can be expressed by the following polynomial relation:

$$f(x) = m + nx + px^2 + qx^3 + rx^4 + sx^5 + tx^6 + \ldots \tag{2}$$

$m \div t$ represents constant coefficients of the expansion, depending on the expression of $f(x)$ function that must be implemented.

The motivation for choosing this particular $g(x)$ approximation function is correlated with the possibilities of its facile implementation in CMOS technology (the multiplying/dividing function has a relatively simple realization). In comparison with this original approximation function, the Pade approximation [24] (having also good accuracy) presents a much more complicated implementation in CMOS technology, requiring squaring and superior-order computational circuits that strongly increase the overall complexity of the function synthesizer. The requirements for an extremely accuracy of the function synthesizer circuit impose a relatively high order of approximation for $g(x)$ function. The increasing of the order of approximation strongly increases the complexity of the designed circuit,

being necessary to realize a tradeoff between the circuit complexity and its overall accuracy. From this point of view, an optimal choice that allows to obtain a very good accuracy and a relative large dynamic range of the function synthesizer using a reasonable circuit complexity is based on a fourth-order approximation.

The fourth-order identity between the Taylor series of $f(x)$ and $g(x)$ functions is equivalent with the identity between the first five terms from the Taylor series of the previous functions, being evident the reason of choosing five coefficients $a_O \ldots a_4$ for defining $g(x)$ function. It results

$$a_O = \frac{(p+q)^3}{(r+q)(r+p+2q)} - \frac{r+q}{p+q} \tag{3}$$

$$a_1 = -\frac{r+q}{p+q} \tag{4}$$

$$a_2 = \frac{(p+q)^2}{r+p+2q} - p \tag{5}$$

$$a_3 = n + p - \frac{(p+q)^2}{r+q} \tag{6}$$

$$a_4 = m - 1 \tag{7}$$

The approximation error will have the following general expression:

$$\epsilon_{f(x)}^{g(x)}(x) \cong \left[\frac{q^2 - 2rp - qr}{p+q} - s\right]\frac{x^5}{f(x)} \tag{8}$$

In order to further reduce the approximation error of the synthesizer circuit, it is possible to increase the order of approximation. For example, a possible fifth-order approximation function that requires a reasonable complexity of CMOS implementation can be generally expressed as follows:

$$g'(x) = \frac{b_O x}{1+b_1 x} + \frac{b_2 x}{1+x} + b_3 x^2 + b_4 x + b_5 \tag{9}$$

$b_O \ldots b_4$ represent constant coefficients, having values imposed by the necessity that the Taylor series of $g'(x)$ function to be identical (in a fifth-order approximation) with the Taylor series (2) of $f(x)$ function. The additional complexity of the circuit that implements $g'(x)$ function comparing with the computation structure required by $g'(x)$ is represented by a current-mode squaring circuit (for obtaining the $b_3 x^2$ term).

Current-mode implementation of the function synthesizer circuit

Block diagram of the function synthesizer with fourth-order approximation

The block diagram of the function synthesizer, based on the original proposed approximation function (1), is presented in Figure 1. The "Multiplier/Divider" circuits are current-mode structures [30,47,48], having the new implementation and the description of their operation presented in the following paragraph. The expressions of I_{OUTa} and I_{OUTb} currents are

$$I_{OUTa} = \frac{I_O I_{1a}}{I_{2a}} \tag{10}$$

and

$$I_{OUTb} = \frac{I_O I_{1b}}{I_{2b}} \tag{11}$$

The output current of the circuit having the block diagram presented in Figure 1 will have the following expression:

$$I_{OUT} = I_{OUTa} + I_{OUTb} + a_3 I_{IN} + a_4 I_O \tag{12}$$

Using the notation $x = I_{IN}/I_O$ and relation (1), it results that I_{OUT} current represents the fourth-order approximation of $f(x)$ function:

$$\begin{aligned} I_{OUT} &= I_O\left(\frac{1+a_O x}{1+a_1 x} + \frac{a_2 x}{1+x} + a_3 x + a_4\right) \\ &= I_O g_2(x) \cong I_O f(x) \end{aligned} \tag{13}$$

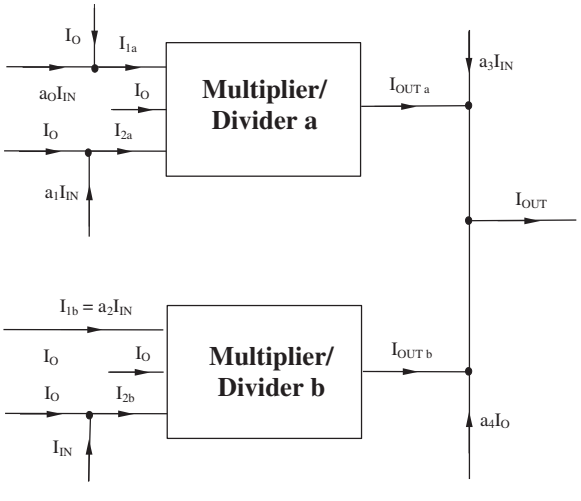

Figure 1 The block diagram of the function synthesizer with fourth-order approximation.

The implementation of the "X²" block

The functional core for designing the "Multiplier/Divider" circuit is represented by a current-mode squaring circuit, having the original implementation presented in Figure 2. The aspect ratios of MOS transistors are $1\mu/0.54\mu$ for M1–M4 transistors and $0.8\mu/0.54\mu$ for M5–M7 transistors.

Noting with $V_{GS}(I)$ the absolute value of the gate–source voltage of a MOS transistor biased at a drain current equal with I the equation of the translinear loop can be expressed as follows:

$$2V_{GS}(I_O) = V_{GS}(I_D) + V_{GS}(I_D + I_{IN}) \tag{14}$$

resulting

$$2\sqrt{I_O} = \sqrt{I_D} + \sqrt{I_D + I_{IN}} \tag{15}$$

Reducing the radicals by squaring the terms and simplifying, it results

$$4I_O - 2I_D - I_{IN} = 2\sqrt{I_D(I_D + I_{IN})} \tag{16}$$

equivalent with:

$$16I_O^2 + I_{IN}^2 - 16I_DI_O - 8I_OI_{IN} = 0 \tag{17}$$

So

$$I_D = I_O - \frac{I_{IN}}{2} + \frac{I_{IN}^2}{16I_O} \tag{18}$$

The expression of the output current will be

$$I_{OUT} = I_D + \frac{I_{IN}}{2} - I_O = \frac{I_{IN}^2}{16I_O} \tag{19}$$

The previous relations can be used only for strong saturated devices and for not too small devices. In order to increase the accuracy of the computations, quasi-identical source–drain voltages for M1–M2 and M3–M4 transistors, respectively, must be imposed. The source–drain voltage of M3 transistor can be expressed as follows

$$V_{SD3} = V - V_{GS1} \cong V - V_{GS2} = V_{SD4} \tag{20}$$

because, considering $I_{IN} << I_O$, M1 and M2 transistors are identical and biased at drain currents that differ only with a small amount. Additionally, for biasing M1 and M2 transistors at approximately equal drain–source voltages, V' potential must be imposed, from the I_{OUT} external terminal, to be equal with V potential. This particular biasing of M1 and M2 transistors will impose quasi-identical source–drain voltages also for M5 and M6 transistors, this fact increasing the accuracy of M5–M6 current mirror.

The M3–M7 transistors are not affected by the substrate effect, as their bulks are connected to their sources terminals. The M1 and M2 transistors have the bulk connected to the ground, so their non-zero bulk-source voltage will be responsible for small errors introduced by the substrate effect. As a result, the expression of I_{OUT} current will slightly be affected by undesired dependencies on technological parameters. The impact of these errors on the overall accuracy of the proposed function synthesizer circuit is small and they can be compensated using specific design techniques. The biasing current of the squaring circuit from Figure 2 is approximately $200\mu A$.

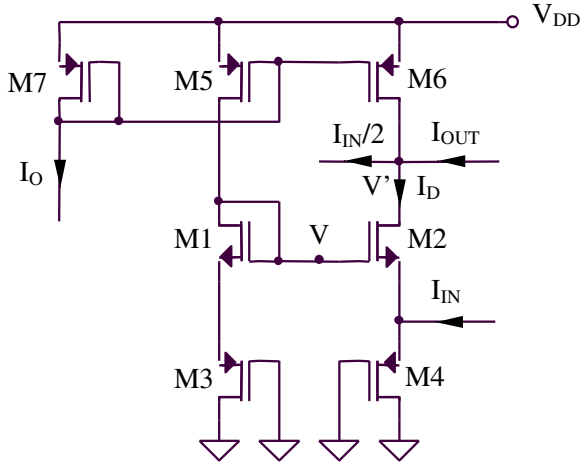

Figure 2 The implementation of the "X^2" block.

The implementation of the "multiplier/divider" block

The original proposed "Multiplier/Divider" circuit is presented in Figure 3a, being designed using two current-mode squaring circuits, similar with the structures presented in Figure 2 (M1–M4 and M3–M6, respectively). The full CMOS implementation of the "Multiplier/Divider" circuit is shown in Figure 3b. The complexity of the "Multiplier/Divider" circuit is minimized by re-using M3–M4 transistors for both squaring circuits. The aspect ratios of MOS transistors are $1\mu/0.54\mu$ for M1–M6 transistors and $0.8\mu/0.54\mu$ for M7–M8 transistors. The output current has the following expression:

$$I_{OUT} = I_{D1} - I_{D2} + 2I_O \tag{21}$$

where two translinear loops similar with the loop analyzed for the "X^2" circuit implement the following expressions of I_{D1} and I_{D2} currents (derived from (19)):

$$I_{D1} = I_2 - (I_1 + I_O) + \frac{(I_1 + I_O)^2}{4I_2} \tag{22}$$

and

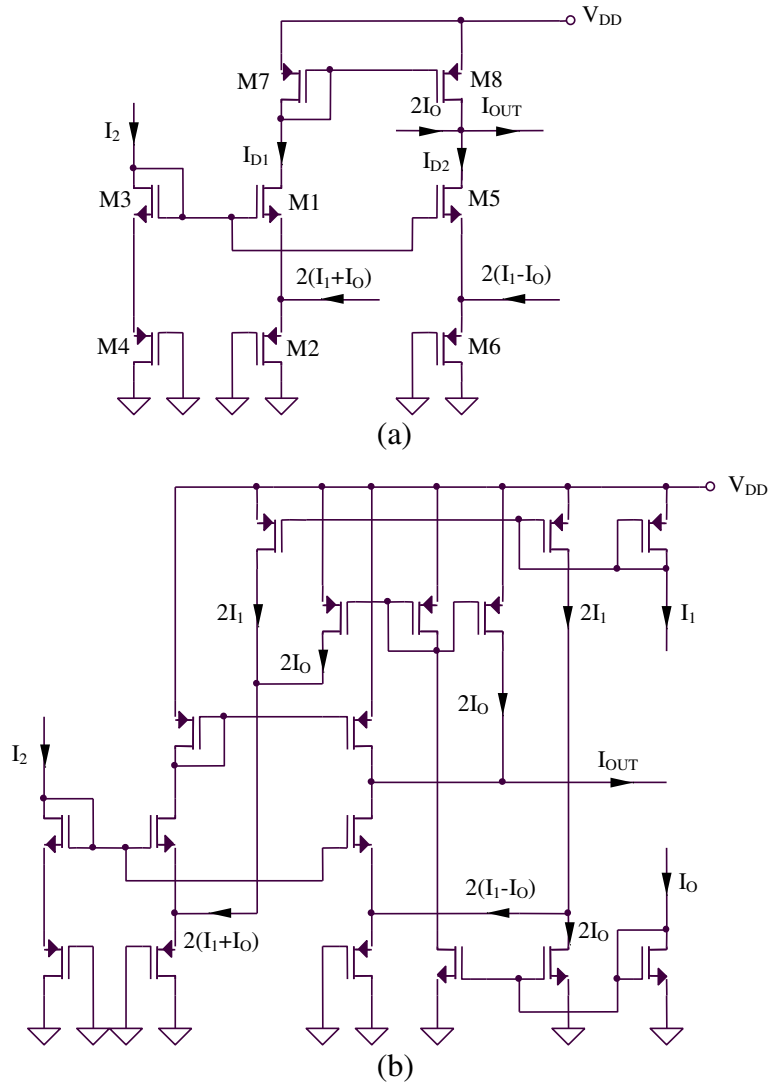

Figure 3 (a) The core of the Multiplier/Divider circuit. (b) The implementation of the Multiplier/Divider circuit.

$$I_{D2} = I_2 - (I_1 - I_O) + \frac{(I_1 - I_O)^2}{4I_2} \tag{23}$$

resulting an output current of the circuit having the following expression:

$$I_{OUT} = I_O \frac{I_1}{I_2} \tag{24}$$

The original proposed Multiplier/Divider circuit presents two important advantages. First, the current-mode operation increases the frequency response of the computational structure. Second, the independence of the output current expressed by (24) on technological parameters removes, in a first-order analysis, the temperature- and technological-caused errors, the overall accuracy of the proposed circuit being increased in this way. Additionally, the resulted concrete implementation of the function synthesizer circuit based on the block diagram proposed in Figure 4 has a smaller complexity comparing with previously reported similar computational structures.

Using MOS transistors implemented in $0.18\mu m$ CMOS technology, the maximal frequency of operation of the proposed function synthesizer circuit is approximately hundreds *kHz - MHz*, depending on the particular model of MOS active devices. The biasing current of the "Multiplier/Divider" circuit is approximately $300\mu A$, while the maximal biasing current of the function synthesizer circuit is smaller than $800\mu A$.

Error mechanisms for function synthesizer circuit

Real circuits are affected by a multitude of errors [3,4] that slightly affects their overall accuracy. The most

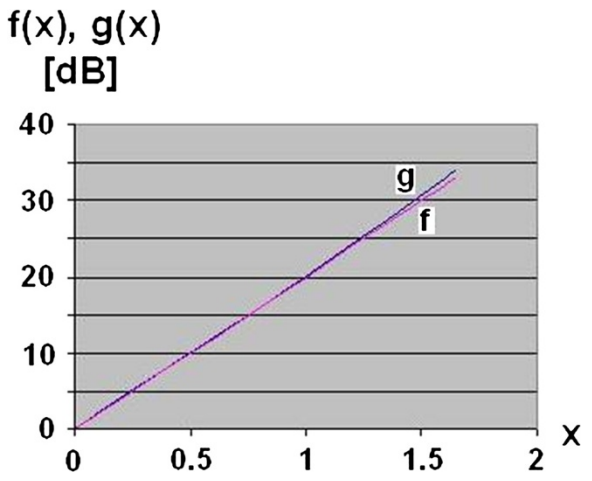

Figure 4 Graphical comparison between *g*(*x*) approximation function and *f*(*x*) = exp(*x*).

important errors that must be taken into account for evaluating the function synthesizer accuracy are presented in the following paragraphs.

The deviation of the MOS transistor characteristic from the square-law, bulk effect, leakage

The saturated MOS transistor squaring characteristic is affected by the second-order effects: mobility degradation (25), channel-length modulation (26), and bulk effect (27):

$$K = \frac{K_O}{[1 + \theta_G(V_{GS} - V_T)](1 + \theta_D V_{DS})} \tag{25}$$

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{26}$$

$$V_T = V_{TO} + \gamma\left(\sqrt{\Phi - V_{BS}} - \sqrt{\Phi}\right) \tag{27}$$

Table 1 Comparison between *g*(*x*) approximation function and *f*(*x*) = exp(*x*)

x	*g*(*x*) (dB)	*f*(*x*) (dB)	ϵ (dB)
0	0	0	0
0.2	4.075	4	0.075
0.4	8.029	8	0.029
0.6	12.011	12	0.011
0.8	16.028	16	0.028
1.0	20.095	20	0.095
1.2	24.239	24	0.239
1.4	28.495	28	0.495
1.6	32.914	32	0.914
1.65	34.001	33	1.001

The errors introduced by the bulk effect [3,4] can be reduced by proper designs that avoid the dependence of the circuit parameters on the threshold voltage. The design of circuits for obtaining a zero bulk-source voltage cancels out the errors introduced by the bulk effect. Additional errors produced by the second-order effects are given by the dependence of K transconductance parameter on V_{GS} voltage. Taking into account only the $K(V_{GS})$ dependence, a small changing of $K(V_{GS})$ voltage comparing with the analysis based on the first-order model of MOS transistors can be determined:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{K}} + \frac{\theta_G}{K} I_D \tag{28}$$

For latest CMOS VLSI nanometer designs, the leakage [3,4] becomes more important, the leakage current depending on the properties of the layout and also on the device structure. The determination of the total leakage cannot be made by adding individual leakage currents, because of a correlation that exists between leakage currents.

The subthreshold leakage is the current produced by minority electrons flowing through p substrate from source to drain, being modeled by an exponential function:

$$I_{SL} = I_{DO}\frac{W}{L}\exp\left(\frac{V_{GS} - V_T}{nV_{TH}}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{TH}}\right)\right] \tag{29}$$

W/L is the aspect ratio of the MOS transistor, V_{TH} is the thermal voltage, n is a parameter, and I_{DO} current is an additional parameter. The subthreshold-off current (obtained for $V_{GS} = 0$ and $V_{DS} >> V_T$) can be expressed as follows:

$$I_{SLoff} = I_{DO}\frac{W}{L}\exp\left(\frac{-V_T}{nV_{TH}}\right) \tag{30}$$

The gate leakage current can be carried by tunneling electrons or holes, the carriers leaking to source, drain, and channel. For junction leakage, low currents are carried by minority carriers drifting across the junction, by the electron–hole generation in junction or by the impact ionization at high reverse bias, the electrons being able to pass the barrier by tunneling through it—Band-To-Band Tunneling current [3,4].

Mismatches in current mirrors

Current mirrors implemented using real circuits present some errors caused by the mismatches between the

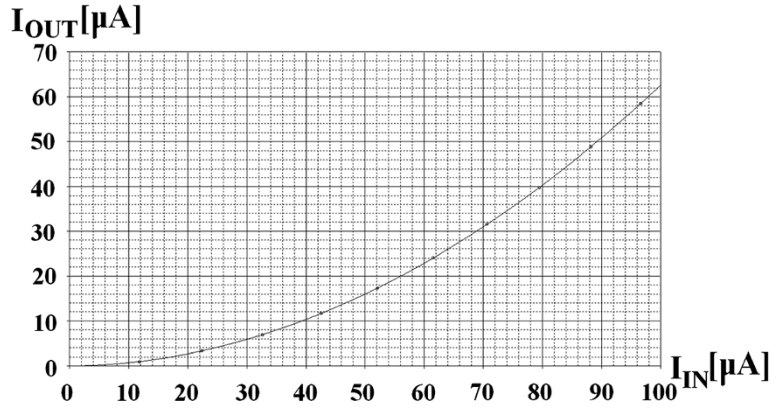

Figure 5 SPICE simulation $I_{OUT}(I_{IN})$ for the squaring circuit.

composing MOS transistors and also by the channel-length modulation:

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_O}{(W/L)_{REF}} \frac{1+\lambda V_{DSO}}{1+\lambda V_{DSREF}} \tag{31}$$

The method for reducing the errors introduced by the channel-length modulation is to impose to the current mirror an output voltage that set $V_{DSO} \cong V_{DSREF}$.

Different threshold voltages and K_n/K_p constants for NMOS/PMOS devices

Real circuits present differences between the threshold voltages and K_n/K_p constants for NMOS and PMOS transistors. In order to avoid additional inaccuracies introduced by the practical situation, translinear loops that represent the functional basis of many computational circuits must contain only NMOS or PMOS active devices or must be implemented using quasi-symmetrical structures from the point of view of this complementarily (the same number of NMOS and PMOS transistors).

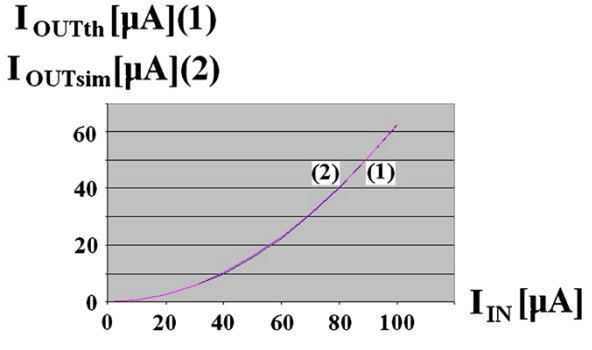

Figure 6 Comparison between the simulated and the theoretical estimated results for the current squarer.

Variations over the process, temperature, and supply voltage

Most of MOS transistors parameters are affected by the process in which the computational circuits are implemented. On the other side, technological parameters present important temperature dependencies. From this perspective, in order to avoid important errors introduced by process and temperature, the practical realizations of analog computational circuits must be done in such a way that minimizes the number of technological parameters in the expression of the output signal. Additionally, the errors caused by the supply voltage variations can be minimized using self-biased cascode configurations. In this context, a tradeoff between power supply rejection ratio and minimal supply voltage has to be considered.

Applications

An original exponential function generator circuit can be designed using the fourth-order approximation function (1), replacing in general relations (3)–(7) the particular values of constant coefficients of expansion (2): $m = 1$, $n = 1$, $p = 1/2$, $q = 1/6$ and $r = 1/24$. The $g(x)$ function that fourth-order approximates the exponential function can be expressed as follows:

$$g(x) = \frac{16+21x}{16-5x} + \frac{1}{126}\frac{1}{1+x} - \frac{7x}{11} \tag{32}$$

Using (8), the approximation error of the exponential function generator will have the following general expression:

$$\epsilon^{g(x)}_{\exp(x)}(x) \cong \frac{x^5}{120\exp(x)} \tag{33}$$

A comparison between $g(x)$ approximation function and $f(x) = \exp(x)$ is shown in Table 1.

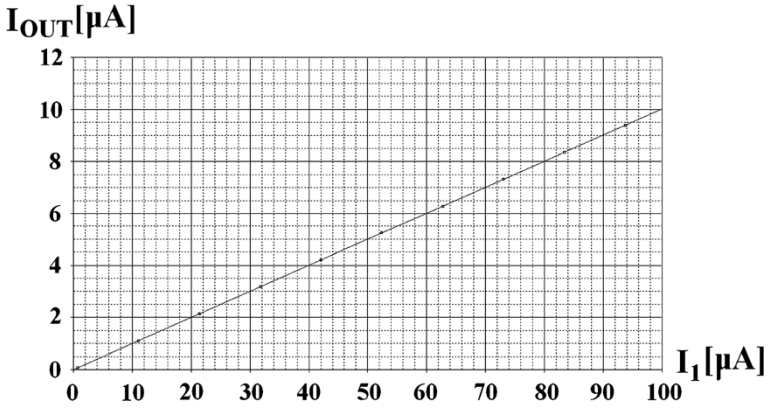

Figure 7 SPICE simulation $I_{OUT}(I_1)$ for the Multiplier/Divider circuit.

A graphical comparison between $g(x)$ approximation function and $f(x) = \exp(x)$ is presented in Figure 4.

As a result of using a fourth-order approximation function, the dynamic range of the proposed exponential function generator is approximately 33 dB, for an error smaller than 1 dB.

Simulations

The proposed function synthesizer circuit is designed for implementing in $0.18\mu m$ generic CMOS technology, the simulations being based on the square-law SPICE LEVEL 3 model. The parasitic and noise effects have been neglected in the performed analysis, but it could be estimated that their impact to the overall accuracy of the proposed function synthesizer circuit are relatively small comparing with other causes of errors (approximation error or second-order effects). The overall accuracy of the proposed fourth-order function synthesizer circuit is 0.3% for an extended range of the input signal.

SPICE simulation $I_{OUT}(I_2)$ for the Multiplier/Divider circuit proposed in Figure 3 is presented in Figure 5. The I_O and I_1 currents have the following values: $I_O = 50\mu A$ and $I_1 = 20\mu A$, while the range of I_2 current was chosen to be between $30\mu A$ and $100\mu A$.

A comparison between the simulated and the theoretical estimated results for the proposed current squarer is shown in Figure 6.

SPICE simulation $I_{OUT}(I_1)$ for the Multiplier/Divider circuit proposed in Figure 3 is presented in Figure 7. The I_O and I_2 currents have the following values: $I_O = 10\mu A$ and $I_2 = 100\mu A$, while the range of I_1 current was chosen to be between 0 and $100\mu A$.

SPICE simulation $I_{OUT}(I_2)$ for the Multiplier/Divider circuit proposed in Figure 3 is presented in Figure 8. The I_O and I_1 currents have the following values: $I_O =$

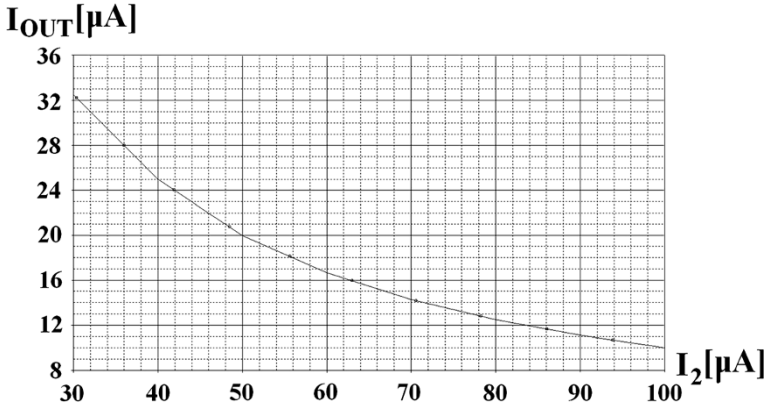

Figure 8 SPICE simulation $I_{OUT}(I_2)$ for the Multiplier/Divider circuit.

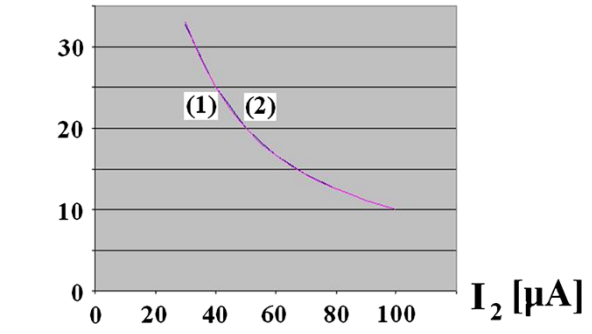

Figure 9 Comparison between the simulated and the theoretical estimated results for the proposed current Multiplier/Divider circuit.

$50\mu A$ and $I_1 = 20\mu A$, while the range of I_2 current was chosen to be between $30\mu A$ and $100\mu A$.

A comparison between the simulated and the theoretical estimated results for the proposed current Multiplier/Divider circuit is shown in Figure 9. The values of I_O and I_1 currents are $I_O = 50\mu A$ and $I_1 = 20\mu A$, while I_2 current has values between $30\mu A$ and $100\mu A$.

As a result of the particular architecture proposed for the realization of the function synthesizer structure, it presents a low-voltage operation (a minimal supply voltage of *IV* for an implementation in the mentioned technology). This value of the minimal supply voltage was obtained using the theoretical analysis of the proposed function synthesizer circuit ($V_{DD\min} = 2V_{SG} + V_{DSsat}$) and also by performing simulations based on the square-law SPICE LEVEL 3 model.

Methods

The necessity of implementing a multitude of continuous mathematical functions in CMOS technology has been solved by the original proposed function synthesizer circuit. A very important advantage of this computational structure is mainly related to its large capability of generating continuous mathematical functions: exponential, multiplying/dividing, or squaring/square-rooting functions. The original operating method was based on a new fourth-order approximation function, having a superior-order polynomial series that match the polynomial series of the approximated function. The current-mode operation and the independence of the circuit performances on the technological errors are responsible for an additional improvement of structure accuracy. The proposed function synthesizer circuit allows a relatively simple implementation in CMOS technology using only two current-mode Multiplier/Divider circuits.

The designed function synthesizer circuit has the advantages of increased modularity and controllability and of minimal design costs per implemented mathematical function. The function synthesizer is designed for implementing in $0.18\mu m$ CMOS technology and it is supplied at *IV*. SPICE simulations confirm the theoretical estimated results, showing an accuracy of 0.3% for an extended range of the input signal. This accuracy is exclusively referring to the precision of generating the previous functions, not to the additional circuits that deserve the proposed function synthesizer structure.

The speed of the original proposed function generator circuit is correlated with its overall accuracy, expecting the necessity of making a tradeoff between the previous performance parameters. Additionally, especially for extreme small values of the approximation error, the noise of the circuit can slightly degrade the circuit performances.

As an immediate application of the function synthesizer circuit, it was proposed a new exponential function generator based on a particular fourth-order approximation function. The circuit has a dynamic range of approximately 33 dB, in the conditions of limiting the error to 1 dB.

Abbreviations

CMOS: complementary metal oxide semiconductor; MOS: metal oxide semiconductor; VLSI: very large-scale integration.

Competing interests

The author declares that they have no competing interests.

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