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# A hot hole-programmed and low-temperature-formed SONOS flash memory

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## Abstract

In this study, a high-performance  $Ti_xZr_ySi_zO$  flash memory is demonstrated using a sol-gel spin-coating method and formed under a low annealing temperature. The high-efficiency charge storage layer is formed by depositing a well-mixed solution of titanium tetrachloride, silicon tetrachloride, and zirconium tetrachloride, followed by 60 s of annealing at 600°C. The flash memory exhibits a noteworthy hot hole trapping characteristic and excellent electrical properties regarding memory window, program/erase speeds, and charge retention. At only 6-V operation, the program/erase speeds can be as fast as 120:5.2  $\mu$ s with a 2-V shift, and the memory window can be up to 8 V. The retention times are extrapolated to  $10^6$  s with only 5% (at 85°C) and 10% (at 125°C) charge loss. The barrier height of the  $Ti_xZr_ySi_zO$  film is demonstrated to be 1.15 eV for hole trapping, through the extraction of the Poole-Frenkel current. The excellent performance of the memory is attributed to high trapping sites of the low-temperature-annealed, high- $\kappa$  sol-gel film.

**Keywords:** Sol-gel; Hole trapping; Flash memory

## Background

Silicon-oxide-nitride-oxide-silicon (SONOS)-type memory is widely used for nonvolatile memory [1]. Compared to conventional floating-gate memory, SONOS-type memory has the advantage of high data retention, high endurance, and fast program/erase (P/E) speed [2]. However, the primary drawback of this memory type is that a higher voltage (typically >10 V) is required to inject carriers into the charge trapping layer, which results in excessive power consumption and leakage current. A device with low operation voltage is necessary for the development of high-performance memory [3].

Recently, high- $\kappa$  materials have been considered as an effective charge storage material to achieve a faster program speed and improved charge retention [4,5]. Numerous technologies have been developed for the preparation of various high- $\kappa$  films, including the sol-gel method, atomic layer deposition, physical vapor deposition, and chemical vapor deposition [6-9]. Among them, the sol-gel method is an appealing technique. Using this method, the high- $\kappa$  film can be easily

synthesized by mixing many types of materials in a solvent, followed by a post-anneal process after spin-coating on a substrate [10]. The advantages of the sol-gel method include simplicity, low cost, good uniformity, and compatibility with the current production lines of semiconductor plants [11]. However, performing high-temperature post-annealing to obtain a satisfying high- $\kappa$  film was unavoidable in previous studies [6, 10-13]. The high-temperature post-annealing, which is typically above 900°C, hinders the wide application of the sol-gel method, such as in thin-film transistors or flexible devices.

In this study, a high-quality  $Ti_xZr_ySi_zO$  film was synthesized using the sol-gel method and low-temperature post-anneal. The sol-gel-derived  $Ti_xZr_ySi_zO$  film was applied as the charge storage layer of the SONOS-type flash memory. Identical to the high-temperature sample, the low-temperature post-annealed memory shows a noteworthy hot hole trapping characteristic and exhibits a lower operation voltage, faster P/E speed, and better data retention than previously demonstrated.

## Methods

The fabrication of sol-gel-derived memory was started with a local oxidation of silicon isolation process on a

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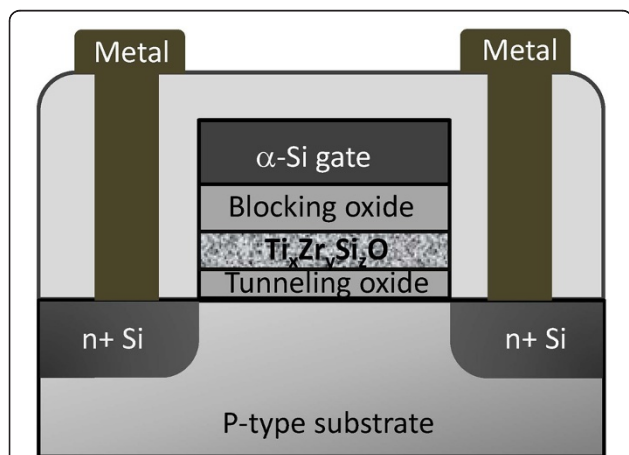
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p-type (100), 6-in. Si substrate. A 4-nm tunneling oxide was thermally grown at 925°C in a furnace. A sol-gel solution containing zirconium tetrachloride ( $ZrCl_4$ ), silicon tetrachloride ( $SiCl_4$ ), and titanium tetrachloride ( $TiCl_4$ ) was then spin-coated onto the substrate at 3,000 rpm for 60 s at ambient temperature. The sol-gel solution used ethanol as the solvent, and the molar ratio of the mixture for  $ZrCl_4/SiCl_4/TiCl_4$ /ethanol was 1:1:1:1,000.

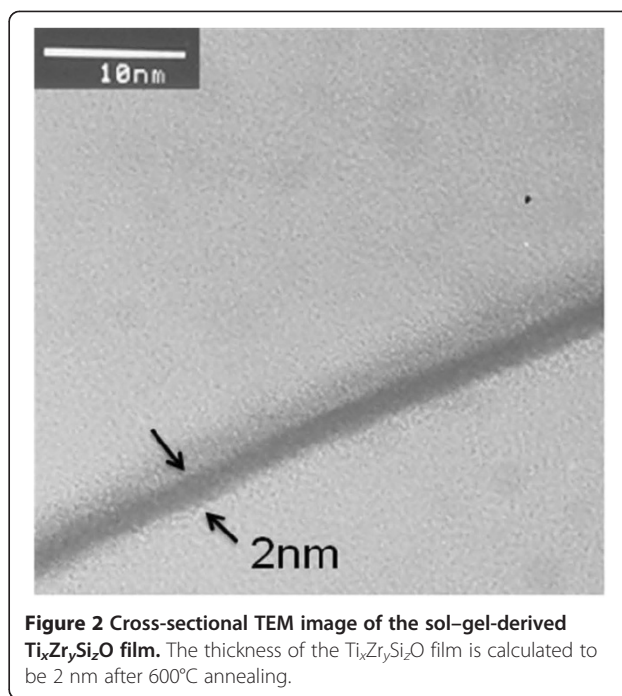
After the sol-gel film was coated, a rapid thermal annealing (RTA) process was conducted at 600°C for 60 s in an oxygen ambience. During the RTA process, a compound layer of metal-oxide-silicate containing titanium and zirconium was formed. A 10-nm blocking oxide film and 200-nm amorphous Si film were then deposited subsequently. The blocking oxide was grown by plasma-enhanced chemical vapor deposition, using silane ( $SiH_4$ ) and nitrous oxide ( $N_2O$ ) as the precursors to form a 10-nm  $SiO_2$ . The 200-nm amorphous Si film, used as the gate electrode, was deposited in the same system using the  $SiH_4$  precursor. After gate patterning,  $As^+$  ions were implanted at 20 keV with a dosage of  $5E15\text{ cm}^{-2}$  and annealed at 600°C for 24 h to define the source and drain. Finally, a 500-nm tetraethyl orthosilicate oxide was formed as the passivation layer, and the subsequent processes were used to fabricate the memory. The schematic structure of the  $Ti_xZr_ySi_zO$  flash memory is shown in Figure 1. The channel width and length of the memory were 10 and 0.35  $\mu\text{m}$ , respectively.

## Results and discussion

Figure 2 shows the cross-sectional transmission electron microscopy (TEM) image of the sol-gel-derived



**Figure 1** Schematic structure of the  $Ti_xZr_ySi_zO$  flash memory. The  $Ti_xZr_ySi_zO$  thin film was used here as the charge trapping layer.

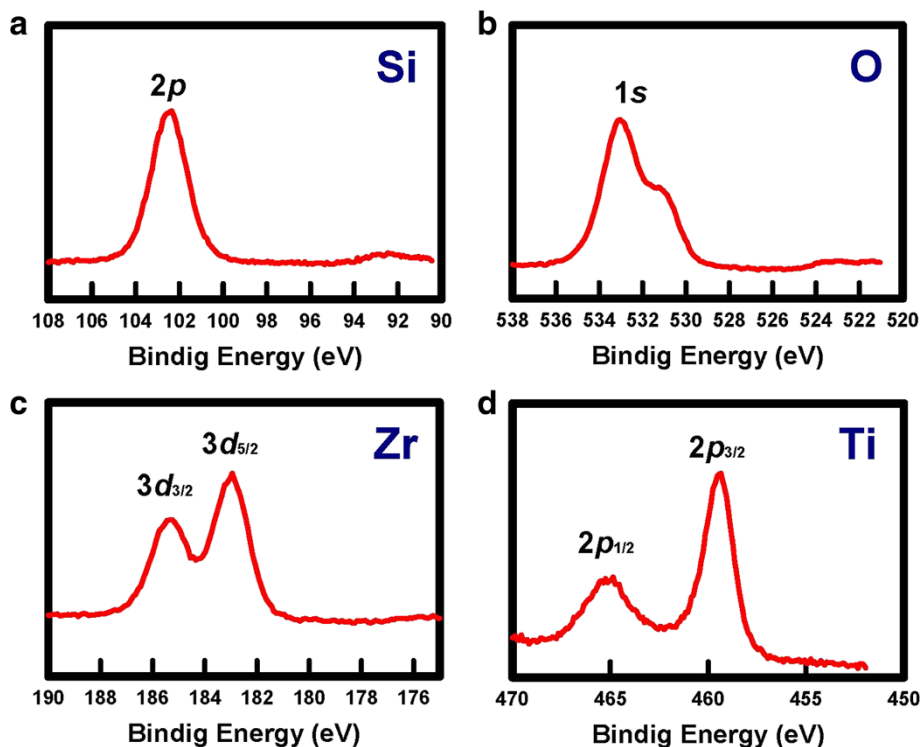


**Figure 2** Cross-sectional TEM image of the sol-gel-derived  $Ti_xZr_ySi_zO$  film. The thickness of the  $Ti_xZr_ySi_zO$  film is calculated to be 2 nm after 600°C annealing.

$Ti_xZr_ySi_zO$  film annealed at 600°C. A continuous and smooth film of 2 nm in thickness was observed, suggesting that no obvious film morphology occurred in the sample annealed at 600°C. The composition of the sol-gel-derived  $Ti_xZr_ySi_zO$  film was analyzed by X-ray photoelectron spectroscopy (XPS), and the Si 2p, O 1s, Zr 3d, and Ti 2p spectra of the  $Ti_xZr_ySi_zO$  film are shown in Figure 3a,b,c,d, respectively. The peaks in the figures indicate the component formation of the  $Ti_xZr_ySi_zO$  film.

Figure 4 shows the  $I_d-V_g$  curves of the  $Ti_xZr_ySi_zO$  memory in fresh, program, and erase states. The measured condition for the program operation was  $V_g = -8\text{ V}$ ,  $V_d = 8\text{ V}$ , and 1 ms, and that for the erase operation was  $V_g = 8\text{ V}$ ,  $V_d = 8\text{ V}$ , and 1 ms. The characteristic curve shows a 3.7-V leftward shift after the program operation and then a shift back to the original, fresh state after the erase operation. Instead of applying a positive gate bias for programming previous cases, a negative gate bias was used to program the  $Ti_xZr_ySi_zO$  memory. That is, a band-band hot hole (BBHH) was used to program, whereas a channel hot electron (CHE) was used to erase this memory. Programming was also attempted by injecting the electrons into the charge trapping layer, according to the method most previous studies reported, by applying a positive voltage to both gate and drain electrodes. However, only a minimal shift of the curve was observed.

Based on the  $I_d-V_g$  measurement results, band diagrams of the  $Ti_xZr_ySi_zO$  memory in the program and



**Figure 3** XPS spectra of the sol-gel-derived  $Ti_xZr_ySi_zO$  film. (a) Si 2p, (b) O 1s, (c) Zr 3d, and (d) Ti 2p spectra.

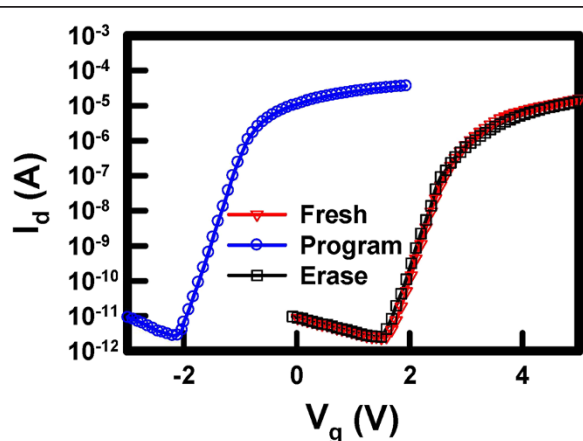
erase operations are illustrated in Figure 5a,b, respectively. For the program operation, a BBHH was used; therefore, hot holes were injected from the silicon substrate and captured by the hole traps in the charge trapping layer, as shown in Figure 5a. In the erase operation, positive gate and drain voltages were applied. Channel hot electrons were injected and then recombined with the holes in the trap site, as shown in Figure 5b.

To demonstrate the thermal emission of carriers in the trap of the  $Ti_xZr_ySi_zO$  memory, the Poole-Frenkel current was measured. The Poole-Frenkel current explains the hot hole trapping effect of the memory [14,15]. The expression for current density according to the Poole-Frenkel emission can be written as [16]:

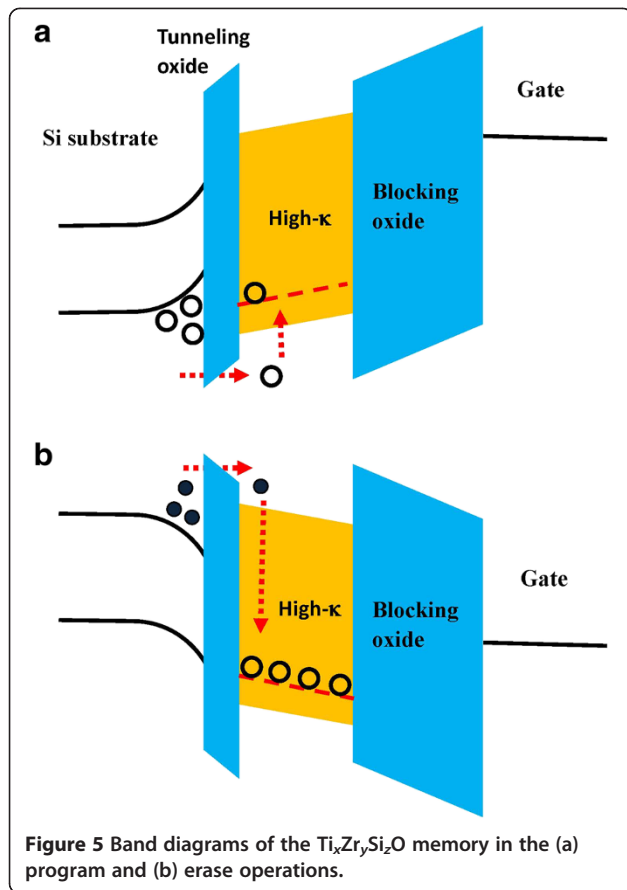
$$J_{FP} = aE_{ox} \exp \left[ \left( (bE_{ox})^{1/2} - \phi_t \right) q / k_b T \right],$$

where  $K_b$ ,  $T$ ,  $a$ ,  $b$ , and  $\phi_t$  are the Boltzmann constant, the measurement temperature, a constant that depends on the trap density, a constant that depends on the electric permittivity, and the depth of the trap potential well, respectively.

If hot hole trapping is the dominant mechanism for programming the  $Ti_xZr_ySi_zO$  memory, the extracted current should follow the Poole-Frenkel emission, that is, a linear slope for the plot of current density ( $J/E$ ) versus the square root of the applied electrical field. Therefore, a negative bias from 0 to -20 V was applied to the gate electrode with a constant 4-V drain bias at measurement to simulate the hot hole program of the memory. Figure 6a shows the plot of current density versus the square root of the applied electrical field under various measuring temperatures at hot hole program operation. Linear regions of the plot imply that the current of  $Ti_xZr_ySi_zO$  memory

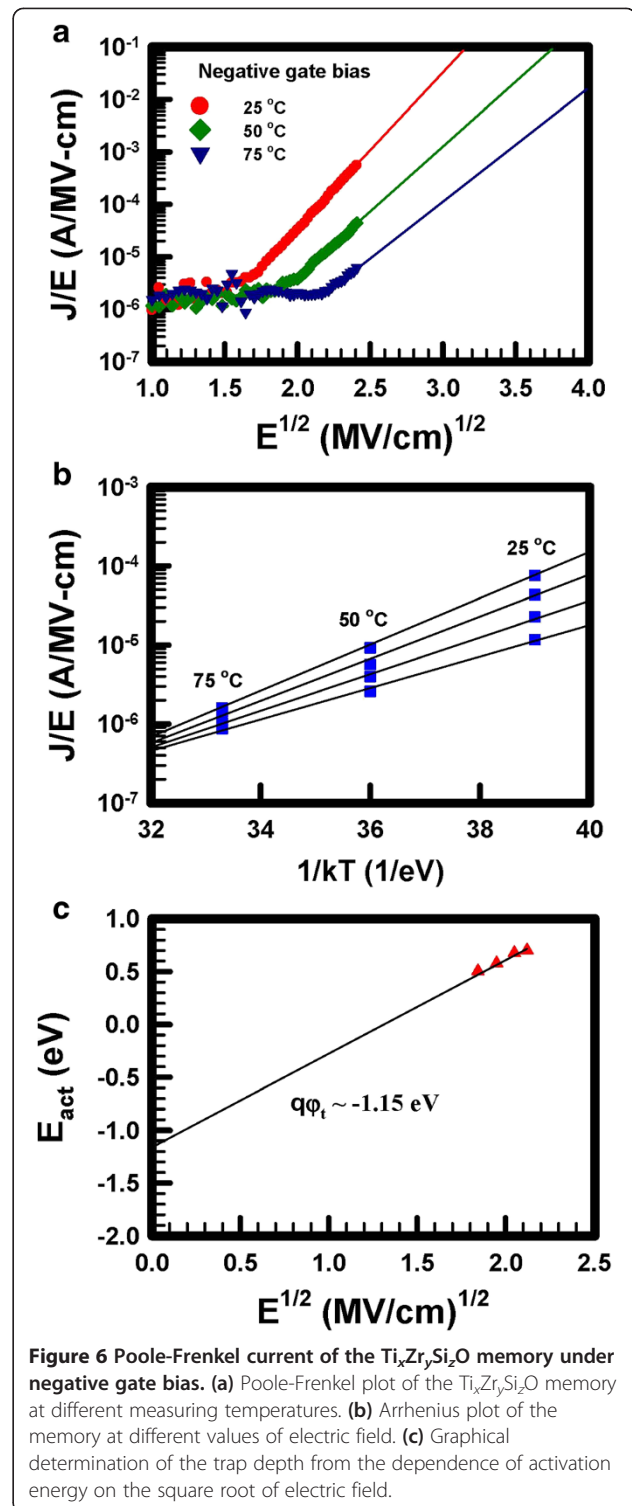


**Figure 4**  $I_d$ - $V_g$  characteristics of the sol-gel-derived  $Ti_xZr_ySi_zO$  memory at fresh, program, and erase states. The memory window is ca. 3.7 V.



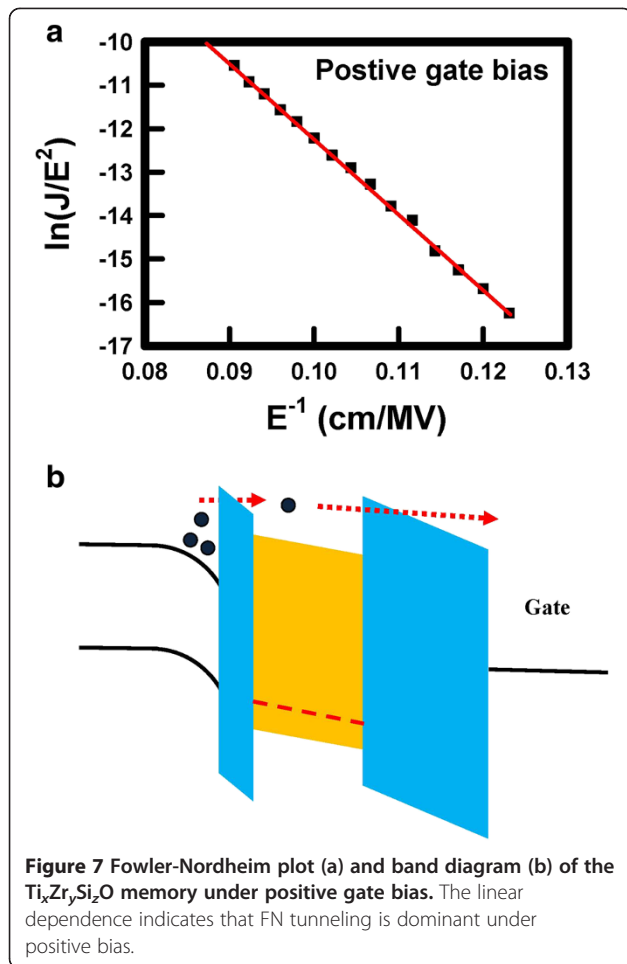
follows the Poole-Frenkel emission. Figure 6b shows an Arrhenius plot of the memory extracted from Figure 6a. The linear dependence of the current densities versus temperatures implies that the charges exhibit a thermally activated behavior, which is consistent with the Poole-Frenkel emission. The barrier height of the  $Ti_xZr_ySi_zO$  film to silicon oxide can be extracted as approximately 1.15 eV for hole trapping, using the Poole-Frenkel current, which is shown in Figure 6c.

In addition to hot hole trapping, the Poole-Frenkel current of the hot electron program was also measured by applying a positive gate voltage. However, the result showed a nonlinear curve. Conversely, the measured result showed a linear dependence of current density, divided by the electric field squared, versus the reciprocal electric field (Figure 7a), which is represented by Fowler-Nordheim tunneling. This result may indicate that the energy band of the  $Ti_xZr_ySi_zO$  film exhibits shallow trap potential well that could not preserve electrons when applying a positive gate voltage. Therefore, electrons were injected into the charge trapping layer and then went through the blocking oxide to the gate electrode. The band diagram of the Fowler-Nordheim (FN) operation



is illustrated in Figure 7b. The expression of Fowler-Nordheim tunneling on an electric field can be given by [17]:

$$J_{FN} = cE_{ox}^2 \exp(-d/E_{ox}),$$



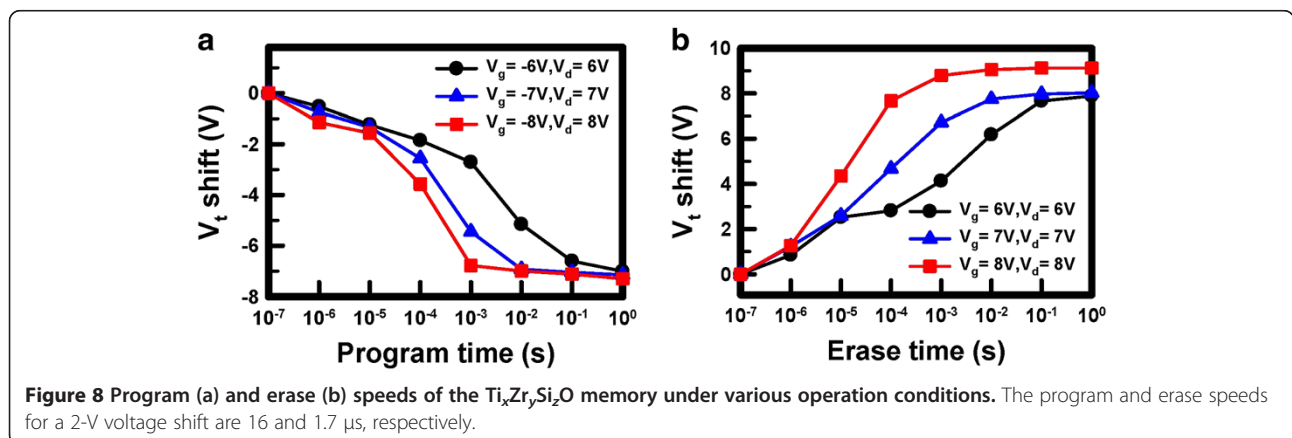
where  $c$  represents a constant that depends on the energy barrier height and  $d$  is a constant that depends on the electric effective mass for tunneling.

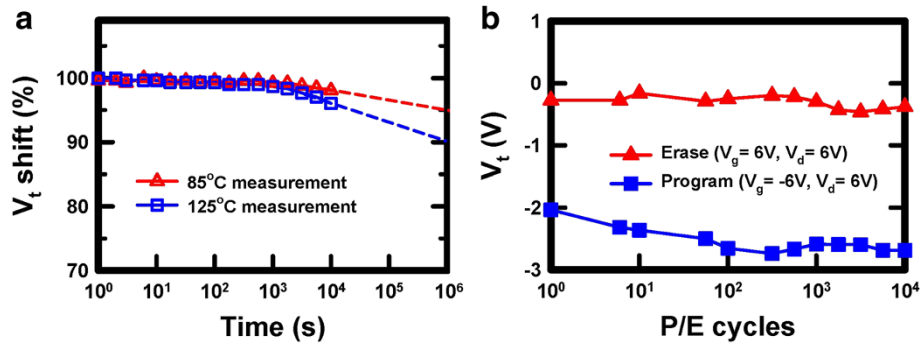
Figure 8a,b shows the program and erase speeds, respectively, of the  $Ti_xZr_ySi_2O$  memory under various

operation conditions. Because the memory exhibited the hot hole trapping property, BBHH was applied to programming and CHE was applied to erasing.

As shown in Figure 8a, the threshold voltage ( $V_t$ ) shift increased with increasing operation voltage; the more 'hot' holes were generated and injected into the charge storage layer. The maximum memory window can be as large as 8 V. The program speed is 16  $\mu s$  with a  $-2$ -V  $V_t$  shift for the program conditions of  $V_g = -8$  V and  $V_d = 8$  V. Compared with the erase speed shown in Figure 8b, only 1.7  $\mu s$  is required for a 2-V  $V_t$  shift. It is reasonable that the erase speed is approximately ten times faster than the program speed because this memory is programmed by BBHH and erased by CHE. Even at only 6-V operation, the P/E speed can be as fast as 120:5.2  $\mu s$  with a 2-V  $V_t$  shift. The fast P/E speed at such low operation voltage is superior to that demonstrated in previous studies [18-20] and is beneficial to the development of high-performance memory. This favorable result is ascribed to the formation of more trapping sites in the  $Ti_xZr_ySi_2O$  film at 600°C annealing, and hence, more carriers can be captured in the traps.

A highly reliable charge retention characteristic of the memory is demonstrated in Figure 9a. The normalized  $V_t$  shift is defined as the ratio of the  $V_t$  shift at the time of interest and at the beginning. The curve is obtained under the program conditions of  $V_g = -7$  V and  $V_d = 7$  V for 1 ms at 85°C and 125°C, respectively. As time extrapolated up to  $10^6$  s, the data retention measured at 85°C shows only 5% charge loss and that at 125°C shows only 10% charge loss. Figure 9b shows the endurance characteristics of the  $Ti_xZr_ySi_2O$  memory. The measurement conditions are  $V_g = -6$  V and  $V_d = 6$  V for programming and  $V_g = V_d = 6$  V for erasing. Despite a small drift of the





**Figure 9** Reliability characteristics of the  $Ti_xZr_ySi_zO$  memory. (a) Retention characteristic of the memory at measurement temperatures of 85°C and 125°C. (b) Endurance characteristic of the memory up to  $10^4$  program/erase cycles.

threshold voltage for both P/E operations, the memory window remained at around 2 V after  $10^4$  P/E cycles. No substantial window narrowing was observed. The threshold voltage downward shift is mainly caused by the interface trap generation and hole trapping in the tunneling oxide.

The electrical performance of the  $Ti_xZr_ySi_zO$  memory is summarized in Table 1 and compared with other sol-gel-derived memories [8,13,21]. As seen in the table, the  $Ti_xZr_ySi_zO$  memory in this study exhibits improved electrical performance, particularly in retention properties. The  $Ti_xZr_ySi_zO$  memory at either 600°C or 900°C annealing can be operated at much higher erase speeds compared to other materials. This is because the erase of the  $Ti_xZr_ySi_zO$  memory is operated by CHE. Moreover, the operation voltage of the sol-gel-derived  $Ti_xZr_ySi_zO$  memory can

be decreased to only 6 V, without sacrificing its performance.

### Conclusion

We demonstrated a high-performance sol-gel-derived  $Ti_xZr_ySi_zO$  memory in this study. The memory exhibits a notable hot hole program characteristic, and hence, a much higher erase speed is achieved. The barrier height for the  $Ti_xZr_ySi_zO$  film to silicon oxide was estimated to be approximately 1.15 eV for hole trapping, using the Poole-Frenkel emission model. Unlike other sol-gel-derived memories that require a higher temperature annealing process, this  $Ti_xZr_ySi_zO$  memory with relatively low-temperature annealing exhibits excellent electrical performance such as low-voltage operation, fast P/E speed, and robust data retention.

**Table 1** Comparison of P/E speed and data retention of the sol-gel-derived high- $\kappa$  memory devices

	This work ( $Ti_xZr_ySi_zO$ with 600°C annealing)	$Ti_xZr_ySi_zO$ NC with 900°C annealing [13]	$Zr_xHf_ySi_zO$ NC with 900°C annealing [6]	$HfSi_xO_y$ with 900°C annealing [21]
Program speed (2-V shift)	$1.6 \times 10^{-5}$ s ( $V_g = -8$ V, $V_d = 8$ V)	$2.4 \times 10^{-5}$ s	$3 \times 10^{-5}$ s	$2 \times 10^{-2}$ s
	$1.2 \times 10^{-4}$ s ( $V_g = -6$ V, $V_d = 6$ V)	( $V_g = -8$ V, $V_d = 8$ V)	( $V_g = 10$ V, $V_d = 9$ V)	( $V_g = V_d = 10$ V)
	$1.7 \times 10^{-6}$ s ( $V_g = V_d = 8$ V)	$1.9 \times 10^{-6}$ s	$2 \times 10^{-3}$ s	$5 \times 10^{-5}$ s
Erase speed (2-V shift)	$5.2 \times 10^{-6}$ s ( $V_g = V_d = 6$ V)	( $V_g = V_d = 8$ V)	( $V_g = -10$ V, $V_d = 9$ V)	( $V_g = -10$ V, $V_d = 10$ V)
	Retention at 85°C	5% loss ( $10^6$ s)	12% loss ( $10^6$ s)	11% loss ( $10^6$ s)
Retention at 125°C	10% loss ( $10^6$ s)	22% loss ( $10^6$ s)	30% loss ( $10^6$ s)	NA

NC nanocrystal.

### Abbreviations

BBHH: Band-band hot hole; CHE: Channel hot electron;  $J/E$ : Current density; P/E: Program/erase;  $\text{SiCl}_4$ : Silicon tetrachloride; RTA: Rapid thermal annealing; SONOS: Silicon-oxide-nitride-oxide-silicon; TEM: Transmission electron microscopy;  $\text{TiCl}_4$ : Titanium tetrachloride;  $\text{ZrCl}_4$ : Zirconium tetrachloride; XPS: X-ray photoelectron spectroscopy.

### Competing interests

The authors declare that they have no competing interests.

### Authors' contributions

Y-MC, S-HL, Y-PH, and C-CW carried out the experiment and measurement. J-YW and C-CW prepared the manuscript. W-LY and C-CW technically supported the study. All authors read and approved the final manuscript.

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