Jordan et al. Journal of Solid State Lighting (2015) 2:4
DOI 10.1186/s40539-015-0023-z

Journal of Solid State Lighting
a SpringerOpen Journal

RESEARCH Open Access

Advanced packaging methods for high-power LED modules

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Abstract

LED luminaires are already beyond retrofit systems, which are limited in heat dissipation due to the old fitting standards. Actual LED luminaries are based on new LED packages and modules. Heat dissipation through the first and second level interconnect is a key issue for a successful LED package. Therefore the impact of known bonding technologies as gluing and soldering and new technologies like sintering and transient liquid phase soldering were analyzed and compared. A realized hermetic high power LED package will be shown as example. The used new techniques result in a module extremely stable against further assembly processes and harsh operating conditions.

Keywords: High power LEDs; Heat dissipation; Sintering; Transient liquid phase soldering; Hermetic packaging

Background

Gluing

Die and wire bonding of LEDs with glued LEDs is the most common way to assemble the LEDs. Even though the TIM (thermal interface material) increased the efficiency in the past, the all over heat dissipation is limited due to the thermal interface resistance (see Fig. 1). This is depending on the imperfect contact of the filler particles with the surface of the connected parts. Beside the low heat dissipation [1–4], delamination is a typical failure mode for glued LEDs which results in a total failure or accelerated aging due to overheating. As gluing is well known, no further investigations were made in this work, but glued samples were used as reference for the other techniques.

Soldering

Today soldering becomes more and more important for high power LEDs [5]. The heat dissipation is up to 30 times better, due to the heat conductivity of the solder itself (*e.g.* Au80Sn20 with 54 W/mK) and the thermal interface resistance is not relevant. For soldering special requests regarding the metallization layers of the LEDs and substrates have to be taken into account. The correct stack of adhesion layer, barrier layer, wetting layer, and solder stop layer is critical for proper packaging. Those are depending on the substrate of the LED (*e.g.* Si, Ge, Cu, sapphire) and the submount (*e.g.* Si, AlN, Al2O3, IMS). If a big manufacturer can control all steps by himself, promising combinations can be designed in advance and the challenge is lower. But often SMEs (Small

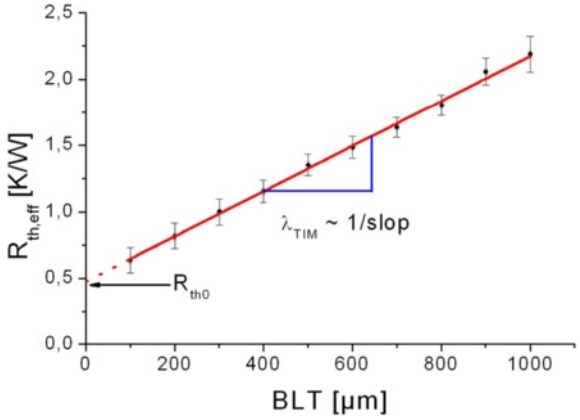

Fig. 1 Extrapolation of the TIM thickness to zero results in the thermal interface resistance [19, 20]

and Medium-sized Enterprises) have to use available parts and combine them successful. In the following examples copper based LEDs are assembled on Silicon based Submount. A special challenge was the CTE (Coefficient of Thermal Expansion) mismatch. The preferred solder was Au80Sn20 (see Fig. 2) due to the high heat conductivity and melting point above later SMD processes.

A common and inexpensive way for die soldering is reflow soldering in an inert atmosphere [6]. Therefor the first tests were done this way. Figure 3 shows the cross section of the assembled LED. Voids in the solder are visible, due to remaining oxides but more important are the cracks in the silicon due to the low ductility of the AuSn solder and the ΔCTE of about 12 ppm.

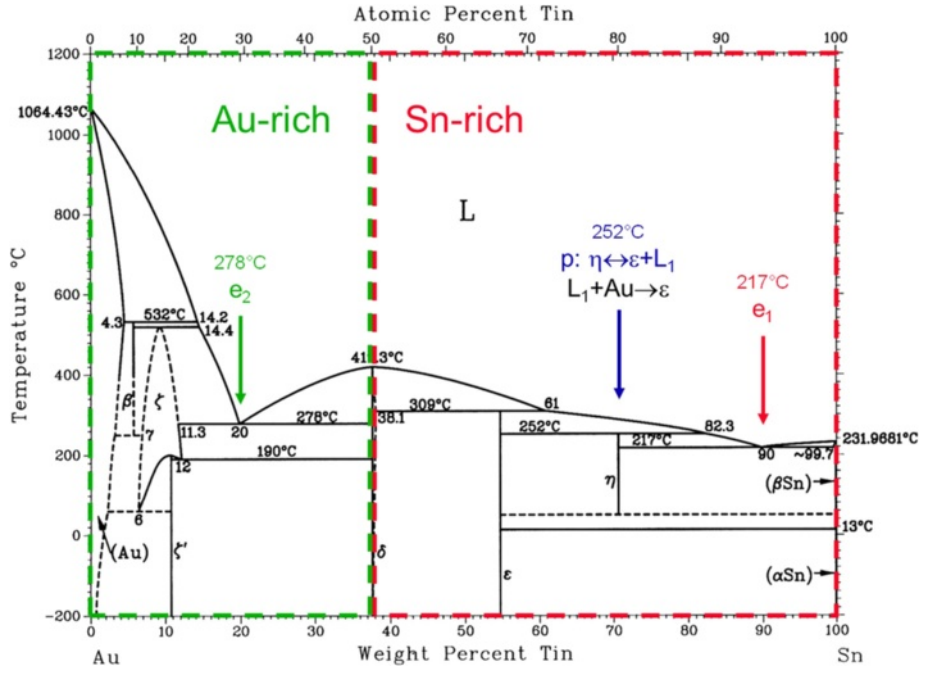

Fig. 2 AuSn phase diagram

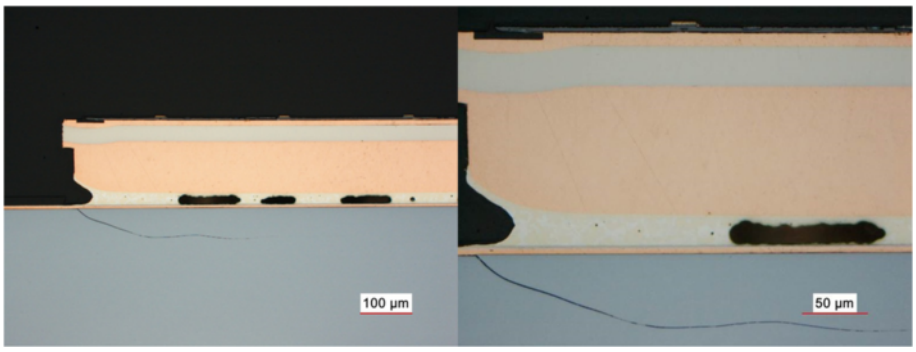

Fig. 3 Assembly tests with AuSn reflow soldering in an inert atmosphere

A second approach for soldering is thermode soldering, were die and substrate are fixed to independent moveable and heatable tools. This technique offers the advantage of a better control of parallelism and position of the die but is slow for high volume, low quality production as each die is handled sequential. High parallel thermode soldering processes are under investigation. With lower magnification this interface looked acceptable (Fig. 4, left), but a closer look (Fig. 4, right) shows, that the formerly voids build oxide layers as an almost continuous gap. Even if the heat can dissipate across this gap it is a high mechanical reliability risk [7].

As AuSn was excluded for this combination of material, SnAg was recommended and a proper reflow soldering process was developed. The key point of the optimization was not to damage the die, to keep it in position, and compensate the CTE mismatch between the parts. Figure 5 shows such a highly reliable interconnection which was built in a mass production suitable reflow process. These assemblies were used for the later comparative analysis.

Thermo compression

Thermo compression is also a well-known process. In the last years the simple but time consuming stud bumping of the parts was substituted by wafer level electroplating of bumps, but this brings out new challenges. On the one hand the flat surface of the electroplated bumps needs higher forces and on the other hand the lower compression in height makes the process more critical regarding the initial height of the bumps. To

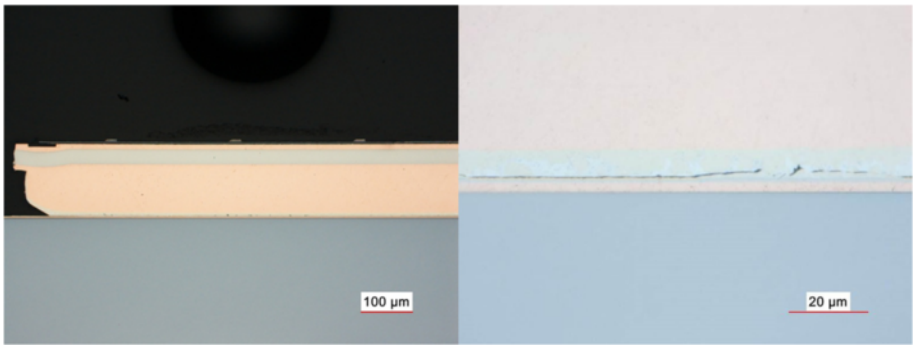

Fig. 4 Assembly tests with AuSn thermode soldering in an inert atmosphere

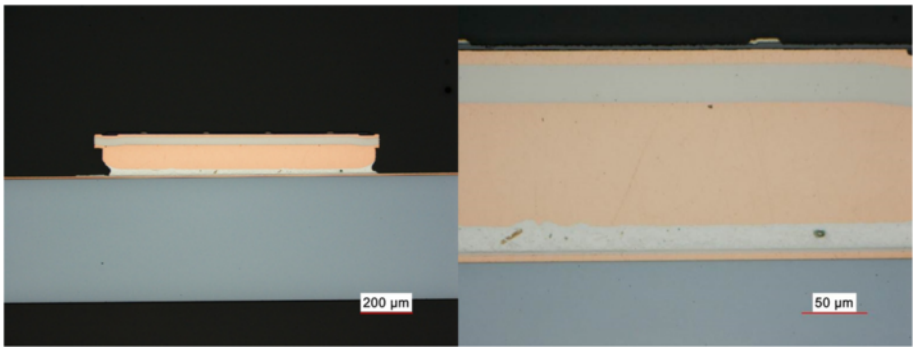

Fig. 5 Assembly tests with SnAg reflow soldering in an active atmosphere

compensate for these disadvantages a further development was done at Fraunhofer IZM. The electroplated bumps are not solid any more but are built of a gold nano sponge [8] (Fig. 6). This sponge needs generally lower parameters for thermo compression bonding and can compensate height differences of the bumps as well as local disturbances like surface defects or particles.

Sintering

A further challenging technique is silver sintering (Fig. 7). In contrast to soldering the connecting material never becomes liquid. This results in a high position and tilt stability of the process. Furthermore the pure metal interconnect has up to 10 times better heat conductivity than eutectic solders (380 W/mK have been achieved by this process [9]) and therefore up to 300 times better than glue. A third advantage is the high ductility, which enables the possibility to connect parts with higher CTE mismatch.

As sintering is a highly time consuming process, common sintering under controlled pressure will not be successful for production. The challenge was to develop a pressure

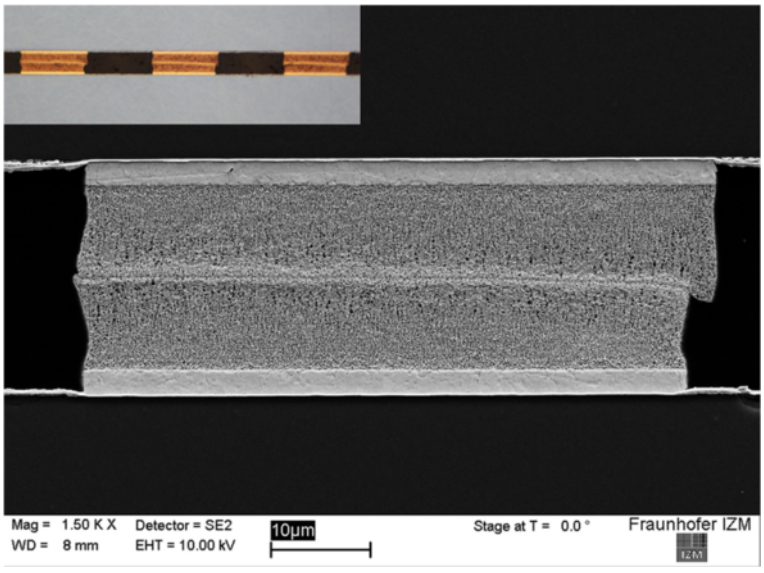

Fig. 6 Nano sponge TC bonded interconnect

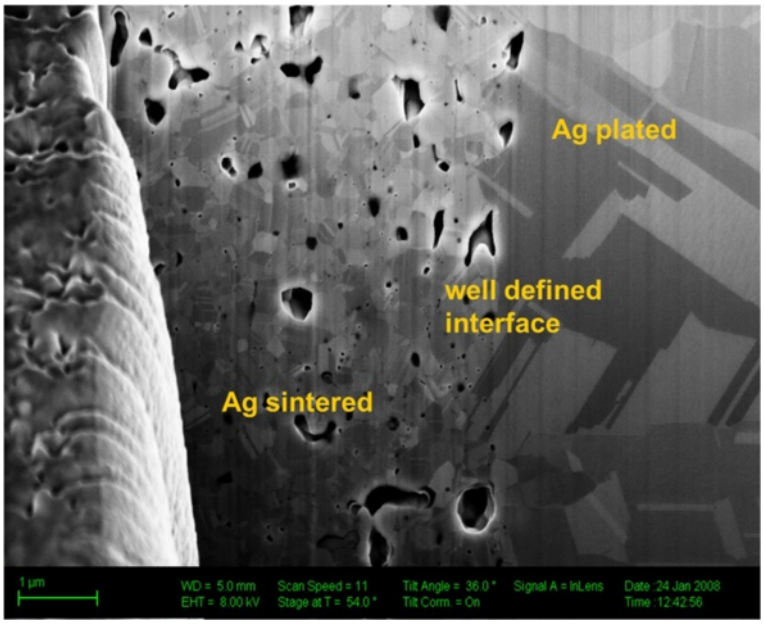

Fig. 7 Sintered silver | silver interface

less sintering process [10, 11]. LED-chips, substrates, time and temperature are varied in a wide range to reach a proper parameter set. Not all results were foreseeable, as the worse shear force for higher process temperatures (Fig. 8). Later investigations have shown, that the diffusion of lower layer metals disturb the sintering process. For the comparative test the optimized parameters were used.

Transient liquid phase soldering

Even if silver sintering is a promising technique, high material costs and long processes are significant disadvantages. Transient liquid phase soldering is an approach with the goal to do assembly with standard pick and place equipment in a quick reflow process [12–16]. For this purpose standard Sn-based solder paste will be supplemented with copper powder (Fig. 9).

During reflow liquid tin-based solder encloses and dissolves the copper. With increasing amount of copper Cu6Sn5 and Cu3Sn forms and the solder solidifies chemically. Using the right amount of copper and a well-defined temperature profile results

Temperature	Chip A on Ceramic	Chip B on Ceramic	Chip A on IMS	Chip B on IMS
225 °C	(8,4 ± 2,1) N	(8,8 ± 3,0) N	(7,6 ± 3,1) N	(7,5 ± 1,5) N
275 °C	< 0,5 N	(8,3 ± 1,9) N	< 2,0 N	(12,7 ± 2,9) N

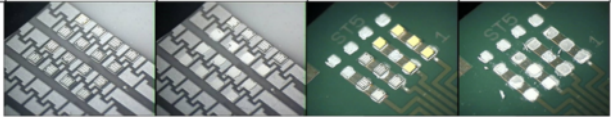

Fig. 8 Shear strength comparison of different pressure less sintering samples (all dice 1 mm^2)

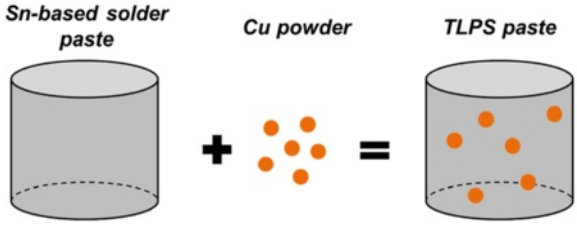

Fig. 9 Principle of transient liquid phase solder paste

in a homogeneous interconnection layer with completely transformed solder and a melting point not below 415 °C (Fig. 10).

Although this technique has clear benefits, it is not a universal solution. *E.g.* higher differences of the coefficient of thermal expansion between chip and substrate cannot be compensated due to the stiff character of the copper tin phases.

Methods

Basics

To receive the temperature at the pn-junction mostly two physically effects are used:

a) Forward Voltage
As a first approximation the forward voltage is depending on the electron band gap and the Boltzmann distribution. The Boltzmann distribution is temperature depending and therefore the forward voltage is decreasing with increasing temperature. The slope is in a range of 2 mV/K.

b) Wavelength Shift
The targeted recombination of the electron from the conducting band (n-type semiconductor) with the holes of the valence band (p-type) is a light emitting process. The wavelength of the emitted light is again depending on the electron band gap, as the forward voltage. If the temperature increases the bandgap decreases and therefore the wavelength shifts to the red. Unfortunately the shift of the wavelength is not direct proportional to the energy difference. Based on Eq. 1 a wavelength shift of 0.8 nm/K will result in the red range, but for the bluish region

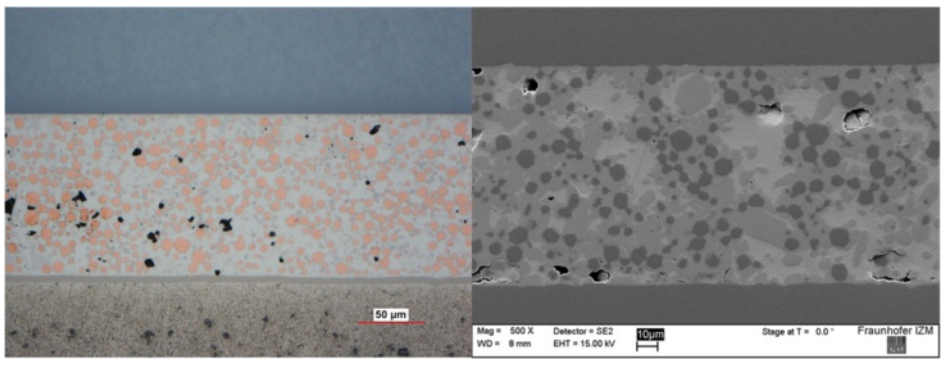

Fig. 10 Cross section built with transient liquid phase soldering (left: light microscopy, right: SEM)

of the visible spectra only a wavelength shift of 0.25 nm/K will occur, which is hardly measureable.

$$E[eV] = h[eVs]\frac{c[m/s]}{\lambda[m]}, \mathrm{h} = 4,1357\text{E-}15 \ \text{eVs}, \ \ \mathrm{c} = 3,0000\text{E}8 \ \text{m/s} \tag{1}$$

Due to the low wavelength shift at short wavelengths the measurement of the forward voltage becomes more important and therefore the measurement technique was established and improved.

Procedure

A real LED will not opened with a certain voltage, the forward voltage, and afterwards let the current flow with any resistance, like an ideal diode [Fig. 11, left side]. In fact it behaves like a diode with ohmic resistors in parallel (parasitic current) und series (inner resistance) [Fig. 11, right side].

Therefore the temperature depending forward voltage cannot be measured under running conditions, as the influence of the ohmic portion of the voltage drop becomes grave with higher current. Also the calibration cannot be done at higher current, without heating the die in a non-controlled way.

Figure 12 (left) shows an example for the working range for the junction temperature measurement. If the current is chosen too high, the die will already be heated up during calibration, is the current too low, the voltage drop becomes too noisy. This area must be defined for each type of LED chip, as it is depending on wavelength and structure.

Within the working range a constant measurement current is applied and the voltage versus temperature characteristic measured for each die (Fig. 12 (right)).

The calibrated dice will afterwards be conditioned with defined ambient parameters and driven with a specified current. Immediately before measurement the current is reduced to the measurement current and the voltage transient is recorded.

Figure 13 shows a typical transient after switching down the driving current to the measurement current. The increasing voltage occurs due to the cooling of the sample. Reference measurements with ohmic resistors have shown a horizontal transient without temperature effects like the diode. To get the forward voltage in the moment of switching of the driving current, a fitting routine was used. With the simplified assumption, that to main heat equilibrations will happen between the epilayer and chip body and in parallel, but slower, between the chip and the substrate, a two exponential decay is used to fit. With the resulting forward voltage and the prior calibration the

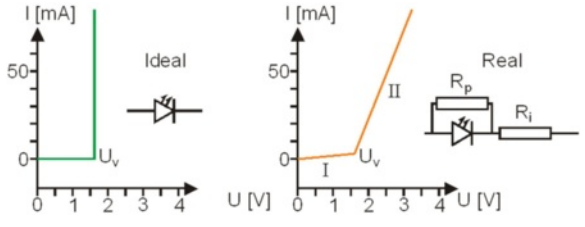

Fig. 11 Schematic UI-curve of an ideal (left) and real (right) LED

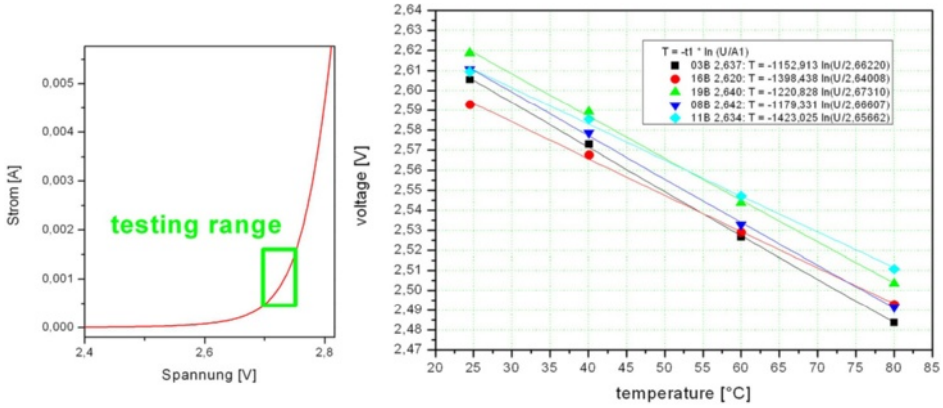

Fig. 12 Suitable range for measurement (left) and exemplary calibration of LEDs (right)

temperature at the junction at driving conditions can be calculated. Fig. 14 shows the results of 3 glued LED samples measured for three different driving currents.

Results and discussion

In the results and discussion section first the comparative measurements of the p/n-junction temperature of assemblies with different packaging technologies will be shown and finally the application of the gained information to build a hermetic LED and sensor package.

Comparative measurements

For each set of comparative measurements the same type of LEDs were used with the same type of submounts, mounted the same way to a water cooled copper cooler kept at 25 °C with a chiller. Only the first level interconnect between the chip and the submount was changed between gluing, soldering and sintering. The transient of the forward voltage was always analyzed for 100 mA, 350 mA and 700 mA driving current for each type of interconnect and at least for three samples.

From the fit of the initial forward voltage the junction temperatures are calculated using the calibration curve and summarized in the following graphs. For the shown energy in the following figures only the thermal portion was used, corrected by the energy

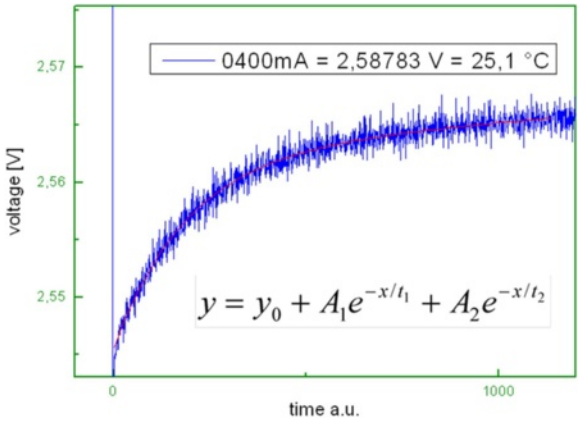

Fig. 13 Typical transient of the forward voltage if switched from driving current to measurement current

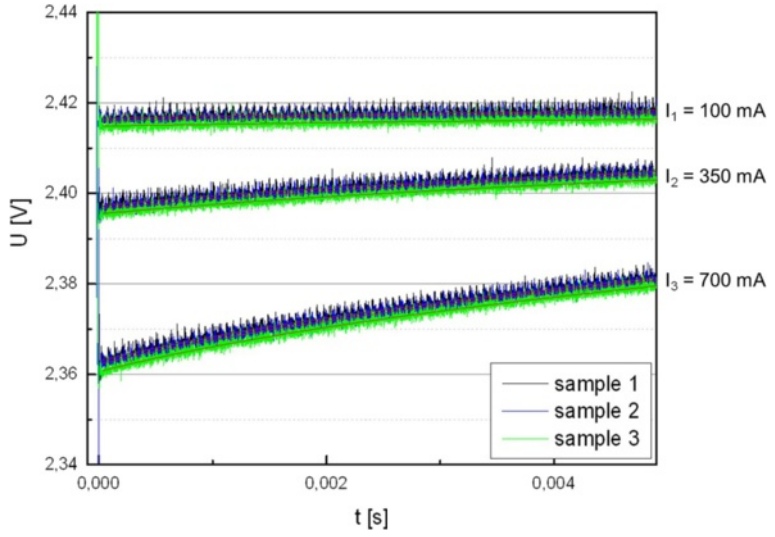

Fig. 14 Transients of glued blue LED

emitted as light. To check the relevance for a wide field of LEDs three different types were investigated. A red AlInGaP volume emitter (Fig. 15), a blue InGaN surface emitter (Fig. 16), and a white LED with chip level phosphor (Fig. 17). As the thermal resistance of the remaining system is unknown, no Rth values but absolute temperatures are given.

Independent from the LED type a clear benefit of soldering (solid line) against gluing (dot line) is visible for the heat dissipation. The advantage of sintering over soldering seems to be small, but this is related to the heat resistance of LED chip substrate, which is now the limiting factor. For further generations of substrate less LED dice, which consists only of the functional thin epitaxial layer (about 5 μm) and a metallization, sintering will become more important.

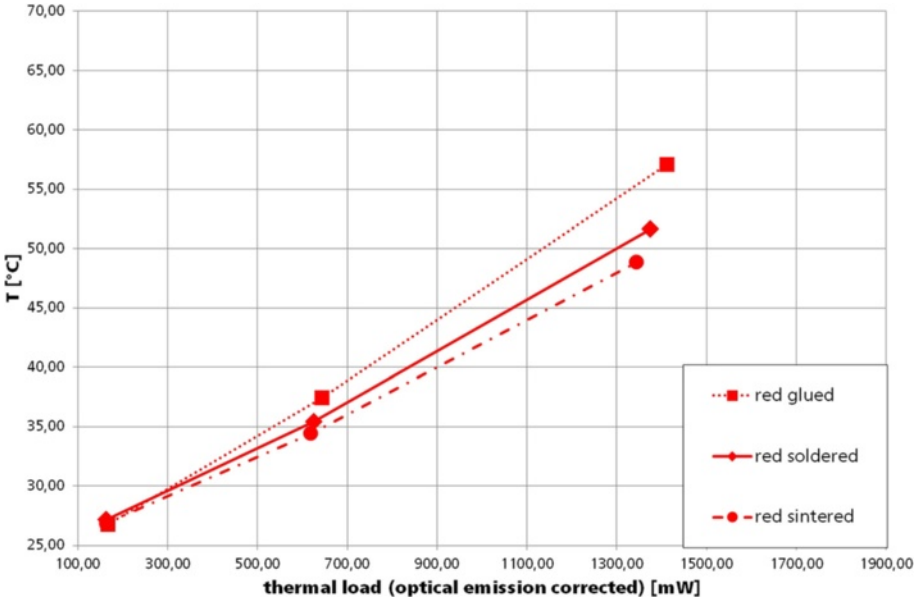

Fig. 15 Comparison of glued, soldered and sintered red LEDs

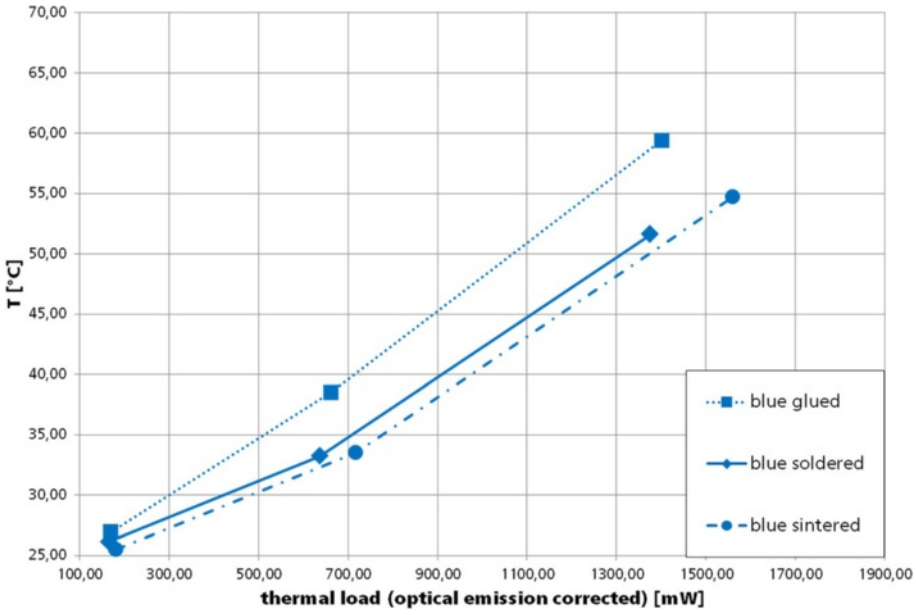

Fig. 16 Comparison of glued, soldered and sintered blue LEDs

Field of application for the p/n-junction measurement

The junction temperature is one indicator for the quality of an LED die or package. After structural analysis, which are done in house by cross sections with optical microscopy, scanning fluorescence microscopy, SEM/EDX, or focused ion beam visualization, nondestructive scanning acoustic microscopy, or computer topographic x-ray analysis the thermal bottle neck can be localized, improved and afterwards verified by additional junction temperature measurements.

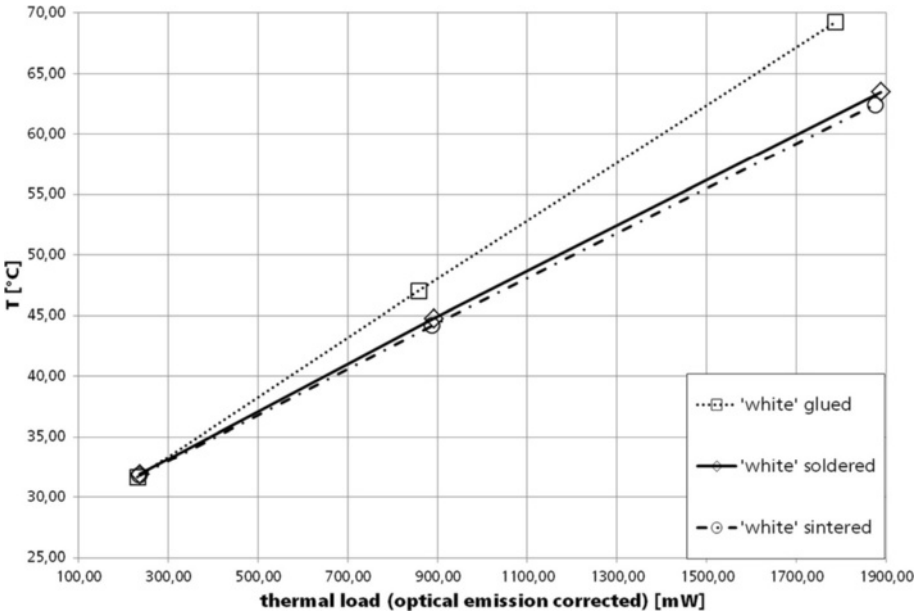

Fig. 17 Comparison of glued, soldered and sintered white LEDs

Especially for failure and reliability analysis the junction temperature is a significant indicator. Delamination or cracks cannot shown in the beginning with ohmic resistance measurement, as the changes are not significant until the die is almost completely lifted. The pn-junction temperature will change continuously with the delamination or crack. Therefore an in-situ measurement equipment was developed to measure the junction temperature during accelerated aging by heat, humidity, and temperature cycles for LED packages as well as for complete modules. Simultaneous measurements of the luminous flux, optical spectra and electrical characteristics will give a comprehensive dataset to localize and correct potential failure on a sophisticated level.

For small samples a chamber with 20 sample positions will be used. For each position forward voltage and current can be monitored and the junction temperature measurement sequence can be applied. Quick temperature changes are realized by a metal membrane below the chuck switching between a high power heater and the cold fluid from a chiller. Each position is equipped with a photodiode or an optical fiber connected to an optical switch which is connected to a spectrometer. Measurement are running completely automatically. For larger samples a climate chamber with temperature, humidity and enforced convection control will be used with a lab built measurement equipment. In the latter the measurements are semiautomatic, temperature ramps more moderate and the number of samples is limited to about 4 samples.

Application of the gained information for hermetic LED and sensor packaging

As challenging project a hermetic LED package was chosen in the European project EnLight. To achieve real hermetic packaging no polymers or porous materials can be used for the interconnection. Also the used materials should withstand harsh environmental conditions. With 1200 lm out of ~ 4,5 m^2 the heating density is with ~ 2 W/mm^2 extremely high. As the package must withstand further assembly processes without remelting only As80Sn20 solder, anodic bonding and transient liquid phase soldering is chosen. To produce the packages in an economic highly parallel way, an 8″ wafer scale packaging process was chosen.

Processing

First of all a substrate wafer with through silicon vias (Fig. 18, left) and a glass cap wafer with a reflecting spacer were produced (Fig. 18, right). Suitable dimension of the vias were calculated in advance [17]. The substrate wafer contains a large electrical

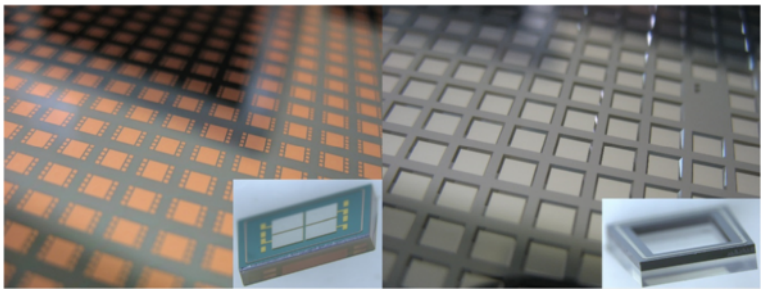

Fig. 18 Left: substrate wafer, bottom view (insert: single substrate top view), right: glass cap wafer before metallization (insert: Single cap with metallization)

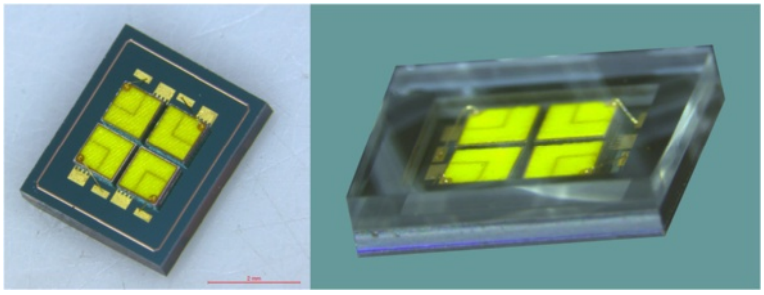

Fig. 19 Left: exemplary substrate with four white LED and wire bonds, right: complete substrate with hermetic glass cap

isolated thermal pad on the bottom side and four die bond positions on the top. The top side structure can easily adapted to available flip chip LED to avoid the wire bond and decrease the total size of the package.

In production the whole substrate wafer will be assembled with LEDs (*e.g.* die soldering & wire bonding (Fig. 19, left) or flip chip soldering or thermocompression). Afterwards the glass cap wafer will be soldered in a transient liquid phase process to the substrate wafer. Finally the assembled modules will be singulated by dicing (Fig. 19, right). Instead of the four white LEDs also three different LED can be assembled and enhanced by a monitor diode in the fourth position (Fig. 20, left). The general function of both packages was tested on a demonstration board (Fig. 20, right).

Analysis

Before the full wafer process starts, substrate level packages are built. These assembled LED packages are analyzed with different methods. As ordered equipment for gross and fine leak tests are not delivered yet, just a rough initial leak test is done. The packages are soaked with organic solvent and afterwards heated up to 250 °C. If the cap was not well sealed it will be blown away. Some dice failed this test, as the delivered LED-chip thickness increased during the project and therefor some wire bond loops touched the glass disturbing the reflow process. Further tests are done with x-ray microscopy to verify the void and gap less sealing ring (Fig. 21, left) and finally local cross section are prepared to verify whether the non remelting Cu6Sn5 phase is built or not (Fig. 21,

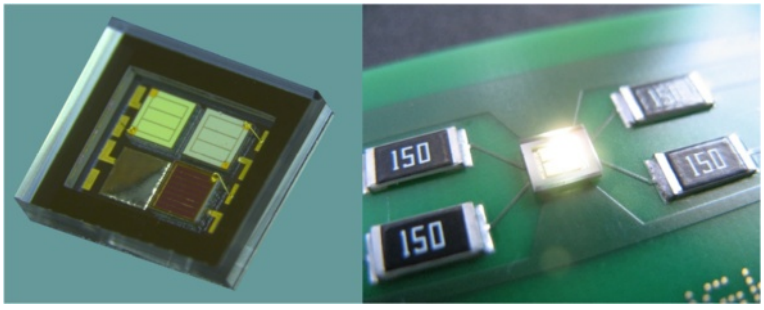

Fig. 20 Left: hermetic RGB module, position of monitor diode is free, as not delivered in time, right: hermetic package on demonstrator board

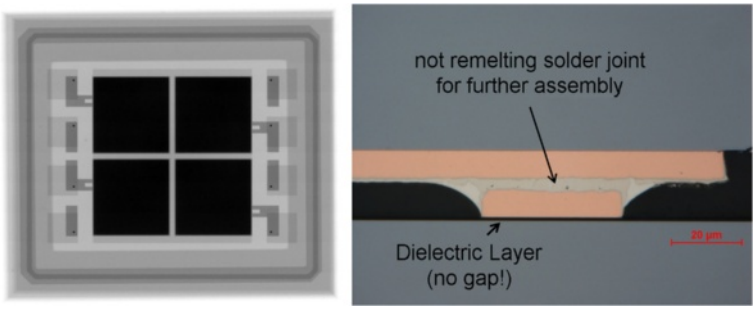

Fig. 21 Left: x-ray microscopy of hermetic package, right: cross section through the sealing ring

right). For those samples passed the initial leak test both following tests were always successful.

Further issues, like second level interconnect between package and board or phosphor coating without polymers, neither as matrix, nor as adhesive will be addressed in the follow-up project HeraKLED in the coming years using transparent ceramics [18].

Conclusions

By understanding available packaging technologies and development of an optimized process chain a very efficient LED module with high luminous flux, resistant against harsh environment can be built with high accuracy on wafer level.

Competing interests

The authors declared that they have no competing interests.

Authors' contributions

CW is responsible for sinter technology development. CE is doing his PhD on the topic of transient liquid phase soldering. MW is responsible for all wafer level technologies. JJ is expert for thermal and thermo mechanical simulations. RJ is managing the LED development activities. All authors read and approved the final manuscript.

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Acknowledgements

Part of this work has been funded within the "EnLight – Energy efficient and intelligent lighting systems" project by the ENIAC Joint Undertaking (project ID: 270707–2) and the German Federal Ministry of Education and Research (FKZ: 16 N11438, Subproject: Erforschung von Elektronikbausteinen für energieeffiziente, intelligente Beleuchtungssysteme).

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Received: 10 December 2014 Accepted: 21 May 2015
Published online: 06 June 2015

References

1. Teerstra et al. "Thermal Conductivity and Contact Resistance Measurements for adhesives". Vancouver, Canada: Proc. of InterPACK; 2007.
2. Wunderle B, Kleff J, May D, Abo Ras M, Schacht R, Oppermann H, et al. "In-situ measurement of various thin Bond-Line-Thickness Thermal Interface Materials with Correlation to Structural Features". Rome: Proc. 14th THERMINIC; 2008.
3. Wunderle B, Ras MA, Klein M, Mrossko R, Engelmann G, May D, et al. "Progress in thermal characterisation methods and thermal interface technology within the "Nanopack" project". Leuven, Belgium: THERMINIC 2009, 15th International Workshop on Thermal Investigations of ICs and Systems; 2009.
4. Abo Ras M, Wunderle B, May D, Schacht R, Winkler T, Rzepka S, et al. "technique for thermal characterization of thermal interface materials and substrates". Vol.2. Lake Buena Vista, Orlando, Florida, USA: ITherm; 2014.
5. Hutter M, Schmidt R, Zerrer P, Rauschenbach S, Wittke K, Scheel W, et al. "Effects of Additional Elements (Fe, Co, Al) on SnAgCu Solder Joints". San Diego: Electronic Components and Technology Conference; 2009. p. 26–9.
6. Hutter M, Ehrhardt C. "Grenzen und Möglichkeiten der Weichlotverbindungen – Betrachtung von Qualität und Zuverlässigkeit". Tagung Weichlöten 2015, Trends und Entwicklungsschwerpunkte in der Leistungselektronik, Hanau, 24. Und 25. März 2015, DVS-Berichte Band 310, ISBN 978-3-945023-37-2, 2015.
7. Wittler O, Walter H, Dudek R, Faust W, Jun W, Michel B. "Deformation and fatigue behavior of AuSn interconnects". Singapore, China: Proc. Electronic Packaging Technology Conference; 2006. p. 297–301.
8. Hutter M, Ehrhardt C, Oppermann H. "Interconnection Technologies for High Operating Temperatures". Micromaterials and Nanomaterials. 2011;13:46–51. ISSN 1619–2486.
9. Wunderle B, Klein M, Dietrich L, Abo Ras M, Mrossko R, May D, et al. "Advances in Thermal Interface Technology: Mono-Metal Interconnect Formation, Processing and Characterisation.". Las Vegas, USA: Proc. 10th Itherm Conf; 2010.
10. Weber C, Hutter M, Ehrhardt C, Oppermann H. "Riliability Testing of Ag Sinter Joints". Nuremberg, Germany: ECWC13 – 13th Electronic Circuits World Convention; 2014.
11. Weber C, Hutter M, Oppermann H, Lang K-D. "Microstructural and mechanical analyses of Ag sintered joints". Nuremberg, Germany: PCIM Europe; 2014.
12. Ehrhardt C, Hutter M, Hermann O, Lang K-D. "Transient Liquid Phase Soldering for lead-free joining of power electronic modules in high temperature applications". In: High Temperature Electronics Conference (HiTEC). 2012. p. 1–9.
13. Ehrhardt C, Hutter M, Oppermann H, Lang K-D. "Transient Liquid Phase Soldering – An emerging joining technique for power electronic devices". In: PCIM. 2013. p. 1–8.
14. Ehrhardt C, Hutter M, Oppermann H, Lang K-D. "Verbindungstechnologien für Baugruppen bei erhöhten Betriebstemperaturen" EBL. DVS/GMM. 2014;7:68–74.
15. Ehrhardt C, Hutter M, Oppermann H, Lang K. "A Lead Free Joining Technology for High Temperature Interconnects Using Transient Liquid Phase Soldering (TLPS)". ECTC. 2014;64:1321–7.
16. CEhrhardt C, Hutter M, Weber C, Goullon L, Oppermann H. "Verbindungstechniken für erhöhte Einsatztemperaturen mikroelektronischer Anwendungen": Microelectronic Packaging in the 21th century; Fraunhofer Verlag 2015. p. 194–9, ISBN: 978-3-8396-0826-5
17. Auersperg J, Dudek R, Jordan R, Bochow-Neß O, Rzepka S, Michel B. "On the crack and delamination risk optimization of a Si-interposer for LED packaging". Wroclaw, Poland: EuroSimE; 2013. p. 14–7.
18. Wätzig K, Kunzer M, Kinski I. "Influence of sample thickness and concentration of Ce dopant on the optical properties of YAG:Ce ceramic phosphors for white LEDs". J Mater Res. 2014;29(Nr.19):S.2318–24.
19. Abo Ras M, Wunderle B, May D, Oppermann H, Schacht R, Michel B. "Influences of technological processing and surface finishes on thermal behaviour of thermal interface materials" Thermal investigations of ICs and Systems. Barcelona, Spain: THERMINIC, 16th International Workshop; 2010.
20. McMullen MD, Kresovich S, Villeda HS, Bradbury P, Li H, Sun Q, et al. Genetic properties of the maize nested association mapping population. Science. 2009;325:737–40.