Hindawi Publishing Corporation
EURASIP Journal on Applied Signal Processing
Volume 2006, Article ID 41898, Pages 1–10
DOI 10.1155/ASP/2006/41898

Analogue MIMO Detection

Robert J. Piechocki,[1] Jose Soler-Garrido,[1] Darren McNamara,[2] and Joe McGeehan[1,2]

[1] *Centre for Communications Research, University of Bristol, Merchant Venturers Building, Woodland Road, Bristol BS8 1UB, UK*
[2] *Telecommunications Research Laboratory, Toshiba Research Europe Ltd, 32 Queen Square, Bristol BS1 4ND, UK*

Received 1 December 2004; Revised 17 May 2005; Accepted 8 July 2005

In this contribution we propose an analogue receiver that can perform turbo detection in MIMO systems. We present the case for a receiver that is built from nonlinear analogue devices, which perform detection in a "free-flow" network (no notion of iterations). This contribution can be viewed as an extension of analogue turbo decoder concepts to include MIMO detection. These first analogue implementations report reductions of few orders of magnitude in the number of required transistors and in consumed energy, and the same order of improvement in processing speed. It is anticipated that such analogue MIMO decoder could bring about the same advantages, when compared to traditional digital implementations.

1. INTRODUCTION

Turbo codes and more general turbo principles (turbo equalisation, turbo multiuser detection, etc.) are bound to have a substantial impact on the next-generation wireless systems. The turbo principle requires exchange of the so-called soft information, which is a probabilistic measure. In current implementations (e.g., turbo coding) this information is sampled then quantised (digitised) and handled by digital signal processors. The amount of digital information to be processed by DSPs and FPGAs is enormous and represent a "bottleneck" for high speed digital systems. However, the soft information, being analogue in nature, is best represented in analogue domain (e.g., electric currents or voltages). More interestingly, it can be processed in this form by analogue networks as well. The analogue decoding paradigm formulated in [1, 2] takes this stand.

First analogue implementations of binary decoders were reported in the literature in [3–5]. Those implementations reported reductions of 1–3 orders of magnitude in number of required transistors and in consumed energy, and the same order of improvement in processing speed. More ambitious CMOS-only implementation of analogue decoders was recently reported in [6, 7].

In truth, it was the neural networks community that first used analogue VLSI circuits to build simple artificial neural networks [8]. Both neural networks and communications engineering are by and large examples of computation, and as a result the fundamental building blocks are the same in both cases. Some fundamentals of analogue computations stem directly from the universal Turing machine paradigm worked out by Alan Turing nearly 70 years ago [9]. Subsequently, they were used in many versions of analogue and mixed-mode (micro-) processors built over the last few decades.

In this contribution we extend the concept of analogue detection and we attempt to layout multiple-input multiple-output (MIMO) analogue decoder. As aforementioned, the state-of-the-art implementations of analogue computation networks realise binary codes. Equalisation in analogue networks was envisaged in [10]. All are examples of probability propagation principle that can be achieved using simple sum-product algorithm. In this contribution we will also be exchanging probabilities, which can be viewed as a form of sum-product algorithm.

The proposed analogue MIMO decoder calculates sets of marginal posterior probabilities (MPPs). The major idea may be conveyed in Figure 1. The mesh represents support for the joint posterior distribution. Each dot in the figure represents a possibility from a finite number of combinations. The thicker dots correspond to the possibilities with higher posterior probabilities. The thick dots on the lines along the axis represent the MPPs of interest. The only way to calculate the exact MPPs in a MIMO system is to enumerate over the joint posterior probability, and then marginalise out. Marginalisation over discrete sets amounts to repeated summations. By Kirchhoff's current law, analogue summation can easily be achieved, and the speed improvement is due to fully parallel manner in which calculations of the joint posterior probability and marginalisation occur. We concentrate on analogue implementations and do not deal with solutions of the digital-to-analogue and analogue-to-digital conversions.

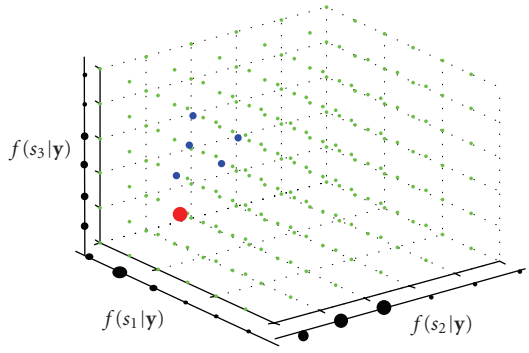


Figure 1: Joint posterior and marginal posterior probabilities in a MIMO system.

The paper is organised as follows. Section 2 describes the studied system and the detection aims. In Section 3 we review basics of the transistor physics and we make a connection with a probabilistic detection. Sections 4 and 5 describe details of analogue implementations of the channel and MIMO decoders, respectively. Section 6 presents SPICE simulation results, and in Section 7 we draw conclusions.

2. SYSTEM DESCRIPTION AND DETECTION AIMS

The object of our study is a MIMO system. The system communicates N bits $b_n, b_n \in \{0,1\}$. The stream of bits is first encoded to $K > N$ coded bits, $c_k, c_k \in \{0,1\}$, interleaved (a random permutation) $\pi, c_{\pi(k)} = \pi(c_k)$. We assume that modulation and encoding onto N_T transmit antennas take place in one operation, space-time modulation encoding, where $D = N_T \log_2(M)$ portion of coded bits $c_{\pi(k)}$ (M is cardinality of the digital modulation; D is a total number of bits transmitted in one time instant). We will assume the simplest form of space-time signalling, essentially a serial-to-parallel converter, which is known as BLAST (spatial-multiplexing) [11]. The resulting $(N_T \times 1)$-dimensional vector $\mathbf{x} = (x_1, \ldots, x_{N_T})^T$ is transmitted from all N_T antennas at a time instant t. We will assume that the signal is transmitted over a narrowband channel $\mathbf{H}$ of size $N_R \times N_T$, where each entry $h_{j,i}$ defines a channel connecting ith transmit with jth receive antenna. The system is conventionally modelled as

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n}, \tag{1}$$

where $\mathbf{y}$ is the receive $N_R \times 1$ vector and $\mathbf{n}$ is the ubiquitous white Gaussian noise, that is, $\mathbf{n} \sim \mathcal{CN}(\mathbf{0}, \sigma_n^2 \mathbf{I})$. Typically, it is assumed that $h_{j,i}$ are i.i.d. random variables $h_{j,i} \sim \mathcal{CN}(\mathbf{0}, 1)$; however this is not required here, except that $h_{j,i}$ should be known to the receiver. The ultimate goal is to detect the transmitted information bits given the received signal and the channel. To be more specific we are looking for a set of point estimates that maximise the set of marginal posterior distributions: $\{f(b_1 \mid \mathbf{y}_{1:T}, \mathbf{H}), \ldots, f(b_N \mid \mathbf{y}_{1:T}, \mathbf{H})\}$ (i.e., maximum a posteriori estimates (MAP)), where $1 : T$ is a Matlab notation for a set $\{1, 2, \ldots, T\}$. In general, this task is computationally not tractable, and instead it is conventional to use a suboptimal procedure, so-called turbo detection. The resulting system with such detector is known as TurboBLAST (turbo spatial multiplexing). More details on many aspects of MIMO can be found, for example, in [11]. Essentially, the turbo detection is an iterative process where the so-called soft MIMO detector computes, for each time instant t, $\{f(x_1 \mid \mathbf{y}_t, \mathbf{H}), \ldots, f(x_{N_T} \mid \mathbf{y}_t, \mathbf{H})\}$, and the soft binary channel decoder computes $\{f(b_1 \mid c_{1:K}), \ldots, f(b_N \mid c_{1:K})\}$.

The main aim of this contribution is to discuss how those tasks can be carried out in the analogue circuits. Since the detection of binary codes using analogue VLSI has been described in the aforementioned references, we will concentrate on the MIMO detection block. The MPPs of interest are calculated as follows:

$$f(x_i \mid \mathbf{y}) = \sum_{x_{-i}} f(x_{1:N_T} \mid \mathbf{y}) \propto \sum_{x_{-i}} f(\mathbf{y} \mid x_{1:N_T}) f(x_{1:N_T}), \tag{2}$$

where x_{-i} is a shorthand for $\{x_1, \ldots, x_{i-1}, x_{i+1}, \ldots, x_{N_T}\}$, that is, "all except i." The observations are independent given the symbols and it is reasonable to assume that the extrinsic information (which becomes the prior for the decoder) is also separable, that is,

$$f(x_i \mid \mathbf{y}) \propto \sum_{x_{-i}} \prod_{j=1}^{N_R} f(y_j \mid x_{1:N_T}) \prod_{i=1}^{N_T} f(x_i). \tag{3}$$

In general any further simplifications (i.e., factorisations) are not possible. If one wants to calculate any marginal, the only way is to calculate the joint posterior distribution and marginalise out the variables (i.e., no message-passing tricks would help). Given our assumption about the noise, the likelihood is Gaussian:

$$f(y_j \mid x_{1:N_T}) \propto \exp\left(-\frac{1}{\sigma_n^2} \left| y_j - \mathbf{h}_{i,:}^T \mathbf{x} \right|^2\right). \tag{4}$$

All operations in (4) can be carried out explicitly in the analogue domain. In this paper we opt for an alternative approach that also computes the exact values of the marginals of interests. Arguably, this will lead to a simpler implementation of at least the analogue part of the MIMO decoder. First, we assume that the digital part of the receiver calculates the QR decomposition of the channel matrix, that is, $\mathbf{H} = \mathbf{QR}$, where $\mathbf{R}$ is upper triangular and $\mathbf{Q}^H\mathbf{Q} = \mathbf{I}$. Left multiplication of the received signal by $\mathbf{Q}$ produces a signal model:

$$\widetilde{\mathbf{y}} = \mathbf{R}\mathbf{x} + \widetilde{\mathbf{n}} \tag{5}$$

(note that the noise statistics do not change). However, the analogue layout of the decoder is different since our model is now causal ($\mathbf{R}$ is triangular). (The QR decomposition has been used in the past with various MIMO detectors.) The

decomposition now looks as

$$f(x_i \mid \mathbf{y}) \propto \sum_{x_{-i}} \prod_{j=1}^{N_R} f(y_j \mid x_{1:j}) \prod_{i=1}^{N_T} f(x_i). \tag{6}$$

For example, in the case of a 3×3 MIMO system the likelihood factors as

$$\begin{aligned} &f(y_1, y_2, y_3 \mid x_1, x_2, x_3) \\ &\quad = f(y_1 \mid x_1) f(y_2 \mid x_1, x_2) f(y_3 \mid x_1, x_2, x_3). \end{aligned} \tag{7}$$

Notice that when implemented in the digital domain there is no real difference between the two approaches, as both boil down to enumerating entire state space of the joint distribution and marginalisation in the second step.

3. TRANSISTOR PHYSICS AND PROBABILISTIC DETECTION

The concept of shifting some of the decoding tasks (typically carried out in the digital domain) to the analogue world stems largely from an excellent match between transistor physics and probabilistic decoding operations. Indeed, the natural and easy way in which probability calculations can be mapped into analogue networks makes us think that transistors actually "like" to work with probabilities. In fact, the nonlinear properties of these devices, far from representing a problem, can be exploited to perform complex operations by using simple well-known analogue structures. Those connections have been previously pointed out in [2, 3, 10].

One example of a nonlinear characteristic is given by the properties of the current flowing across the collector I_C of a bipolar transistor, which is given by

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right), \tag{8}$$

where I_S is the saturation current, V_T is the thermal voltage, and V_{BE} is the voltage difference between the base and the emitter. Perhaps the simplest arrangement of two transistors is a differential pair; see Figure 2.

From (8) we can obtain the currents flowing across both transistors: $I_1 = I_S \exp((V_1 - V)/V_T)$ and $I_2 = I_S \exp((V_2 - V)/V_T)$, $(\Delta V = V_2 - V_1)$;

$$\begin{aligned} \frac{I_1}{I} &= \frac{I_S \exp\left((V_1 - V)/V_T\right)}{I_S\left(\exp\left((V_1 - V)/V_T\right) + \exp\left((V_2 - V)/V_T\right)\right)} \\ &= \frac{1}{1 + \exp\left(\Delta V/V_T\right)}, \\ \frac{I_2}{I} &= \frac{I_S \exp\left((V_2 - V)/V_T\right)}{I_S\left(\exp\left((V_1 - V)/V_T\right) + \exp\left((V_2 - V)/V_T\right)\right)} \\ &= \frac{\exp\left(\Delta V/V_T\right)}{1 + \exp\left(\Delta V/V_T\right)}. \end{aligned} \tag{9}$$

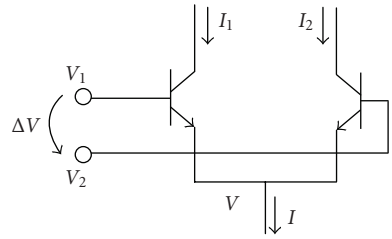


Figure 2: Bipolar differential pair.

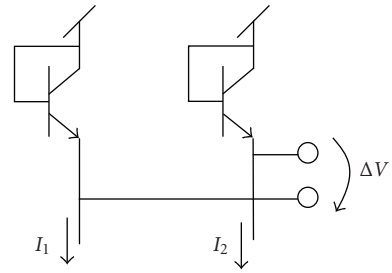


Figure 3: Diode-connected transistor pair.

Those expressions can be readily recognised as conversions between the so-called L-values (logarithm of a ratio of probabilities or likelihoods) and probabilities/likelihoods, by associating $L(x) = \Delta V/V_T$ and $P(x_i) = I_i/I$. The reciprocal transformation is also achievable with just two transistors connected in a diode configuration (Figure 3). The difference of voltage between the two emitters is $V_{BE1} = V_T \log(I_1/I_S)$ and $V_{BE2} = V_T \log(I_2/I_S)$, hence $\Delta V = V_{BE1} - V_{BE2} = V_T \log(I_1/I_2)$.

Another very useful operation is obtained by comparing the difference of currents in the differential pair of Figure 2:

$$\begin{aligned} I_1 - I_2 &= I\left(\frac{\exp\left(\Delta V/V_T\right)}{1 + \exp\left(\Delta V/V_T\right)} - \frac{1}{1 + \exp\left(\Delta V/V_T\right)}\right) \\ &= I\left(\frac{\exp\left(\Delta V/2V_T\right) - \exp\left(-\Delta V/2V_T\right)}{\exp\left(\Delta V/2V_T\right) + \exp\left(-\Delta V/2V_T\right)}\right) \\ &= I \tanh\left(\frac{\Delta V}{2V_T}\right). \end{aligned} \tag{10}$$

The above operation is indeed very useful, since a posterior expectation of a binary random variable (in AWGN channel) is given by a hyperbolic tangent, that is, $E_{X|Y}\{X\} = \tanh((1/\sigma_n^2)y)$.

4. ANALOGUE IMPLEMENTATION OF A LOW-DENSITY PARITY-CHECK CHANNEL DECODER

This work is concerned with an analogue implementation of a MIMO decoder. However, a channel decoder will typically

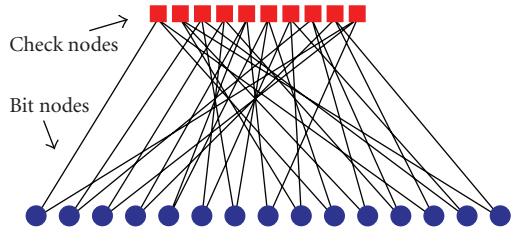


Figure 4: Bipartite graph of the LDPC rate-6/15 code.

be an integral part of a MIMO system. It should be clear that it makes perfect sense to implement both the MIMO and the channel decoder operations in one analogue circuitry. In this section we outline the design of an analogue Low-Density Parity-Check (LDPC) decoder.

The code of choice is a LDPC code of rate 6/15. This is a very short length code for a LDPC code, whose parity-check matrix is not really "low density." However we will keep referring to it as a LDPC code for the clarity of presentation. LDPC codes are conveniently described by bipartite graphs. A bipartite graph represents pictorially the parity-check matrix of a LDPC code. It is also useful in the detection, since the sum-product algorithm operations can be described on such graph; see, for example, [12]. The bipartite graph of the chosen 6/15 code is shown in Figure 4. The layout of the analogue decoder for this code is shown in Figure 5. The squares in Figure 5 are the check-node analogue processors and the circles are the bit-node analogue processors. It is basically an unfolded version of the bipartite graph. All operations within the check and bit nodes are performed in the voltage-domain. For further details of implementation of similar binary decoders and a discussion on current/voltage-domain implementation trade-offs, we refer to an excellent monograph [3].

Figure 6 depicts a response of the analogue decoder and outputs of "digitally implemented" sum-product algorithm with a high level of noise ($E_b/N_0 = 0\,\text{dB}$) for a given received sequence. In this case, the iteration-based (digital) and the analogue decoder give amazingly similar results. Figure 6 shows actually a close-up of the first microseconds of the analogue response and the first iterations of the digital one to illustrate how the error correction is performed mainly at these first steps of the decoding process. The message sent was 001100, encoded as 111110100001100. However, the received values would be initially hard decoded as 001010 (i.e., with errors in the bits 4 and 5). Considering the digital decoder, the two errors are corrected in the first and third iterations, respectively, while with the analogue decoder they are corrected after a transient of 0.99 and 1.87 microseconds. Both responses are incredibly similar, almost as if the L-values at each iteration of the digital decoder were the sampled points of the contiguous time waveforms of the analogue decoder. This, however, is just a mere observation and it is presented here more as a curiosity and not as a result.

5. ANALOGUE IMPLEMENTATION DETAILS OF THE MIMO A POSTERIORI PROBABILITY DECODER

As indicated in (4), the fundamental operations required to be implemented are multiplication, summation, and negative exponential function, that is, $\exp(-x)$. In this section we discuss how those basic blocks can be implemented in analogue circuits.

5.1. Multiplier

The most important function that has to be implemented with analogue circuits is multiplication of two input voltages, both of which can be positive or negative. A four-quadrant multiplier circuit is therefore needed to achieve this. This basic block is used most often in the analogue MIMO detector. The Gilbert multiplier circuit [8] performs multiplication using the output from a differential pair as the input for another two differential pairs; see Figure 7. The circuit is arranged in such a way that the output current is given by the combination of all four upper currents:

$$\begin{aligned}&(I_{13}+I_{24})-(I_{14}+I_{23})\\&\quad=I_b\tanh\frac{k(V_1-V_2)}{2}\tanh\frac{k(V_3-V_4)}{2}.\end{aligned}\tag{11}$$

The output current and voltage of the Gilbert multiplier follow a $\tanh(x)$ rule, which for small input voltage differences can be approximated by $\tanh(x)\approx x$. Additionally, this basic circuit has a limitation on the inputs: $\max(V_3,V_4) > \min(V_1,V_2)$.

Multiplication is typically performed on random voltages. Hence, it is difficult to make any assumptions about the range of the input signals. A wide-range multiplier [8] is required in order to ensure that the circuit works properly for both high and low input voltage levels. One possible choice is the wide-range Gilbert multiplier circuit, shown in Figure 8. The wide-range multiplier isolates the bottom differential pair from the upper differential pairs using current mirrors. This allows the range of V_3 and V_4 to be independent of V_1 and V_2 allowing the circuit to work properly for input voltages close to the supply voltage. The SPICE simulated output of the wide-range Gilbert multiplier is shown in Figure 9. The figure shows V_{out} as a function of V_1, for different choices of V_2. The observed voltage is closely approximated by $\Delta V_{\text{out}} = V_1V_2/V_{\text{ref}}$ (with $V_{\text{ref}} = 10\,\text{mV}$). For high input values the $\tanh(x)$ behaviour starts being noticed, degrading the output characteristic of the circuit. For moderate input values, up to 30–60 mV, the linearity is high enough to multiply the two inputs with great accuracy.

5.2. Summation

The summation operation is most conveniently performed in the current domain. By Kirchhoff's current law, it is

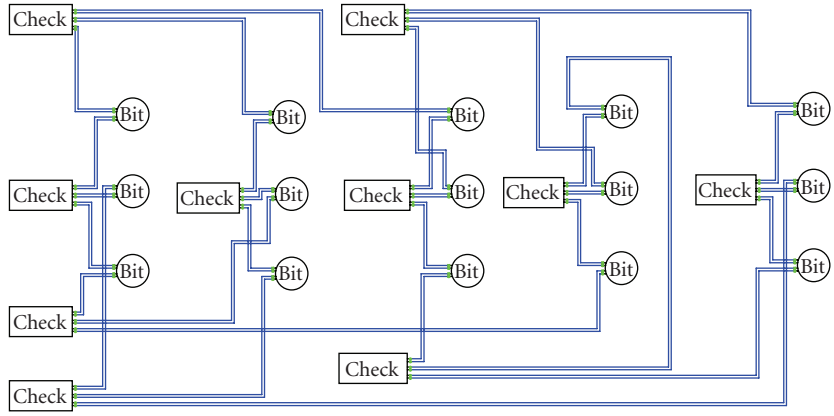
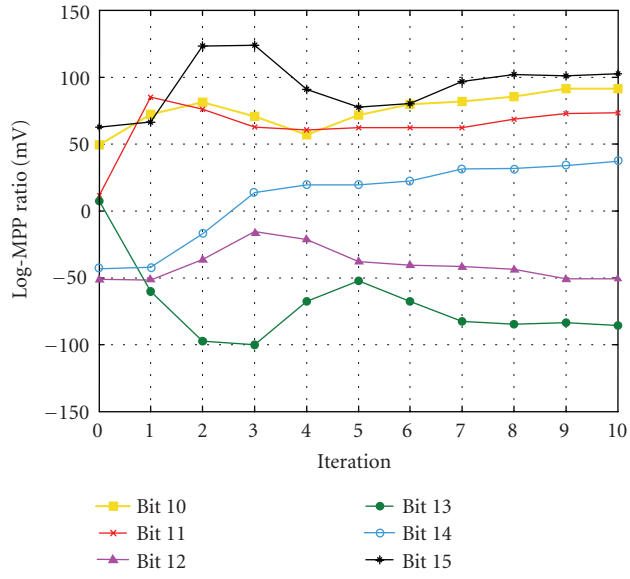
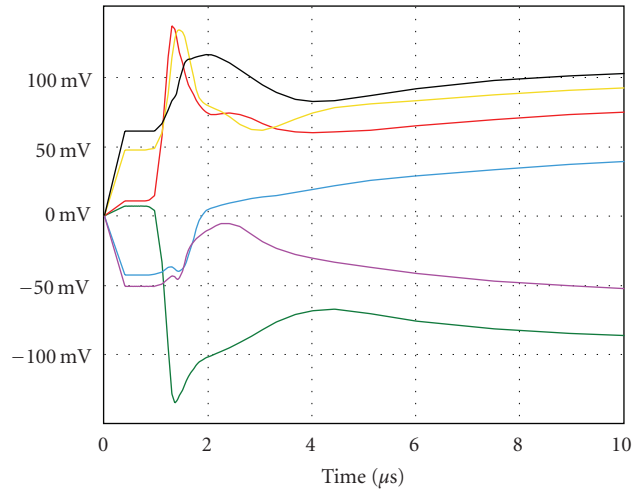


Figure 5: Layout of the analogue LDPC code decoder.



(a)



(b)

Figure 6: (a) Beliefs' values at the output of digital decoder, and (b) the equivalent waveforms of the analogue decoder, (LDPC 6×15).

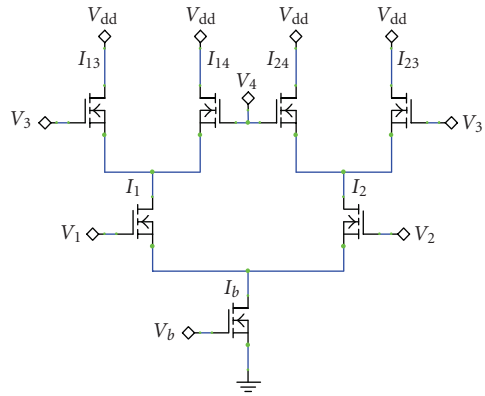


Figure 7: Gilbert multiplier basic cell.

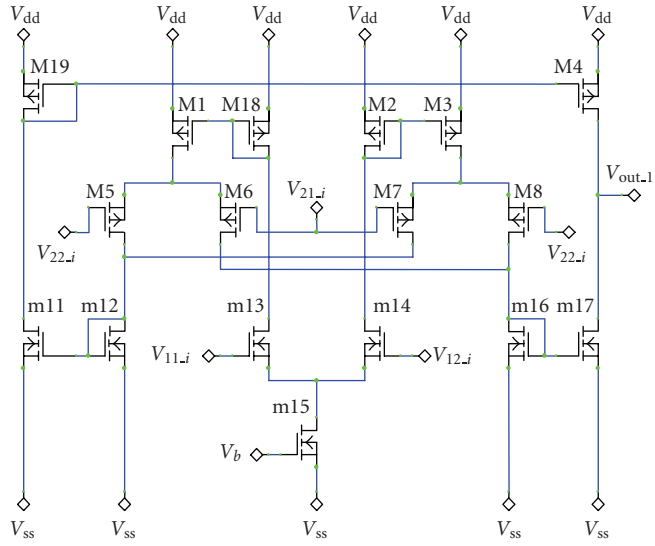


Figure 8: Wide-range Gilbert multiplier.

enough just to connect the wires in a node. Indeed, such summers are used in the MIMO decoder in the "marginaliser" block. A voltage summation is also required to avoid excessive number of voltage-current-voltage transformations. A circuit [13] capable of performing voltage summation is shown in Figure 10. By simple analysis of the circuit, the output voltage can be obtained as a function of the gate-source voltages of the transistors [13]:

$$\begin{aligned}\Delta V_{OS} &= \sqrt{\frac{(W/L)_1}{(W/L)_2}}\left((V_{GS1} - V_{GS2}) + (V_{GS3} - V_{GS4})\right)\\ &= \sqrt{\frac{(W/L)_1}{(W/L)_2}}(\Delta V_1 + \Delta V_2),\\ \Delta V_{OS} &= V_{O1} - V_{O2}, \qquad \Delta V_1 = V_{11} - V_{12},\\ \Delta V_2 &= V_{21} - V_{22},\end{aligned} \tag{12}$$

where W and L are the width and length of a transistor respectively. Figure 11 shows the simulated response for $(W/L)_1 = (W/L)_2$ ($W = 16\,\mu$ and $L = 1.6\,\mu$).

5.3. Negative exponential

The last building block needed to implement the analogue MIMO detector is a circuit with a negative exponential response in the voltage domain, that is,

$$\Delta V_{\text{out}} = K V_{\text{ref}} \exp\left(-\frac{\Delta V_{\text{in}}}{V_{\text{ref}}}\right), \tag{13}$$

where V_{ref} is a reference voltage, ΔV_{in} and ΔV_{out} are the input and output differential voltages, respectively, and K is a normalisation constant that has no effect on the response of the system, since we are using this block to obtain the elements of a probability density function. To keep the transistor count as

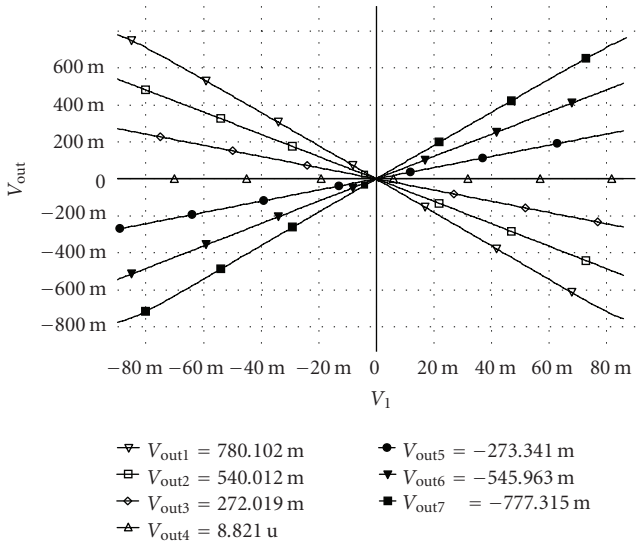


Figure 9: Output characteristics of the wide-range Gilbert multiplier. The plots correspond to the second input set at ±90 mV, ±60 mV, ±30 mV, and 0 V.

low as possible we use a simple approximation for the negative exponential function. A simplified equation for the drain current through a saturated nMOS transistor in the strong inversion region is

$$I_D = \frac{K}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2, \tag{14}$$

where K is a technology-dependent factor, W and L are width and length of the transistor, V_{GS} is the gate-source voltage applied, and V_T is the threshold voltage. We can approximate the negative exponential by a function of the type $f(x) = A - B\sqrt{x}$ using a single transistor fed with a current I_d that we obtain from a transconductance stage. For small input values such approximation is good enough for our purposes. However, if the input grows bigger, the approximation function can become negative where the true exponential would not. Therefore, it is required to clip the output voltage to ensure it never becomes negative. The final circuit is depicted in Figure 12. Transistors M9—M17 form a transconductance amplifier [8] that converts the input voltage into a current. This current is passed to a transistor M1 that performs the approximation function. Transistors M2 and M3 restrict the output to positive values, and finally, M4–M8 are used to shift the output voltage to an adequate level for interconnection with other building blocks.

Figure 13 depicts simulation results of this circuit. The ideal response shown corresponds to (13) with $K = 1.8$ and $V_{\text{ref}} = 10\,\text{mV}$. The thick line is the error between the ideal response and the approximation.

The one remaining operation $|x|^2$ is simply achieved by a four-quadrant multiplier realising $x \cdot x$.

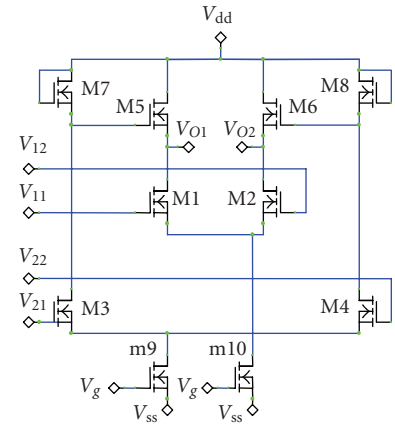


Figure 10: Voltage differential adder circuit.

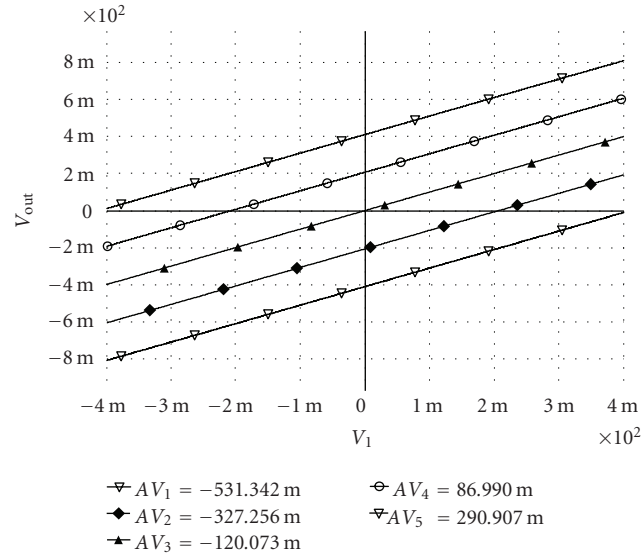


Figure 11: Output characteristics of the differential adder circuit. The plots correspond to the second input set at ±400 mV, ±200 mV and 0 V.

6. ANALOGUE MIMO DECODER EXAMPLE AND RESULTS

We have simulated in the SPICE software an analogue MIMO decoder with 3 transmit and 3 receive antennas. All transistor models used here are basic models (standard BSIM 3v3 MOS model) supplied with nearly all SPICE software packages. A BPSK modulation was assumed. Six bits of data are encoded to 15 (coded) bits by the LDPC code of Section 4. The MIMO decoder consists of 5 identical modules, each providing MPPs for 3 coded bits. The outputs of the MIMO decoder are wired directly to the analogue LDPC decoder. One of the modules is presented in Figure 14. The layout of the module corresponds to a factor graph that describes (6) for the case of $N_T = 3$, that is, (7). Each of the square

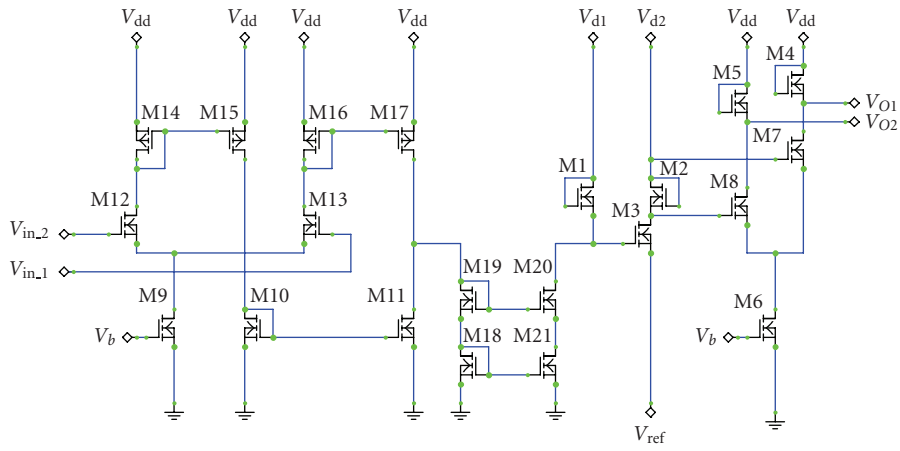


Figure 12: Block diagram of the negative exponential MOS circuit.

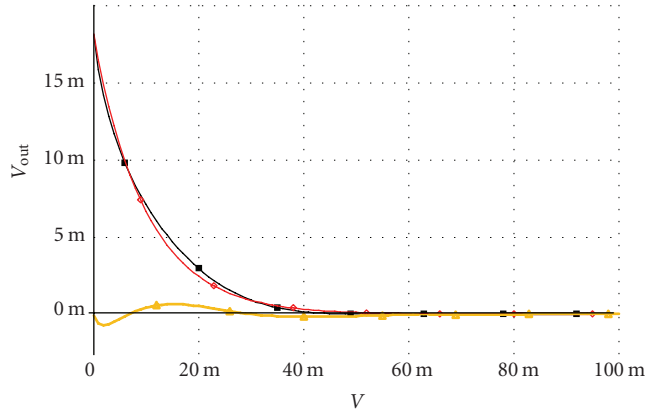


Figure 13: Output characteristic obtained from SPICE and the ideal response.

blocks performs analogue computations corresponding to (4).

The outputs of the modules are fed to the marginaliser block. The marginaliser consists of triple output cascode current mirrors and appropriately connected wires to obtain current summations. Table 1 depicts results of a comparison between the analogue LDPC decoder and a standard sum-product detection (software simulation of a digital decoder). An error is defined as a difference in posterior probability estimates of a given bit being zero, that is, Error $= \Pr_{\mathrm{APP}}(b = 0) - \Pr_{Analogue}(b = 0)$. A great accuracy of the analogue decoder can be observed. Table 2 depicts comparison results between the analogue MIMO decoder and a simulated exact a prosteriori probability (APP) MIMO decoder (full enumeration without any approximations). A good accuracy of analogue MIMO decoder can be observed, albeit inferior to that of the LDPC decoder. The inaccuracies are introduced mainly by the approximation in the exponential function and variations in the currents due to the non-ideal behaviour of the transistors.

7. CONCLUSIONS

In this contribution we have proposed an analogue detector for a MIMO system. It is expected that such decoder will offer similar advantages to those reported by analogue binary decoders, that is, significant improvements in processing speed, reduction in transistor count, power efficiency, and heat dissipation. On the downside, since the decoder mimics the full complexity APP decoder (albeit very efficiently), the transistor count (not the processing speed) increases exponentially. Such MIMO decoder may still be feasible for a MIMO system with small number of transmit antennas and simple modulation formats. However, one of the major challenges seems to be the design of reduced-complexity high-performance algorithms that could be executed in analogue VLSI networks.

It is very difficult to envisage modern receivers completely deprived of DSP/FPGAs. Wireless receivers perform many other logical operations (apart from the detection) that can efficiently be executed only in software programmable processors. Therefore, a reasonable approach

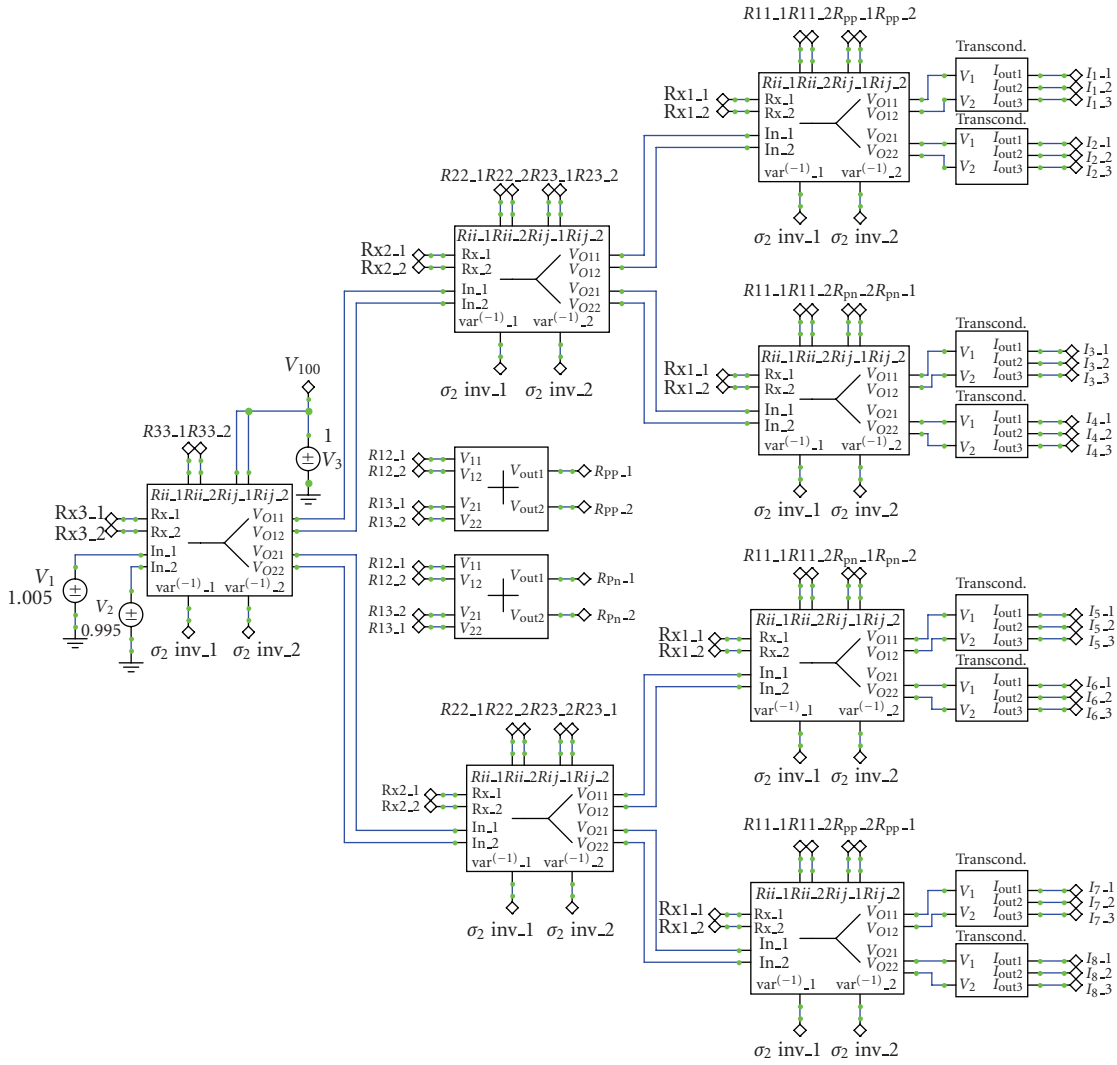


Figure 14: Layout of the basic module of the analogue APP MIMO decoder.

Table 1: Analogue LDPC decoder comparison results.

E_b/N_0 (dB)	Mean (absolute value (error))	Variance (error)
0	2.90e −03	5.92e −05
1	5.00e −03	1.86e −04
2	4.90e −04	1.24e −05
3	1.08e −08	2.36e −15
5	2.91e −09	1.62e −16
7	4.37e −10	1.07e −17

Table 2: Analogue MIMO decoder comparison results.

E_b/N_0 (dB)	Mean (absolute value (error))	Variance (error)
0	0.020 60	0.000 86
1	0.026 50	0.001 50
2	0.020 90	0.001 10
3	0.018 20	0.000 95
5	0.014 20	0.000 73
7	0.012 70	0.000 93
9	0.013 00	0.001 30

would be a mixed-mode architecture, where the analogue decoder would act as a highly specialised and very efficient "subcontractor," that is, a coprocessor working together with a digital main processor. At the very least, in this paper we have shown that such architecture deserves further research as it may offer substantial benefits.

ACKNOWLEDGMENT

R. Piechocki and J. Garrido would like to thank Toshiba TRL Ltd for sponsoring their research activities.

REFERENCES

[1] H.-A. Loeliger, F. Lustenberger, M. Helfenstein, and F. Tarkoy, "Probability propagation and decoding in analog VLSI," in *Proceedings of IEEE International Symposium on Information Theory (ISIT '98)*, pp. 146–146, Cambridge, Mass, USA, August 1998.

[2] J. Hagenauer and M. Winklhofer, "The analog decoder," in *Proceedings of IEEE International Symposium on Information Theory (ISIT '98)*, pp. 145–145, Cambridge, Mass, USA, August 1998.

[3] F. Lustenberger, *On the design of analog iterative VLSI decoders,* vol. 2 of *Series in Signal and Information Processing*, Hartung-Gorre, Konstanz, Germany, 2000, Ph.D. dissertation.

[4] A. Xotta, D. Vogrig, A. Gerosa, et al., "An all-analog CMOS implementation of a turbo decoder for hard-disk drive read channels," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS '02)*, vol. 5, pp. 69–72, Scottsdale, Ariz, USA, May 2002.

[5] A. F. Mondragon-Torres, E. Sanchez-Sinencio, and K. R. Narayanan, "Floating-gate analog implementation of the additive soft-input soft-output decoding algorithm," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 50, no. 10, pp. 1256–1269, 2003.

[6] V. C. Gaudet and P. G. Gulak, "A 13.3-Mb/s 0.35-μm CMOS analog turbo decoder IC with a configurable interleaver," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 11, pp. 2010–2015, 2003.

[7] C. Winstead, J. Dai, S. Yu, C. Myers, R. R. Harrison, and C. Schlegel, "CMOS analog MAP decoder for (8,4) Hamming code," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 122–131, 2004.

[8] C. Mead, *Analog VLSI and Neural Systems*, Addison-Wesley, Reading, Mass, USA, 1989.

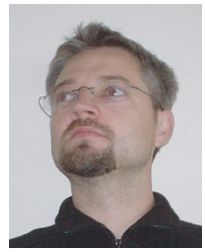
[9] R. Herken, Ed., *The Universal Turing Machine: A Half-Century Survey*, Oxford University Press, Oxford, UK, 1988.

[10] J. Hagenauer, E. Offer, C. Measson, and M. Moerz, "Decoding and equalization with analog non-linear networks," *European Transactions on Telecommunications*, vol. 10, pp. 659–680, 1999.

[11] A. Paulraj, R. Nabar, and D. Gore, *Introduction to Space-Time Wireless Communications*, Cambridge University Press, Cambridge, UK, 2003.

[12] S. Haykin, *Communication Systems*, John Wiley & Sons, Chichester, West Sussex, UK, 4th edition, 2001.

[13] J. S. Pena-Finol and J. A. Connelly, "A MOS four-quadrant analog multiplier using the quarter-square technique," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 1064–1073, 1987.



Robert J. Piechocki received his M.S. degree from the Technical University of Wroclaw, Poland, in 1997 and his Ph.D. degree from the University of Bristol in 2002, both in electrical engineering. He is currently a Research Fellow at the Centre for Communications Research, University of Bristol. His research interests lie in the areas of statistical signal processing for communications and radio channel modelling for wireless systems.

Jose Soler-Garrido received the Telecommunications Engineer degree from the Polytechnic University of Valencia, Spain, in 2004. Currently he is pursuing his Ph.D. degree in the Department of Electrical and Electronic Engineering, University of Bristol, UK. His main research interests include analogue VLSI design for detection/decoding and MIMO wireless systems.

Darren McNamara received the M. Eng. degree in electrical and electronic engineering from the University of Bristol, UK, in 1999. During this period he was sponsored by Racal Radio Ltd, where he followed their graduate training programme and worked on wireless communication systems. In 2003 he received the Ph.D. degree, also from the University of Bristol, in the area of MIMO channel measurement and analysis. Since November 2002 he has been with the Toshiba Telecommunications Research Laboratory in Bristol, UK.

Joe McGeehan received the B. Eng. and Ph.D. degrees in electrical and electronic engineering from the University of Liverpool, UK, in 1967 and 1971, respectively. He is presently a Professor of communications engineering and Director of the Centre for Communications Research at the University of Bristol. He is concurrently the Managing Director of Toshiba Research Europe Limited: Telecommunications Research Laboratory (Bristol). He has been actively researching spectrum-efficient mobile radio communication systems since 1973, and has pioneered work in many areas including linear modulation, linearised power amplifiers, smart antennas, propagation modelling/prediction using ray tracing and phase-locked loops. Professor McGeehan is a Fellow of the Royal Academy of Engineering and a Fellow of the Institute of Electrical Engineers. He was the joint recipient of the IEEE Vehicular Technology Transactions "Neal Shepherd Memorial Award" (for work on smart antennas) and the IEE Proceedings Mountbatten Premium (for work on satellite tracking and frequency control systems). In 2003, he was awarded the degree of D. Eng. from the University of Liverpool for his significant contribution to the field of mobile communications research, and in June 2004, was made a Commander of the Order of the British Empire (CBE) in the Queen's Birthday Honours List for services to the communications industry.