To the Issue of the Memristor's HRS and LRS States Degradation and Data Retention Time

A. V. Fadeev^{a, *} and K. V. Rudenko^{a, **}

^a Valiev Institute of Physics and Technology, Russian Academy of Sciences, Moscow, 117218 Russia

*e-mail: AlexVFadeev@gmail.com

**e-mail: rudenko@ftian.ru

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Abstract—In this review of experimental studies, the retention time and endurance of memristor RRAM memory elements based on reversible resistive switching in oxide dielectrics are studied. The influence of external parameters—switching pulses and ambient temperature—as well as internal factors—evolution of the concentration of oxygen vacancies in the filament region, the material, structure; the thickness of the active dielectric layer, material of metal electrodes on the long-term stability of high resistance state (HRS) and the low resistance state (LRS) of the memristor is discussed.

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INTRODUCTION

Due to the promising prospects for the construction of nonvolatile memory ICs of terabit capacity and applications for neuromorphic computing [1], the number of studies in the field of memory devices based on resistive switching in dielectrics has grown exponentially. Memory cells based on the storage of electric charge have approached the physical limits of scaling due to the lack of ideal dielectrics, limiting current leakage through structural defects, and tunneling effects. In contrast, in memory cells based on resistive switching mechanisms (ReRAM), an ideal dielectric is not needed, but the structure of its local defect regions have to be limited to the nanoscale. The cationic-anionic charge transport in this region under the influence of an external electric field leads to a local and reversible change in the structural defects of the dielectric, which is externally expressed in stepwise changes in the conductivity of the cell and resistive switching between its states with high resistance (HRS or RESET state) and low resistance (LRS or SET state). These states are established after exposure to a switching pulse of a certain polarity, duration, and amplitude. In the absence of external electric fields, an ideal memristor (a resistor with memory) is able to maintain the HRS and LRS for as long as desired with the fixed value of the electrical resistance of the cell. Thus, a bit of information in the memristor memory cell is stored in the form of structural changes in the local region of the dielectric enclosed between the two conducting electrodes. Memristors with only two levels of electrical resistance (one-bit), integrated into the cross-bar architecture [2–6], and in 3D configura-

tions [7, 8], represent the foundation for future ultralarge integrated circuits of fast nonvolatile memory ReRAM with a long retention time. At the same time, multilevel (multibit) memristors with a set of intermediate discrete levels of electrical resistance of the cells (from 4 to 20) [9–17] offer the possibility of creating systems with a parallel computing mechanism and synaptic plasticity function, which is necessary for constructing recurrent neural networks and next generation artificial intelligence architectures [18–21].

Unipolar [16, 12] and bipolar [23–25] switching between the HRS and LRS is possible. In unipolar devices, switching between resistive states is carried out by the voltage pulses of the same polarity but of different amplitudes. In bipolar memristors, in order to change the cell states, it is necessary to reverse the polarity of the applied pulse [26]. In the mode of reading the HRS and LRS, small measuring voltage pulses are used that do not lead to switching between memristor states, but their parameters require careful analysis in terms of a possible cumulative long-term effect.

Different designs and structures of resistive cells can have different switching mechanisms. For example, in a number of memristors, the resistance value of the HRS and LRS depends on the contact area [27–29]. This may be due to both the drift-trap mechanism of charge carriers [27, 29] and the formation of multiple filaments [28]. The advantage of devices of the first type is lower power consumption, but at the same time they have a worse HRS/LRS ratio and a lower switching speed. In addition, they have significantly poorer prospects for scaling in high-density integrated cir-

Fig. 1. Diagram of a memristor cell in a highly conductive (a, b) and low-conductive (c, d) states. For asymmetrical (a, c) and symmetrical (b, d) cases.

cuits. Devices of the second type can be used as multi-bit devices.

For systems with a high degree of integration, cell structures that are analyzed further, where the entire area of the metal-dielectric interface is not involved in the process of resistive switching and the sharp change in the electrical resistance is due to the formation of one or several electrically conductive filaments of a sub-10-nm thickness of the filaments, which are more promising (Fig. 1).

The formation of filaments in dielectric layers was observed experimentally in [30–32]. Filament-type cells are characterized by a high switching rate and a high HRS/LRS resistance ratio, and are currently most widely studied [33, 34]. Filamentary memristors, in turn, are subdivided into those in which switching is based on the movement of oxygen anions (charged oxygen vacancies) [4, 35–37] and those in which the conducting filament is formed by metal cations (Ag, Ni, Cu) [11, 20, 38, 39].

Memristors, based in principle on the transport of anions, must contain an excessive amount of vacancies (usually oxygen vacancies in oxide dielectrics). An excess concentration of vacancies can be obtained by (i) choosing a nonstoichiometric metal oxide as an active medium, (ii) using an oxidizing metal as an electrode in contact with a dielectric, or (iii) using multilayer composite dielectrics as a vacancy generator. In the last two cases, nonstoichiometric regions are created at the interfaces of the layers: reservoirs of oxygen vacancies.

There are also structures of memristors, where the switching process includes the transport of both oxygen ions and metal cations [2, 27, 40–43] simultaneously. For example, the movement of Ta cations was observed in the Ta/HfO₂/Pt anionic memristor [11]. Even atoms of chemically inert electrodes, such as Pd in Pd/AlO_x/Pd [35], or Pt in Pt/TiO₂/Pt [44] in some cases can participate in the mechanisms of resistive switching.

For the formation of an initial filament in a newly fabricated cell, a pulse of a higher voltage (forming) is usually required [45, 46], compared with pulses of further switching. Due to inhomogeneities in the composition and structure in the dielectric film of the cell, as well as nanoroughness (needle-shaped protrusions) of metal electrodes, the forming voltage pulse creates a local inhomogeneity of the field strength, and, accordingly, is controlled by the breakdown of the dielectric, which forms a conducting channel (channels) in the form of filaments with a high content of oxygen vacancies or metal cations. Generally speaking, the individual forming of each cell for a giga- or terabit memory chip is not economically feasible; therefore, ways of creating formless filamentary memristors that do not require individual forming procedures are currently being intensively sought [17, 40, 47, 48].

A number of requirements are imposed on modern single-bit resistive memory cells for building ultralarge integrated circuits (ULICs) based on them: device design scalability, SET/RESET rewriting voltage less

than 1 V, power consumption less than 10 pJ per switch, switching time less than 10 ns, information retention time not less than 10 years at 85°C, number of rewriting cycles (endurance) 10^{12} , etc. A number of parameters, such as scalability [40, 49, 50], speed [9, 50, 51], and energy efficiency [52, 53], have already been achieved, albeit, in different cell designs and with different active dielectric materials.

At the same time, the current priority issues are endurance of the considered devices and retention time of information (retention time). These problems are the subject of analysis in this study.

DEGRADATION OF MEMRISTORS

Despite the fact that endurance of more than 10^{12} switchings was observed, for example, in [6, 47, 50], and the required retention time was stated in [54–57], these results were achieved in the study of a single device.

Switching of filament-type memristors involves disruption/creation filaments. For vacancy memristors, a filament is a region with an excess concentration of vacancies. Having an effective positive charge, oxygen vacancies attract electrons, forming neutral complexes. Such a complex (F-center) can be represented as a quasi-atom with energy levels located in the forbidden zone. Breaking away from the vacancy, the electron goes into the conduction band according to the reaction $F^x \rightarrow V_x^+ + e^-$. In cationic memristors, a filament is a conductive filament formed by metal cations. The advantage of the first group consists in longer retention times due to the rather high migration energy of the oxygen ions in the bulk of most oxides (>1 eV) [4, 58, 59]. In the case of the motion of cations, their activation energy for bulk diffusion is much lower (<0.3 eV) [60], which favors low switching voltages but also low retention times [61].

Papers [31, 62, 63] are devoted to the observation of filaments and the study of the dynamics of their switching. In [64, 65], a stochastic approach is proposed that simulates microscopic processes inside transition metal oxides. The model is based on percolation theory and a resistor network. The dynamics of the migration of oxygen vacancies without taking into account the Joule heating of the filament during the flow of an electric current [66–70] and taking into account the Joule heating [21, 71–76] were studied theoretically based on the kinetic equations.

The retention time of information for memristors is determined by the stability of the LRS and HRS in time. In order to determine it, after the SET/RESET transition to the structure, a voltage pulse is applied ($V_{\text{read}} \approx 0.1$ V, $t_{\text{read}} \approx 1$ ms) periodically ($\Delta t \approx 1$ s) and the dependence of the current on time is recorded for each resistive state. To eliminate the effect of charge accumulation, the polarity of the switching pulse should be periodically changed. This was done, for

example, in [37]. The predicted retention time of the memristor states should be 10 years at a temperature of 85°C. Real measurements are carried out over several hours/days, after which the data are extrapolated over time [48, 77, 79]. Thanks to the Arrhenius dependence probabilities of the formation/recombination of point defects, as well as their diffusion/drift processes, the retention time of information is often determined at elevated temperatures [37, 80–81]. After that, the retention time is recalculated to the required temperature value. This approach is also susceptible to errors. Thus, in the work [77], the dependence of resistance on the information retention time for the Pt/Al₂O₃/HfO₂/Al₂O₃/TiN memristor is investigated at room and elevated (85°C) temperatures. At room temperature, the resistances of the LRS and HRS increased with the observation time, while at 85°C, they decreased. In [37], using the TiN/HfO_x/Pt memristor as an example, it was shown that the estimate of the retention time based on data extrapolation may be incorrect due to the detected abrupt degradation of the HRS state by the complete failure at a certain point in time.

The endurance of a memristor cell is determined by its stability as a result of multiple switching cycles. Each cycle consists of a set of voltage pulses: $V_{\text{set}} (\sim 1$ V, ~ 10 ns)– $V_{\text{read}} (\sim 0.1$ V, ~ 10 ns)– $V_{\text{reset}} (\sim -1$ V, ~ 10 ns)– $V_{\text{read}} (\sim 0.1$ V, ~ 10 ns). As a result, the dependence of the current (resistance) on the number of such cycles is obtained [33].

Analyzing the experimental data of many publications on structures in which switching is caused by the formation/rupture of a conducting filament, it can be seen that after a series of cyclic switchings in the memristor cell, the HRS and LRS are not reproduced with ideal accuracy. In a practically acceptable case, the resistances of the high-resistance and low-resistance states of single-bit memristors should remain within the allowable windows for HRS and LRS, set by the maximum and minimum values (Fig. 2a). Such behavior would mean no degradation of states. However, in some cases, it turns out that either the high resistance or low resistance is out of the specified range.

Memristor degradation is expressed as a change in resistance over time or number of switchings. Ultimately, degradation leads to device failure by the memristor “sticking” in a state with a certain resistance value [82]. When tested for endurance, the most common degradation of the state of the HRS (Fig. 2b), leading to a decrease in resistance in this state and, as a result, to the impossibility of switching the LRS into the HRS, takes place [9, 15, 21, 42, 83]. Sometimes, R_{HRS} increases with increasing switching cycles [52, 84] (Fig. 2c), and in some cases there is an increase in the resistance of R_{LRS} [25, 85] (Fig. 2d).

For retention time, the most typical cases are an increase in resistance in the LRS and a decrease in the HRS [28, 48, 80, 81, 86–88] (Figs. 2b, 2d). In [80, 81], the retention time of the Ir/Ta₂O₅₋₈/TaO_x/TaN mem-

Fig. 2. The dependence of the resistance of the memristor (R) on the number of switching cycles (N) or retention time (t) in the absence of degradation (a), monotonic degradation of high-resistance (b, c), and low-resistance (d) states.

ristor was investigated. It was found that for a memristor with a filament of a larger cross section, a decrease in resistance is observed in the HRS and an increase in resistance in the LRS for filaments with a smaller cross section. This result suggests that the degradation of the LRS and HRS states in the study of retention time is primarily determined by diffusion processes. For filaments of a small diameter, due to radial diffusion, the filament dissolves, leading to a decrease in the LRS. For filaments of a large diameter, the HRS degrades due to longitudinal diffusion in the rupture region.

During the switching cycles of states, the authors of the works [36, 82, 89–90] found a situation when, as a result of degradation, the memristor takes on some intermediate state between the R_{HRS} and R_{LRS} (Fig. 3). The degradation of a Ti/HfO_x/TiN memristor was investigated in [36]. The endurance test fails when 2.5×10^4 switching cycles after the application of a negative pulse. The memristor is stuck in an intermediate position between the HRS and LRS. Before the failure, the resistance of the LRS gradually decreased, while the HRS remained practically stable. The reason for the degradation, according to the authors, is due to the fact that SET/RESET repetitions lead to the appearance of additional defects, which causes (i) an increase in the reservoir of defects near the upper electrode and (ii) a decrease in the energy of their migration due to the higher density of vacancies, which leads

to an increase in the filament. It was found that the maximum value of the limiting voltage (V_{stop}) during the RESET cycle is the key parameter that controls the endurance of the switching (a decrease in V_{stop} leads to an increase in endurance). Sticking in an intermediate state was also observed for a Ti/HfSiO_x/TiN memristor [89]. It showed a slight decrease in the HRS and LRS with the number of cycles less than 1.5×10^5 ; then, the LRS began to grow, and the HRS fell sharply until they coincided. It has been found that the fault is always caused by negative voltage, i.e., when the filament breaks. The authors believe that the failure is due to the injection of defects from the lower electrode. As a result, the filament thickens, causing a decrease in the HRS.

Smooth resistance change HRS and LRS from first switching cycles/observation times observed in [5, 10, 25, 42, 43, 48, 49, 80, 81, 85, 86] (Fig. 2). Analysis of the Cu/HfO₂/Pt devices [42] showed a monotonic decline in the HRS with the first switching cycles and sticking in the LRS (Fig. 2b). A decrease in V_{SET} was noted with an increase in the number of switching cycles, while V_{RESET} grew. The main difference between the initial and switched filaments was the copper concentration, which was significantly higher in the second case. By adjusting the switching voltages, it was possible to achieve $>10^9$ switching cycles. Arrays of Cu/TaO_x/Pt memristors consisting of 50 cells were investigated in

Fig. 3. Resistance dependence (R) of a memristor on the number of switching cycles (N) in case of failure of the memristor in the intermediate state of resistances.

[42]. The time for which the HRS and LRS were maintained after 1, 100, and 1000 switching cycles was studied. It was observed that with an increase in the number of switching cycles, the time period during which the LRS state is maintained increases, while the time period for which the HRS is maintained decreases. This reduces the dispersion of resistances from device-to-device. According to the works [15, 42], the newly formed filament takes on its stationary shape, corresponding to the parameters of the switching pulse, after a certain number of switching cycles. If the pulse parameters are chosen incorrectly, then the evolution of the filament to the equilibrium state will be accompanied by degradation of the LRS and/or HRS.

In many cases, the resistance begins to change only after a certain critical value of the observation time/switching pulse [24, 37, 42, 52, 90] (Fig. 4).

For a TaN/ZnO/ZrO₂/Pt memristor [24], the LRS does not change within 10³ switching cycles, while the HRS begins to decline after 900 cycles (Fig. 4a). The authors attribute the possible reasons for the deterioration of the HRS to the unstable RESET operations

arising from the excessive growth of conductive filaments and the creation of other filaments during the switching cycles. A decrease in the HRS with increasing switching cycles, caused by unrecovered defects in the oxide matrix, accumulating from cycle-to-cycle, was also observed in the TiN/HfO_x/AlO_x/Pt memristor [10].

In [90] degradation of the highly conductive state was observed (Fig. 4b). At the same time, an increase in voltage V_{SET} was detected after 10⁷ and 10⁹ switching cycles. According to the authors, this increase indicates a decrease in the mobility of oxygen vacancies. Since the failure of the memristor occurs at a fixed voltage, by increasing the voltage at the gate of the memristor, it can be returned to the operating state again. In [91], using a TiN/Hf/HfO₂/TiN memristor as an example, a method for controlling the motion of defects was proposed. Four regions were found depending on the resistance of the LRS and HRS on the number of switching cycles: (i) where the resistance states are stable, (ii) resistance increases in LRS state, (iii) the memristor is stuck in the HRS, and (iv) in a region restored by the application of a higher positive voltage. It was found that, after a failure, the rupture region is surrounded by defects with lower/higher energy levels, which disappear after the memristor is restored, which confirms their role in degradation. When the concentration of these defects reaches a critical level, they (i) repel other defects from the transition to the discontinuity region, causing the SET to fail; (ii) they can form a shunt current path at V_{set} by reducing the stress in the region of the filament's rupture and contributing to the degradation of the memristor; (iii) the defects impede conductivity when V_{read} due to energy level shift and/or the longer electron tunneling path.

The possibility of creation a memristor memory cell after its failure is also discussed in [52]. Thus, the endurance of the memristor TiN/Hf/HfO₂/TiN is ~10⁷ switchings, but after each failure it was possible to restore the device by applying an increased SET voltage (by a fac-

Fig. 4. Resistance dependence (R) of a memristor on the number of switching cycles (N) or retention time (t) with a sharp degradation of the high-resistance (a) and low-resistance (b) states.

tor of at least 5). Thus, the introduction of a check operation can significantly increase the lifespan of these devices. For an Pt/TiO₂/TiN memristor [9], a test during retention at 85°C showed that resistances with higher values increase slightly with time, while the states with lower resistances remained practically unchanged for more than 256 hours. The endurance test passed 2×10^6 switching cycles, after which the memristor became stuck in the LRS state. The RESET operation using the DC sweep mode returned the device to an operating state, after which it withstood another $\sim 10^6$ switching cycles.

Further, various factors are discussed that affect the endurance and retention time of information in memristor memory cells.

1. Influence of Temperature

The operation of memristors is based on the drift of ions within the dielectric layer and reactions of the formation/recombination of point defects. The degradation of memristors is caused by diffusion processes through the conducting electrodes and in the region of the dielectric surrounding the filament. All the listed processes have an Arrhenius dependence and, therefore, strongly depend on temperature. Therefore, it should be expected that the increase in temperature leads to a decrease in the endurance and retention time of memristors [42, 43]. The decrease in retention time with increasing temperature has been confirmed by numerous studies. Thus, tests at elevated temperatures (100, 125, 140°C) [92] showed that the retention time (τ) dropped with increasing temperature, and $\ln \tau$ turned out to be a linear function of the reciprocal temperature, which indicates the diffusion nature of degradation. The growth of temperature leads to earlier degradation also for the Cu/HfO₂/Pt memristor [42]. In this case, the HRS was practically independent of temperature, which indicates tunneling as the dominant form of conduction in a weakly conducting state. The metallic properties of the LRS of this memristor are indicated by the linearity of the current-voltage characteristic with positive temperature dependence. In [78], a formless W/AlO_x/Al₂O₃/Pt/Ti memristor was obtained with a high switching speed (28 ns). The study of this memristor at high and low temperatures relative to room temperature showed a decrease in the HRS/LRS resistance ratio ($\sim 10^3$ at 100, $\sim 10^3$ at 298, and ~ 80 at 400 K) and retention time ($\sim 10^6$ s at 100 K, $\sim 10^4$ s at 400 K) at elevated temperatures.

In contrast, in [21] the addition of a layer HfO_x layer in an Au/CeO_x/Al memristor provoked an increase in temperature in the region of the filament and increased the endurance of this structure. In [46] it was possible to reduce the forming voltage from 2.5 to 1.7 V due to the process at increased (125°C) temperatures. At the same time, the spread of the HRS and LRS resistances was reduced and the information

retention time increased by a factor of more than 40. The authors believe that the reason for the obtained improvements is the recombination of excess oxygen vacancies.

The test for the retention time for a Pt/Al₂O₃/HfO₂/Al₂O₃/TiN memristor [77] was carried out at room and elevated (85°C) temperatures. At room temperature, after 10^2 s, there is a parallel increase in the LRS/HRS resistance; and at 85°C, a parallel decline. The authors explain the obtained result by the competition of two effects: (i) oxygen from the atmosphere can slowly diffuse into the samples at room temperature, which leads to a gradual decrease in the concentration of oxygen vacancies, i.e., an increase in the HRS and LRS; (ii) an increase in temperature provokes the creation of oxygen vacancies. At low temperatures the first mechanism prevails; and at high temperatures, the second mechanism is prevalent.

These results indicate that, in order to increase the retention time, it is necessary to choose materials with high energies of migration of oxygen vacancies. However, this will inevitably lead to an increase in the switching voltage. From the point of view of the endurance of devices, the lower temperatures are not a guarantee of an increase in the number of switchings, since lower temperatures make it difficult to recover the broken filament. Thus, for a W/AlO_x/Al₂O₃/Pt/Ti memristor [78], the best endurance was achieved at room temperature (10^8 at 100, 10^{10} at 298, and 10^7 at 400 K).

2. Influence of Switching the Pulse Parameters

The selection of the switching pulse parameters is the simplest way to improve the performance of the device. Therefore, the study of the influence of the duration and amplitude of the applied SET/RESET pulses is an important stage in the study of the properties of memristors.

Using the example of a TiN/HfO₂/Hf/TiN memristor, the authors [79] showed that with the optimal selection of the SET/RESET pulse parameters, the memristor's endurance can exceed 10^{10} . Most authors [90–92, 94] note that an increase in the switching amplitude leads to a decrease in the endurance of the device.

Thus, it was found in [90] that an increase in the voltage in a TiN/HfO₂/Hf/TiN memristor leads to its earlier failure, which is explained by the decrease in the mobility of oxygen vacancies (the energy barrier increases), due to the local relaxation of amorphous HfO₂ to the minimum energy state (short-range atomic rearrangement) caused by elevated temperatures. Also in this work, an increase in endurance was observed with an increase in the LRS resistance (below the operating current). A memristor whose operating principle is based on the diffusion of silver

ions [92] has shown endurance $>10^8$ switching cycles. According to the authors, the result obtained is associated with minimizing the switching voltage, since the endurance readings are reduced on devices with a large limiting current. The rise in the RESET voltage and its duration also reduced the endurance of the TiN/Ta₂O₅/Ta memristor [94]. It was found that at high voltages and pulse durations the memristor sticks in the HRS position; and at low voltages, in the LRS. The results are explained by the gradual oxidation of the TiN electrode, which ultimately leads to the impossibility of filament reduction due to the difficult removal of O from TiN in the first case. However, toggling with lower RESET voltages may be insufficient for the oxidation of TiN, but sufficient for the diffusion of oxygen ions along the internode or grain boundaries. The endurance of the TiN/Hf(Al) O/Hf/TiN memristor was tested at two SET voltages of 1.5 and 2.5 V [83]. In the first case, after $\sim 10^7$ there was a sharp rise in the LRS and a smoother rise in the HRS until they coincided. For 2.5 V after $\sim 10^7$ there is a decline in the HRS to the LRS level.

It was found in [89] that the endurance of the Ti/HfSiO_x/TiN memristor as a function of the applied voltage for the given duration has the maximum (V_m). An increase in duration leads to a decrease in V_m , leaving the maximum number of switchings approximately constant. The dependence of the area of the hysteresis loop of current-voltage characteristic at various recording voltages (0.2, 0.4, 0.6, 0.8, 1, and 1.2 V) in a 10-nm memristor was studied in [95]. It was found that the loop area first gradually increases with an increase in the write voltage, and after the critical value (~ 1 V) it drops sharply. It was found that the resistance in the HRS is practically independent of the recording frequency and voltage, while the LRS resistance increases sharply with increasing voltage at low switching frequencies and weakly at high frequencies. In [48], it was found for an unformed Al/ZnO/Al memristor that the hysteresis window decreases with an increase in the sweep frequency. According to the authors, the detected interstitial oxygen ions play a decisive role in the process of resistive switching, contributing to the destruction of oxygen vacancies during the RESET process.

A number of works suggest varying the amplitude and/or duration of the switching pulse to increase the service life of the device. The conductivity values of a Ta/TaO_x/Pt memristor [96] in the 1T1R cell array was achieved by a combination of transistor gate control and a developed feedback algorithm. It was obtained that one cell of the TaO_x memristor can be precisely and repeatedly programmed (more than 10^6) to precisely represent 6-bit values. The authors of [97] managed to improve the endurance of the Ti/HfO₂/Pt memristor due to the smooth transition from the ON state to the OFF state and vice versa. This was achieved by using a positive offset current sweep

during the SET and a rising voltage sweep during the RESET. By adding a series resistor to a Pt/Ta/TaO_x/Pt/Ta to the memristor [98], with the correct resistance during the SET and RESET cycles, it is possible to suppress the unevenness of the internal voltage drop across it, which leads to a significant increase in its service life. Application of a fixed write pulse can lead to degradation due to changes in the thickness/length of the break in the filament. To avoid this, the theoretical model [99] proposes a recording scheme that identifies the optimal amplitude and duration for the recording pulse. It has been found that the proposed scheme for various malfunctions of the memristor can effectively improve its endurance.

3. Influence of the Concentration of Oxygen Vacancies

The concentration of oxygen vacancies is the governing parameter for memristors, whose operation is based on the movement of oxygen anions. The more vacancies that are contained in the oxide the smaller the voltage that is required for the formation of a filament. However, the accumulation of a large number of vacancies may be more likely to lead to the formation of pores, multiple filaments, and/or resizing of the initially formed filament during rewriting operations.

According to the work [100], the mechanisms of degradation of memristors can be attributed to the additional oxygen vacancies generated/recombined during switching, which leads to a change in the initial structure of the filament. When additional oxygen vacancies are generated during switching in or near the filament region, the filament increases, while the HRS and LRS decrease. The increase in resistance is a result of the additional recombination between oxygen ions and oxygen vacancies with an increase in the distance between the gaps during the RESET. Sometimes the memristor sticks in the intermediate state, mainly due to the defects that emerge from the upper and lower electrodes, which can lead to breakage of the filament.

The dependence of the endurance of the Pt/TaO_{2-x}/Ta₂O_{5-x}/Pt memristor on the concentration of vacancies in the TaO_{2-x} layer was studied in [50]. It was found that an increase in the concentration of oxygen vacancies lowers the switching resistance and the number of switching cycles. For memristor of $30 \times 30 \mu\text{m}^2$, endurance was achieved for 10^{12} switching cycles.

However, according to [101], where structures based on TiO₂ with different concentrations of oxygen vacancies (10, 20, and 30%) were investigated, it was found that the best manifestation of the memristor properties corresponds to a concentration of oxygen vacancies of 20%. The work [102] is also devoted to a study of TiO_x-based memristors. Four TiO_x sublayers were made in it with different contents of oxygen

vacancies, and various combinations of the succession of layers were investigated. It was found that the ON/OFF ratios and retention times in both the on and off states are the best for a structure with a sequence of layers corresponding to a nonmonotonic distribution of the oxygen vacancy concentration. At the same time, the creation of a TaO_x film in a $\text{Pt}/\text{TaO}_x/\text{Pt}$ memristor [103] with an oxygen concentration gradient ranging from $\text{Ta}_2\text{O}_{5-x}$ at the anode to TaO_{2-x} at the cathode made it possible to increase the endurance of the studied memristor to values exceeding 10^9 switching cycles. For $\text{Pt}/\text{HfO}_x/\text{TiN}$ [104], it was shown that in the case of an excessive number of vacancies ($\text{HfO}_{1.5}$ compared to HfO_2), a reduced forming potential is required, but at the same time, an increase in the spread of resistances is observed in both the HRS and LRS. In this study, a model is proposed that includes the rupture of the filament caused by the field and temperature. The rupture occurs near the anode in the case of a stoichiometric oxide, and at both interfaces in the case of an oxygen deficiency. According to the model, the thermal ion/vacancy motion decreases in the oxygen-deficient memristor due to the higher heat transfer.

Thus, the concentration of oxygen vacancies is the most important parameter in the creation of anionic memristors. However, an unambiguous relationship between the concentration of vacancies and the endurance of the device has not been traced, and further research is required in order to understand it.

4. Active Dielectric Layer Structure and Thickness

The choice of the dielectric and its parameters radically changes the switching characteristics, as well as its endurance and retention time.

One of the most important parameters is the thickness of the dielectric layer. A decrease in the thickness, on the one hand, leads to a decrease in the amplitude of the switching pulse, but on the other hand, it decreases the ratio of resistances in the high-resistance and low-resistance states. The growth of the TaO_x film thickness from 10 to 60 nm [54] for the $\text{Pt}/\text{TiO}_x/\text{TaO}_x/\text{Pt}$ memristor shows a nonmonotonic dependence of the HRS and LRS resistance on film thickness with the minimum corresponding to 20 nm. At the same time, according to [83], an increase in the thickness of the HfO layer in the $\text{TiN}/\text{Hf}(\text{Al})\text{O}/\text{Hf}/\text{TiN}$ structure increases the endurance of the device.

Multilayer dielectrics are the subject of research by many authors [18, 39, 105]. The addition of an additional layer promotes the formation of a vacancy reservoir, and its thickness and composition affect the size of the specified reservoir and the migration and formation energies of vacancies. The use of multilayer dielectrics also affects the energy of the formation/migration of defects, which decreases in the area of the oxygen deficiency [29, 106].

In addition, the dependence of the heat capacity, density, and thermal conductivity on the film thickness leads to a change in the heating of the filament with a variation in the thickness, and, therefore, strongly affects the diffusion, drift, and creation/recombination of vacancies [21]. In the works [12, 13, 27, 107–117], an increase in the stability of devices with a two-layer dielectric, such as $\text{AlO}_x/\text{HfO}_2$, $\text{Ta}_2\text{O}_{5-x}/\text{TaO}_{2-x}$, $\text{ZrO}_x/\text{HfO}_x$, ZrO_2/AlON , and $\text{AlO}_x/\text{Al}_2\text{O}_3$, was reported.

The $\text{Ag}/\text{SiO}_2/\text{Ta}_2\text{O}_5/\text{Pt}$ memristor was studied in [39], the switching properties of which are based on the disruption/creation of the Ag filament. Due to the SiO_2 layer, in which the mobility of Ag ions is low, the growth direction thins the Ag filament in the Ta_2O_5 layer, which leads to the dissolution of the Ag filament in the Ta_2O_5 layer in the following operations. In single-layer $\text{Ag}/\text{Ta}_2\text{O}_5/\text{Pt}$ and $\text{Ag}/\text{SiO}_2/\text{Pt}$ structures, there is a strong scatter in the HRS. The $\text{Ag}/\text{SiO}_2/\text{Ta}_2\text{O}_5/\text{Pt}$ memristor showed lower switching voltages and less variation in the HRS and LRS resistances from cycle-to-cycle. The endurance of the memristor cell has also increased. The $\text{SiO}_2/\text{Ta}_2\text{O}_5$ boundary is a reservoir of vacancies due to which this memristor cannot be considered purely cationic, which may explain the increased endurance of the composite memristor.

It was found in [118] that $\text{Ti}/\text{TiO}_2/\text{Pt}$ breaks down during the RESET, which results in an LRS with extremely low resistance, which confirms the overgrowth of the conductive filaments. However, the addition of a vacancy-rich-2 nm ZrO_{2-x} layer on the Ti/TiO_2 boundary increased the retention time ($>10^4$ s) without any apparent degradation of the HRS and LRS resistances. According to [119], graphene can be used as an intermediate layer between the electrodes and the dielectric to reduce the scatter of parameters between cycles, by suppressing the diffusion of atoms between the electrode and the insulator, thereby increasing its endurance. The introduction of graphene can reduce energy consumption due to its high out-of-plane contact resistance (compared to metal electrodes) and suppress surface effects: chemisorption and/or photodesorption. The introduction of the TiO_2 layer to the $\text{Pt}/\text{HfO}_2/\text{TiO}_2/\text{ITO}$ memristor [120] made it possible to reduce the switching voltage due to the formation of a virtual cathode in the HfO_2 layer. Similar results were obtained in [54] for the $\text{Pt}/\text{TiO}_x/\text{TaO}_x/\text{Pt}$ memristor. The $\text{Ti}/\text{TiO}_x/\text{Pt}$ and $\text{Ti}/\text{HfO}_2/\text{Pt}$ devices were manufactured to clarify the role of the TiO_x layer in the $\text{Ti}/\text{HfO}_2/\text{TiO}_x/\text{Pt}$ memristor [13]. The $\text{Ti}/\text{HfO}_2/\text{Pt}$ memristor demonstrates explicit switching, whereas the $\text{Ti}/\text{TiO}_x/\text{Pt}$ memristor does not. This means that the resistive switching effect mainly occurs in the HfO_2 layer, while the TiO_x layer can serve as a reservoir of vacancies. The influence of an intermediate TiO_2 layer on the

switching characteristics of the ZrO_2 -based memristor was studied in [121]. Compared to the $\text{Cu/ZrO}_2/\text{Pt}$ and $\text{Cu/ZrO}_2/\text{TiO}_2/\text{Pt}$ devices, the forming voltage, switching voltage, and reset current of the $\text{Cu/TiO}_2/\text{ZrO}_2/\text{Pt}$ and $\text{Cu/TiO}_2/\text{ZrO}_2/\text{TiO}_2/\text{Pt}$ devices are clearly improved. The formless $\text{Ag/MnO/Ta}_2\text{O}_5/\text{Pt}$ memristor [12] has three states: LRS, IRS, and HRS. The third state is explained as a break of the filament in MnO , and the HRS in both MnO (vacancy reservoir) and Ta_2O_5 . The resistance window is 10^4 . The $\text{MnO/Ta}_2\text{O}_5$ system has greater endurance and a lower switching voltage than structures with a single layer. The influence of the Al_2O_3 layer [122] in the $\text{Ti/Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3/\text{Pt}$ memristor was studied by comparing its properties with a memristor without or with only one Al_2O_3 layer. It was found that the initial version has the largest resistance window and endurance of more than 10^5 cycles without visible degradation. According to the authors of [27], switching in a formless $\text{Pt/NbO}_x/\text{TiO}_y/\text{NbO}_x/\text{TiN}$ memristor was carried out due to the capture/release of electrons, where the oxygen vacancies in the central TiO_y and/or Ti impurity centers in the NbO_x layer near the upper Pt electrode play the role of traps. In this device, the switching current was much lower than that of the oxygen ion migration memristors. Adding the NiO_x layer [123] in $\text{ITO/TaO}_x/\text{NiO}_x/\text{Al}$ lowers the switching voltage greatly (ITO is a solid solution of indium(III) and tin(IV) oxides, typically 90% of the former and 10% of the latter). The proposed design avoids the breakage of filaments during the RESET process, which provides a more uniform and stable resistive switching behavior than other ReRAM devices. A study of the effect of an additional dielectric layer on the thermal properties was carried out in [21]. With the ratio of the thickness of the HfO_x layers to the CeO_x layers of 0.1 for the $\text{Au/CeO}_x/\text{HfO}_x/\text{Al}$ memristor, the maximum heating is observed in the filament region, which is explained by the dependence of the thermal conductivity of the hafnium oxide layer on the thickness. With this ratio, the maximum endurance ($>2 \times 10^5$) and the minimum operating switching voltage are observed.

Various dielectric materials were compared in [124, 125]. It was revealed in [124] that a memristor with $\text{Ta}_2\text{O}_5/\text{Ta}$ has significantly better endurance ($>10^9$) compared to the HfO_2/Hf memristor. A comparison of the HfO_2 , TiO_2 , Ta_2O_5 , and Al_2O_3 metal oxides as an insulating layer of the memristor is carried out in [125, 126]. The energies of the formation of oxygen vacancies and their migration barriers were calculated. It is shown that contact with an active metal lowers the energy of vacancy formation. The high energy of formation reduces the likelihood of new vacancies forming during switching cycles, which ensures a constant number of vacancies and, as a consequence, increases endurance. TiO_2 oxide contains a number of substoichiometric TiO_{2-x} phases, which will prevent the pres-

ervation of the number of vacancies and, therefore, it is not advisable to use it to increase the endurance of devices. Al_2O_3 has a relatively high energy of formation of the O vacancy and high migration energy, making the migration of vacancies in the ReRAM cycle difficult. According to the authors, the endurance of Ta_2O_5 is due to the fact that Ta_2O_5 remains amorphous at higher temperatures than HfO_2 and the adaptability of its lattice to the formation of oxygen vacancies.

Thus, by combining various oxides and varying the thickness of the films of an active medium, it is possible to control the switching parameters of the memristor, as well as its service life and information retention time.

5. The Influence of the Parameters of Conducting Cell Electrodes

The memristor electrode material not only affects the switching parameters but can also lead to rapid degradation of the device. The electrode material can be reactive with respect to oxygen and inert. The first type of electrodes is typically used to create a vacancy reservoir at the electrode/dielectric interface through a heterogeneous chemical reaction with the dielectric material. In this case, the energy of the formation/migration of defects decreases upon contact with the active electrode [125].

[103] compared to the different electrode materials for the TaO_x -based memristor. It was found that memory cells with Ir, Pt, and Au electrodes having a high work function of electrons show stable resistance switching behavior, in contrast to Ag or W electrodes. In this study, it was found that stable switching occurs for metals of electrodes, whose electrochemical potential is greater than that of Ta. This indicates that the absence of the oxidation reaction of the electrodes is preferred for resistance switching. The authors [5] found that using Ru as the bottom electrode (BE) in the $\text{Pt/Ta}_2\text{O}_5/\text{BE}$ memristor leads to a decrease in the switching voltage and a significant (by almost 3 orders of magnitude) maximum current level compared to the BE electrodes from Ta and Pt. Replacing the TiN electrode with Ru [94], which has a lower affinity for the oxygen anions in the $\text{TiN/Ta}_2\text{O}_5/\text{Ta}$ memristor resulted in an increase in stability to more than 10^8 switching cycles. The authors explain the results obtained by the continuous slow oxidation of TiN at the heterointerface, which changes the vacancy balance in the reservoir and, ultimately, leads to the impossibility of filament reduction due to the difficult removal of O atoms from TiN. The characteristics of the $\text{Pt/HfO}_2/\text{TiO}_2/\text{HfO}_2/\text{Pt}$ and $\text{Pt/HfO}_2/\text{TiO}_2/\text{HfO}_2/\text{TiN}$ memristors, due to the material of the electrodes, were compared in the work [23]. In the case of a Pt electrode, the HRS/LRS ratio is $\sim 10^5$; and for the TiN electrode, it is $\sim 10^2$. In addition, the TiN memristor exhibits a strong HRS scatter and requires large switching voltages to extract vacancies from the reservoir.

For Pt/Ta₂O_{5-x}/TaO_{2-x}/Al₂O₃/Pt [127], it was found that the roughness at the Pt/Ta₂O_{5-x} interface affects the switching mechanism in the memristor cell. The roughness contributes to the strong localization of the electric field, contributing to the formation of single filaments. At the same time, increasing the smoothness of the contacts contributes to the formation of multibit states. Previously, in [84] it was also found that due to the chemical-mechanical polishing (CMP) in the manufacture of the TiN/HfO_x/TiN memristor cell resulted in increasing the endurance to more than 10¹⁰ switching cycles.

CONCLUSIONS

The review discusses the influence of temperature and switching pulse parameters, as well as the concentration of oxygen vacancies in the reservoir, materials of the conducting electrodes, and the active dielectric layer in the memristor, on the ability of devices to maintain the given value of the HRS and LRS resistance over time, and the stability of the HRS and LRS states during multiple rewriting cycles.

According to the results presented in the review, it can be concluded that the influence of these parameters on the endurance and the retention time of the states of memristors is complex and multifactorial. However, the following qualitatively described tendencies can be distinguished:

—A rise in temperature leads to a decrease in the endurance of the memristor cell due to the growth of activation processes of diffusion/migration and the generation/recombination of point defects. An increase in temperature can also lead to the formation of crystals of a new phase, which also reduces the endurance of the devices.

—An increase in the switching voltage and an increase in the switching pulse duration beyond the minimum required values also reduce the cell endurance, which can be explained by the excessive temperature rise in the filament region, and by the evolution of the filament during switching to a nonstationary state (breakage or excessive thickening).

—An increase in the concentration of oxygen vacancies in the reservoir and the active region of the dielectric contributes to a decrease in the forming potential and sometimes leads to the formation of a formless memristor, but at the same time the spread of resistances increases the HRS and LRS with the sequential switching of the cell, and its endurance is also reduced.

—The use of cells' electrodes inert with respect to oxygen increases the service life and retention time of the information in the memristor cells. The films of the electrodes should have a minimum number of defects and insulate the active medium of the dielectric from the external environment. In some cases, it

was found that sometimes a memristor degrades due to the defects introduced by the electrodes.

—The use of multilayer dielectric structures as the active medium of the memristor makes it possible to adjust the size and position of the vacancy reservoir, as well as the energy of the formation/migration of defects.

—Of the analyzed dielectrics in memristors, tantalum oxide Ta₂O₅ has the lowest energy of the migration and formation of oxygen vacancies, and remains amorphous at higher temperatures. This explains its advantage in the endurance of the cells and allows the use of low switching potentials.

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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