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ELECTRONICS AND RADIO ENGINEERING

A Generator of Nanosecond High-Voltage Pulses Based on Shock-Ionized Dynistors

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Abstract—A generator of high-power nanosecond pulses consisting of four stages that are switched on in a relay-race mode is described. Each stage contains a storage capacitor with an operating voltage of 8 kV and an assembly of series-connected shock-ionized dynistors. The possibility of switching current pulses with an amplitude of 800 A to a load of 30 Ω a rise time of 4 ns, and a repetition rate of 100 Hz is demonstrated. The prospects for increasing the output voltage and the output energy of the generator are determined.

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Ensuring the high efficiency of nanosecond pulse generators requires the use of switches with a subnanosecond time of switching to a well-conducting state. A small spread of the enabling instants, a long service life, and a short shutdown time give certain advantages to semiconductor switches.

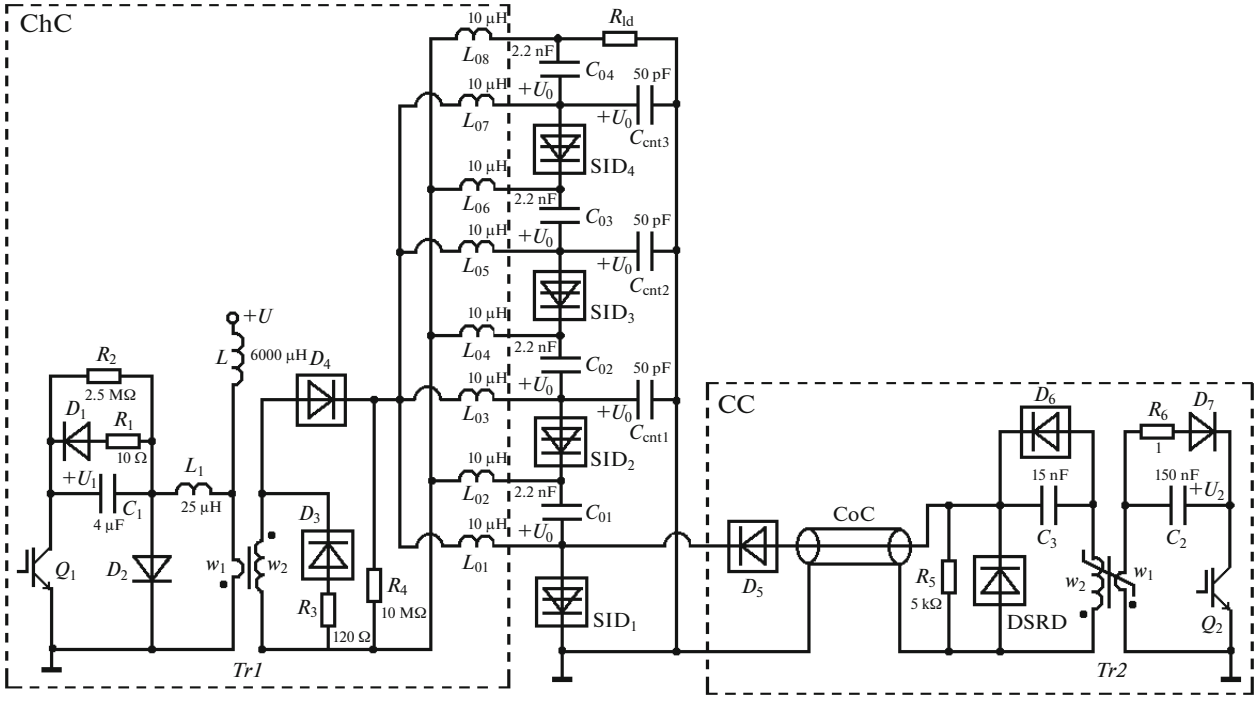

Fig. 1. Electrical circuit of the pilot generator: (Q_1, Q_2) IRGPS60B120KDP (two in parallel); (D_1, D_7) HER308 (two in series), (D_2) HER508 (two in series), (D_3) PG309 (two in parallel), (D_4) HER308 (16 in series), (D_5) K100UF (two in parallel), (D_6) HER308 (three in series); (CoC) RK75 cable; (DSRD) assembly of 24 16-mm-diameter diode structures; (*Tr1*) 2NSR amorphous-permalloy core, eight rings with dimensions of 64 × 40 × 10 mm, $w_1 = 4$, $w_2 = 75$; and (*Tr2*) N87 (EPCOS) ferrite core, eight rings with dimensions of 25.3 × 14.8 × 10 mm, $w_1 = 1$, $w_2 = 3$.

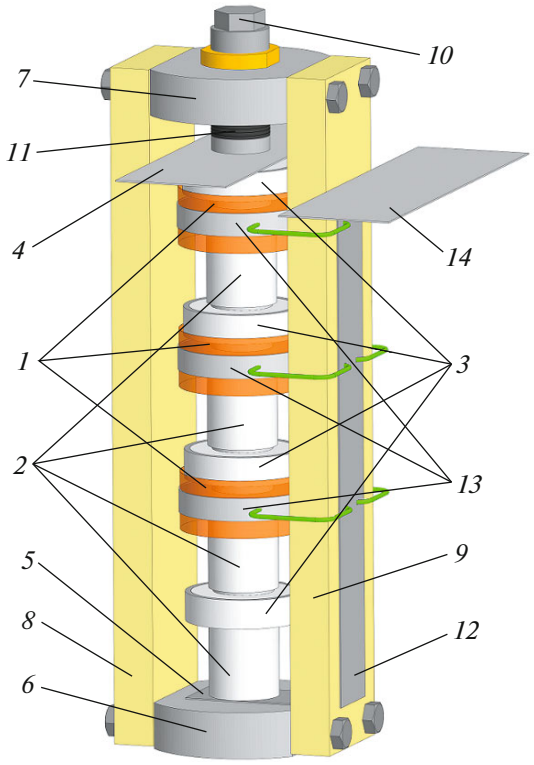

Fig. 2. Design of the SID-generator stages: (*1*) insulating film; (*2*) dynistor assemblies; (*3*) storage capacitors; (*4*, *5*) potential and grounded buses, respectively; (*6*, *7*) aluminum flanges of the clamping device; (*8*, *9*) caprolon plates of the clamping device; (*10*) bolt for providing a clamping force; (*11*) spring washers; (*12*) bus; (*13*) tape electrodes; and (*14*) output bus.

Currently, the most powerful semiconductor switches with subnanosecond switching times are the thyristor-type two-electrode silicon structures (dynistors) described in [1–4]; their principle of operation was first described in [5]. They are switched by a high voltage pulse with a nanosecond rise time. In the process of applying a rapidly increasing nanosecond voltage pulse to the dynistor structure, an avalanche breakdown does not have time to develop, and the field strength in its base regions reaches a value sufficient to initiate the shock ionization. The current carriers created as a result of the shock ionization provide very fast (shorter than a nanosecond) switching of the dynistor structure to a high-conductivity state, which is then maintained due to the two-way injection of current carriers from emitters.

The high efficiency of generators of powerful nanosecond pulses with switches based on optimized shock-ionized dynistors (SIDs), which were first described in [10–12], was shown in [6–9]. These generators contain a high-voltage storage capacitor, which is discharged through a load when an assembly of series-connected SID structures is switched on. SIDs are switched either simultaneously using a common control circuit or in a relay-race mode when the control circuit triggers a small number of dynistor structures, while the rest are switched on using additional capacitors that form an overvoltage wave. The main disadvantage of such generators is that the amplitude of their output voltage cannot be greater than the charging voltage of the storage capacitor.

The relay-race initiation of SIDs determines the possibility of developing multistage SID generators constructed according to the well-known Marx scheme, which provides formation of an output voltage by summing the voltages of stages constructed on the basis of comparatively low-voltage storage capacitors.

This possibility was confirmed by developing an experimental four-stage SID generator in which the voltage of a stage U_0 was 8 kV. Each stage contained a KVI-3 disk storage capacitor with a capacitance of 2.2 nF and a SID assembly consisting of four dynistor structures located between aluminum cylindrical electrodes in a tubular fluoroplastic body. The SID structures were 16 mm in diameter and allowed the application of a stationary voltage of 2.5 kV. At a rise time of a triggering action of ~2.5 ns, the SID structures were switched at a voltage of ~4.6 kV.

The electrical circuit of the generator is shown in Fig. 1. It contains SID_1–SID_4 units, a load R_{ld}, storage capacitors C_{01}–C_{04}, and triggering capacitors C_{cnt1}–C_{cnt3}. In the initial state, all capacitors are charged to the same voltage U_0 using a charging circuit (ChC). The charging-process duration (~15 μs) is determined by the duration of the current that flows through the winding w_2 of a step-up transformer *Tr1* after switching a transistor switch Q_1 on. Inductances L_{01}–L_{08} eliminate the mutual influence of the capacitors C_{01}–C_{04} during formation of a voltage pulse across the load. The DC circuit (~1 A) based on a choke L stabilizes the magnetic state of the transformer *Tr1* core.

The SID_1 unit of the first stage is enabled by a control circuit (CC). The other SID units are switched in a relay-race mode using the capacitors C_{cnt1}–C_{cnt3}.

The control circuit is made according to the scheme considered in [7]. The high-voltage triggering nanosecond pulses are formed using a diode opening switch in the form of an assembly of series-connected DSRD (drift step-recovery diodes) structures that were first described in [13]. After switching the transistor switch Q_2 on, a direct current with an amplitude of ~210 A and a fundamentally short duration (~350 ns) flows through the DSRD assembly. As a result, the capacitor C_3 is charged and a reserve of electron–hole plasma is created in the DSRD structures. When the DC current terminates, the transformer *Tr2* core satu-

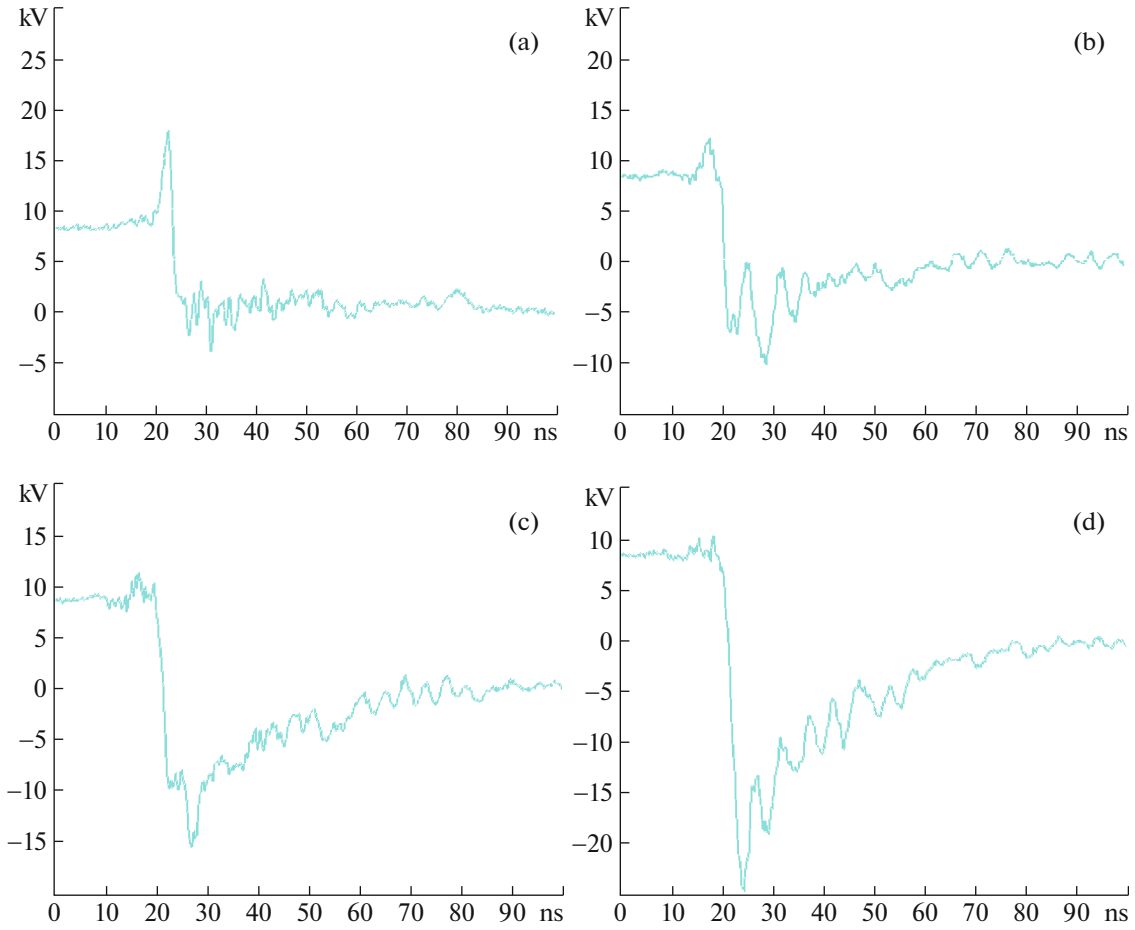

Fig. 3. Waveforms of the voltages at (a) the SID_1 unit and at the (b) C_{cnt1}, (c) C_{cnt2}, and (d) C_{cnt3} capacitors.

rates, the inductance of the winding w_2 decreases abruptly, and the C_3 discharge current with a fundamentally short leading edge (~100 ns) flows through the DSRD assembly. This current provides the withdrawal of the entire accumulated charge from the DSRD structures and their shutdown in a time shorter than 3 ns.

During switching the DSRD structures off, a nanosecond voltage pulse with an amplitude of ~27 kV is formed at the input of the cable (CoC), which is determined by the product of the cable's characteristic impedance by the current through the winding w_2 at the instant of disabling the DSRD assembly. As a result, a voltage pulse with an amplitude exceeding U_0 is created at the end of the cable, and the CC output current flows through the diode D_5. This current provides fast charging of the capacitance of the SID_1 unit to the switching-on voltage $U_m \approx 18$ kV, which is determined by the sum of the switching-on voltages of the dynistor structures.

After the SID_1 unit is enabled, a discharge current of the capacitors C_{cnt1} and C_{01} is switched to the SID_2 capacitance; its rise rate is determined by the wiring inductance of the C_{cnt1}–SID_2–C_{01}–SID_1 circuit. As a result, the voltage across SID_2 increases rapidly from the initial value $U_0 = 8$ kV to the switching-on voltage U_m. Since $U_m > 2U_0$, enabling the SID_2 unit requires a sufficiently large capacitance of the capacitor C_{cnt1}. After SID_2 is enabled, the capacitors C_{cnt2}, C_{02}, and C_{01} begin to discharge through the SID_3 capacitance, and the voltage across SID_3 rises abruptly to the switching-on voltage U_m. Enabling of the SID_3 unit leads to switching-on of the SID_4 unit in the relay-race mode. As a result, a discharge current pulse of the series-connected capacitors C_{01}–C_{04} is switched to the load R_{ld}.

The operating conditions of the triggering capacitors C_{cnt1}–C_{cnt3} determine the high voltage of their charge exchange during the formation of the generator output voltage. The high reliability of these capacitors is provided by the simplicity of their design. One capacitor electrode is manufactured in the form of an aluminum cylinder and insulated with several layers of an adhesive tape in the form of a polyimide film with a width of 30 mm and a thickness of 42 μm. The second electrode is an adhesive tape in the form of a cop-

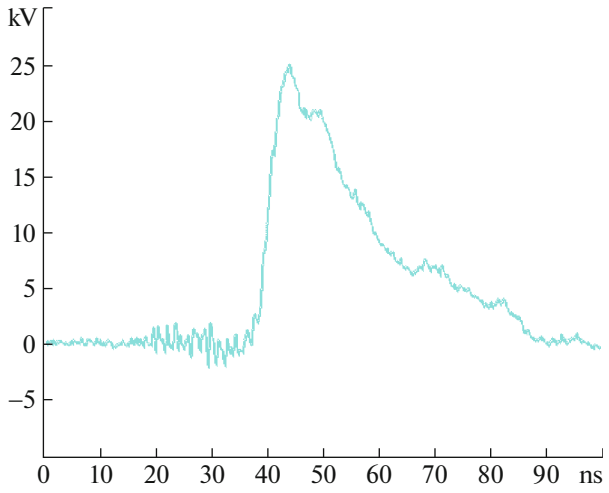

Fig. 4. Voltage waveform at the load.

per band with a width of 5 mm and a thickness of 100 μm, which is located on the outer layer of the film insulation in opposition to the cylindrical electrode. The capacitance of the triggering capacitor is determined by the diameter of the cylindrical electrode, the thickness of the film insulation, and the width of the tape electrode.

Figure 2 shows the design of the stages of the SID generator.

The cylindrical electrodes of the triggering capacitors are wrapped with an insulating film (*1*) and are located between the dynistor assemblies (*2*) and the storage capacitors (*3*). The electrical contact with a potential bus (*4*) and a grounded bus (*5*) is performed using a clamping device that contains aluminum flanges (*6*, *7*) and caprolon plates (*8*, *9*). The clamping force is created with a bolt (*10*) and transmitted using spring washers (*11*). The low inductance of the discharge circuit of the storage capacitors is achieved as a result of using a bus (*12*) connected bifilarly to a circuit that consists of dynistor units (*2*) and capacitors (*3*). The bus (*12*) is connected to the tape electrodes (*13*) of the triggering capacitors and to the output bus (*14*). The load is connected between the buses (*4*, *14*).

The generator was investigated under natural cooling conditions at a repetition rate of output pulses of 100 Hz. The load had the form of an assembly of low-inductance resistors and had a resistance of ~30 Ω.

Figure 3 shows the voltage waveforms at the SID_1 assembly (Fig. 3a) and at the triggering capacitors C_{cnt1}, C_{cnt2}, and C_{cnt3} (Figs. 3b–3d, respectively) that were measured with a Tektronix P6015A probe.

The waveform in Fig. 3a indicates that the voltage across the SID_1 unit increases to a triggering value of ~19 kV within a time of ~2.5 ns, which causes it to switch very quickly to the high-conductivity state. It can be seen from the waveforms in Figs. 3b–3d that the capacitors C_{cnt1}–C_{cnt3} in the initial state are charged to a voltage of 8 kV. A short voltage surge is due to their additional charging by the CC output current in the SID_1 enabling process. After SID_1–SID_4 are enabled, the discharge currents of the capacitors C_{01}–C_{04} branch to C_{cnt1}–C_{cnt3}. As a result, C_{cnt1}–C_{cnt3} are recharged to a higher reverse voltage.

Figure 4 shows a waveform of the voltage across the load. It was measured with a broadband divider with a resistance of ~500 Ω, which provided reliable measurements of signals with a rise time of more than 0.5 ns. The design of the divider was described in detail in [14]. Since the load has a resistance of 30 Ω, the output-current amplitude and rise rate are 800 A and 200 A/ns, respectively.

Thus, the conducted studies have shown that the pilot SID generator is capable of switching a pulse power of ~20 MW within a time of ~4 ns. An increase in the generator output energy and in the output voltage can be obtained via an increase in the capacitance of the stages and by using additional stages, respectively.

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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REFERENCES

1. Efanov, V.M., Kardo-Sysoev, A.F., Tchashnikov, I.G., and Yarin, P.M., *Proc. 1996 Int. Power Modulator Symposium,* Boca Raton, FL, 1996. https://doi.org/10.1109/MODSYM.1996.564440

2. Grekhov, I., Korotkov, S., and Rodin, S., *IEEE Trans. Plasma Sci.,* 2008, vol. 36, no. 2, part 1, p. 378. https://doi.org/10.1109/TPS.2008.918661
3. Korotkov, S.V., Aristov, Yu.V., Voronkov, V.B., Zhmodikov, A.L., Korotkov, D.A., and Lyublinskii, A.G., *Instrum. Exp. Tech.,* 2009, vol. 52, no. 5, pp. 695–698. https://doi.org/10.1134/S0020441209050091
4. Gusev, A.I., Lyubutin, S.K., Rukin, S.N., and Tsyranov, S.N., *IEEE Trans. Plasma Sci.,* 2016, vol. 44, no. 10, part 1, p. 1888. https://doi.org/10.1109/TPS.2016.2542343
5. Grekhov, I. and Kardo-Sysoev, A., *Sov. Tech. Phys. Lett.,* 1979, vol. 5, no. 8, p. 395.
6. Korotkov, S.V., Aristov, Yu.V., and Korotkov, D.A., *Instrum. Exp. Tech.,* 2022, vol. 65, no. 5, p. 750, https://doi.org/10.1134/S0020441222050074
7. Korotkov, S.V. and Aristov, Yu.V., *Instrum. Exp. Tech.,* 2022, vol. 65, no. 5, p. 745. https://doi.org/10.1134/S0020441222050062
8. Korotkov, S.V., Aristov, Yu.V., and Kozlov, K.A., *Prib. Tekh. Eksp.,* 2023, no. 4, p. 70. https://doi.org/10.31857/S0032816223040134
9. Korotkov, S.V., Aristov, Yu.V., Zhmodikov, A.L., and Korotkov, D.A., *Prib. Tekh. Eksp.,* 2023, no. 4, p. 74. https://doi.org/10.31857/S0032816223040146
10. Korotkov, S.V., Aristov, Yu.V., and Voronkov, V.B., *Instrum. Exp. Tech.,* 2019, vol. 62, no. 2, pp. 161–164. https://doi.org/10.1134/S002044121901010X
11. Korotkov, S.V., Aristov, Yu.V., Zhmodikov, A.L., and Korotkov, D.A., *Instrum. Exp. Tech.,* 2020, vol. 63, no. 5, p. 683. https://doi.org/10.1134/S0020441220050176
12. Korotkov, S.V., Aristov, Yu.V., Korotkov, D.A., and Zhmodikov, A.L., *Rev. Sci. Instrum.,* 2020, vol. 91, p. 084704. https://doi.org/10.1063/5.0015284
13. Grekhov, I., Efanov, V., Kardo-Sysoev, A., and Shenderey, S., *Solid-State Electron.,* 1985, vol. 28, no. 6, p. 597. https://doi.org/10.1016/0038-1101(85)90130-3
14. Belkin, V.S. and Shul'zhenko, G.I., *Preprint of Institute of Nuclear Physics Siberian Branch USSR Acad. Sci.,* Novosibirsk, 1991, no. 91–51.

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