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High-speed hybrid complementary ring oscillators based on solution-processed organic and amorphous metal oxide semiconductors

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Solution-processed single-crystal organic semiconductors (OSCs) and amorphous metal oxide semiconductors (MOSs) are promising for high-mobility p- and n-channel thin-film transistors (TFTs), respectively. Organic−inorganic hybrid complementary circuits hence have great potential to satisfy practical requirements. However, some chemical incompatibilities between OSCs and MOSs, such as heat and chemical resistance, make it difficult to rationally integrate TFTs based on solution-processed OSC and MOS onto the same substrates. Here, we report a rational integration method based on the solution-processed semiconductors by carefully managing the device configuration and the deposition and patterning techniques from a materials point of view. The balanced high performances as well as the uniform fabrication of the TFTs led to densely integrated five-stage ring oscillators with a short propagation delay of 1.3 μs per stage.

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Solution technique is of vital interest to both industry and academia for manufacturing electronic devices. To meet the requirements from low-cost and mass-producible electronics, such as printed electronics, Internet of Things (IoT) technology and Trillion Sensors Universe, solution techniques suitable for thin-film transistors (TFTs) on plastic substrates get more and more attention, where the solution-processed deposition of semiconductors is the primary subject. From engineering point of view, complementary circuits, which are constructed from the pairs of p- and n-channel TFTs, with high-mobility and performance-balanced p- and n-channel TFTs are preferred for actual devices such as radio-frequency identification tags and sensors because they can enable high operation speeds, low power dissipation, wide noise margin, and an easy and compact circuit design. For this aim, organic semiconductors (OSCs) are the most promising for the TFT applications owing to their solubility, low fabrication temperature and high compatibility with flexible substrates[1]. Thus far, OSC materials and solution techniques have been developed to facilitate the implementation of organic TFTs, particularly with single-aligned crystals or single crystals[2–8], which could be beneficial for high electrical properties. Despite the advantages of complementary circuits, most of solution-processable and high-mobility OSCs predominantly behave as hole-transporting materials, thus providing p-channel TFTs. In other words, (so-called n-type) OSCs suitable for n-channel TFTs are still lagging behind p-type counterparts due to their anisotropic crystal packings and less effective electronic couplings due to the essential introduction of strong electron-withdrawing groups[9]. Meanwhile, thin films of amorphous metal oxide semiconductors (MOSs) can be also prepared by solution processes, such as the sol-gel method, and have been developed for n-channel TFTs[10–15] because of their high electron mobility, excellent uniformity, and good ambient stability. By contrast to OSCs, MOSs are hardly useful for p-channel TFTs owing to the unfavourable hole formation as well as hole-transporting path due to the presence of highly occupied localised oxygen 2*p* orbitals[16]. Most of the reported circuits based on either only solution-processed OSCs or MOSs are hence designed by unipolar or pseudo-complementary operations[17–21], or complementary circuits with an unsatisfactory performance[22–27].

Therefore, the organic−inorganic hybrid system is one way to overcome such limitations as reported by using a vacuum process[28–31]. On the other hand, integrated circuits composed of solution-processed p-type OSC and n-type MOS[32–36] need to overcome chemical issues during their integration into the same circuit. For instance, OSCs are self-assembled in the solid states via weak van der Waals forces, whereas MOSs are covalently bound, which leads to incompatible processing parameters, such as temperature, heat and chemical resistance, and adaptability to lithographic processes. Due to the curing conditions, MOSs are prepared in advance of OSC deposition, which often deteriorates the MOSs maybe due to organic solvent vapour and heat during the OSC deposition. In addition, fine patterning is mandatory in both semiconductors and electrodes to avoid crosstalk and realise high-speed operations, and the requirement of a high degree of integration for practical application affords further tasks; therefore, the complementary circuits based on solution-processed, high-performance OSC and MOS are challenging. Although a few solution-processed hybrid complementary circuits have been demonstrated with photolithographic processes, their TFT performances, such as mobility and on-off switching ratio, were compromised because of the low mobility of macromolecular OSCs and the chemical degradation of MOSs[35,36]. In other words, there were no rational and feasible methodologies to integrate solution-processed OSCs and MOSs into complementary circuits despite the very simple concept of hybridisation.

In this study, we demonstrate the hybrid complementary circuits composed of solution-processed high-performance semiconductors: single crystals of a small-molecule OSC, 3, 11-dinonyldinaphto[2, 3-*d*:2', 3'-*d'*]benzo[1, 2-*b*:4, 5-*b'*]dithiophene (C_9-DNBDT-NW), and amorphous indium zinc oxide (IZO) for p- and n-channel TFTs, respectively. They were selected because of their high carrier mobility, uniformity, and potential scalability[7,37,38]. Herein, the patterning and integration of solution-processed MOS- and OSC-based TFTs were carefully managed through the selection of materials and processes to suppress chemical and physical degradations due to solvents and heat for high-speed operations. In the following sections, we will describe our achievements based on the hybrid complementary inverters, which exhibit desirable switching properties and excellent long-term stability on a plastic substrate. Demonstration of five-stage complementary ring oscillators revealed the uniformity of both single-crystal C_9-DNBDT-NW and amorphous IZO, and the short propagation delay of 1.3 μs per stage with an operation voltage of 10 V was achieved, indicating that the present facile method combining the advantages of solution-processed OSC and MOS can meet future IoT demands.

Results and discussion

Integrated process. The hybrid complementary inverter on a polyimide (PI) substrate with C_9-DNBDT-NW single crystals and amorphous IZO as the p- and n-channel material, respectively, is schematically illustrated in Fig. 1a. Both the p- and n-channel TFTs have bottom-gate top-contact structures. As illustrated in Fig. 1b, for the IZO-based n-channel TFT, gate electrodes were fabricated by photolithography and a lift-off process. Meanwhile, the AlO_x gate dielectric layer was formed by atomic layer deposition (ALD). The IZO layer was deposited by spin coating and patterned via photolithography and wet-etching. To reduce the number of photolithography steps, source/drain (S/D) electrodes of n-channel TFTs and gate electrodes of p-channel TFTs were fabricated simultaneously. Then, polymethylmethacrylate (PMMA) and parylene were sequentially formed as a bilayer gate dielectric for p-channel TFTs and as a passivation layer for n-channel TFTs to protect the back-channel of IZO-based TFTs against potential damage during subsequent integration processes, where PMMA could protect IZO from undesired chemical reaction with the monomeric diradical intermediate of parylene[39]. C_9-DNBDT-NW single-crystal was solution-crystallized by continuous edge casting method[7,40] on a superhydrophilic nano-ground glass template. Then the template was placed on the target substrate with C_9-DNBDT-NW facing PMMA/parylene dielectric layer. The C_9-DNBDT-NW single-crystal was transferred from the template to the surface of parylene by being mediated by a few water droplets penetrated into the C_9-DNBDT-NW/superhydrophilic template interface[41].

A cross-polarised optical micrograph of C_9-DNBDT-NW single crystals on the as-fabricated IZO-based TFTs before patterning revealed a clear crystal domain (Supplementary Fig. 1). Scanning electron microscopy (SEM) images of the cross-section of the C_9-DNBDT-NW channel produced by focused ion beam (FIB) machining revealed burr-free gate electrodes of the p-channel TFT (Supplementary Fig. 2), which ensures the parylene surface smooth enough for transferring the C_9-DNBDT-NW single crystal layer without undesired mechanical damages. OSC patterns and Au S/D electrodes were formed via a two-step patterning process, in which photosensitive dielectric materials (PDMs, a dry-film photoresist)/PMMA double sacrificial layers were employed for a damage-free

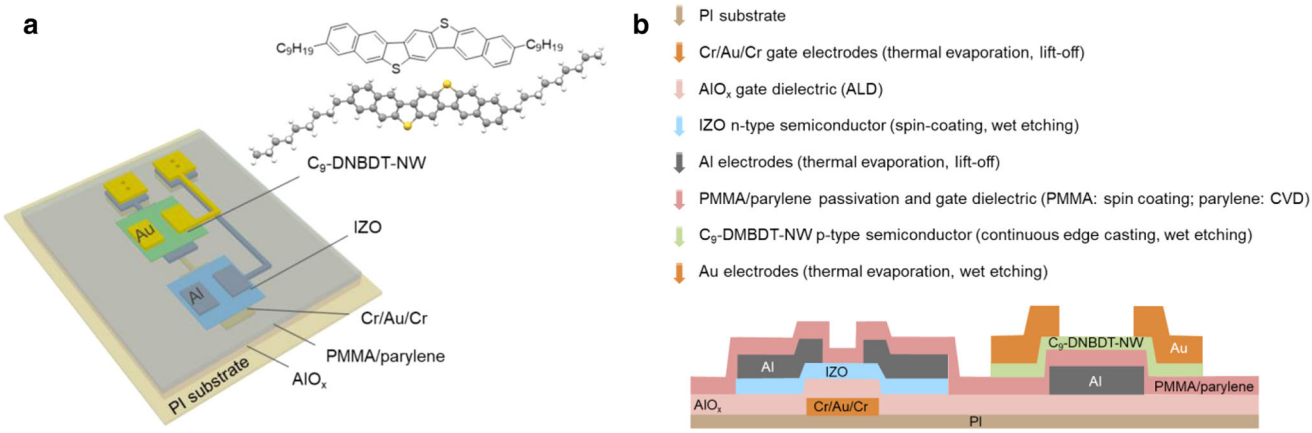

Fig. 1 Schematic structure, process flow and cross section of a hybrid complementary inverter with IZO as the n-channel material and C_9-DNBDT-NW single crystal as the p-channel material. a Schematic device structure. **b** Process flow and cross section.

patterning of OSC-based TFTs. As shown in Supplementary Fig. 3, PDM (the top layer) enables the formation of the OSC and S/D patterns while PMMA facilitated the stripping of the resist with acetonitrile, thus causing little damage to the OSC. The PDM was laminated on the substrate and patterned by photolithography[42,43], while the PMMA layer was deposited via spin coating and etched with O_2 plasma. Furthermore, the PDM contributed to the damage-free fabrication of OSC-based TFTs as the solvent content in the dry film was <2 wt.% and the PDM patterning process is based on the polymerization of double bonds rather than the generation of photoacids. Therefore, the potential damage induced by solvents or acids in conventional photolithography could be eliminated effectively. The contact resistance (R_c) of C_9-DNBDT-NW-based TFTs fabricated by this technology was studied using the transfer-line method, as described in the Supporting Information (Supplementary Note 1). The intrinsic mobility (μ_{int}) of C_9-DNBDT-NW TFTs was ~10 $cm^2 V^{-1} s^{-1}$ and the normalised contact resistance (R_cW) was ~230 Ω cm (Supplementary Fig. 4), which is comparable to our previous work on a monolayer C_9-DNBDT-NW-based TFT[44].

Electrical performance of the hybrid inverters. A micrograph of a complementary inverter is shown in the inset of Fig. 2a. The output curves revealed that both the n- and p-channel TFTs exhibited a typical output with good pinch-off behaviour and negligible hysteresis (Fig. 2a). The transfer characteristics of each TFT in the linear and saturation regions are illustrated in Fig. 2b–e. In the case of C_9-DNBDT-NW-based TFTs, transfer curves in the linear (Fig. 2b) and saturation (Fig. 2d) regions indicated the linear and saturation mobilities (μ_{lin} and μ_{sat}, respectively), on-off current ratio (I_{on}/I_{off}), off current (I_{off}), and turn-on voltage (V_{on}) of 5.8 and 5.1 $cm^2 V^{-1} s^{-1}$, 10^8, 10^{-12} A, and ~2 V, respectively; the corresponding values in the IZO TFT were 2.9 and 4.0 $cm^2 V^{-1} s^{-1}$, 10^8, 10^{-12} A and ~0 V, respectively (Fig. 2c, e).

Due to contact resistance, the effective mobility (μ_{eff}) is lower than μ_{int}, especially in short-channel devices, as shown in Eq. (1),

$$\mu_{eff} = \mu_{int} \frac{1}{1 + \frac{R_C W}{L} \mu_{int} C_i (V_G - V_{th})} \quad (1)$$

where C_i is the gate capacitance per unit area, V_G represents gate voltage, and V_{th} is the threshold voltage. The μ_{eff} of the C_9-DNBDT-NW-based TFT was estimated to be ~5.9 $cm^2 V^{-1} s^{-1}$, which is similar to the experimental value. In the case of the IZO-based TFT, R_cW was estimated to be 29 Ω cm and the effective resistance measured after the integration process is at similar to that of IZO TFTs before integration[38]. The good performance of C_9-DNBDT-NW- and IZO-based TFTs can be attributed to the high performance of the semiconductor materials and the well-designed integration processes. Patterned gate electrodes and short channels lead to degraded performance[45], especially in TFTs with bottom-gate top-contact structures. This may be because (1) as the channel length decreases, contact resistance starts to dominate, (2) the S/D patterning process may damage the semiconductor layer, and (3) the uneven surface caused by patterned gate electrodes may affect the uniformity of the active layer in the solution-processed semiconducting thin film. In this study, these problems were solved by using damage-free processes for both p- and n-channel TFTs, controlling the thickness and edge conditions of the gate electrode, and excluding the damage from further p-channel TFT integration process on IZO-based TFTs, which was processed with a bilayer PMMA/parylene passivation structure.

The hybrid complementary inverter exhibited the full rail-to-rail output swing and negligible hysteresis (Fig. 3a, b). The corresponding voltage gain and static current (I_{supply}) values are shown in Fig. 3c, d, respectively. At a V_{DD} of 7 V, a nearly symmetrical voltage transfer curve (VTC) with a midpoint voltage (V_M) of 3.42 V and maximum voltage gain of 38 V/V was observed. I_{supply} was 1×10^{-9} A at $V_{in} = 0$ V while I_{supply} was on the order of 10^{-7} A at high V_{in} (Fig. 3d), where the static power consumption was still <0.76 μW at $V_{DD} = 7$ V, for example. The higher static I_{supply} at high V_{in} was due to higher I_D of the p-channel TFT at $V_G = 0$ V or $V_{in} = 7$ V than that of the n-channel TFT at $V_G = 0$ V or $V_{in} = 0$ V by 5 orders of magnitude (3×10^{-7} and 1×10^{-12} A, respectively) (Supplementary Figure 5). Our future work will aim to control V_{on} for p-channel TFTs to further lower the static power consumption of complementary inverters. Figure 3e shows the VTC obtained with a V_{DD} of 7 V; the noise margins high (NM_H) and noise margin low (NM_L) are indicated by green rectangles ($NM_H = 2.7$ V and $NM_L = 1.9$ V).

It is particularly important to note that the hybrid complementary inverter exhibited a decent performance even after exposure to the ambient atmosphere (air) for 5 months (Fig. 3f), whereas the off current slightly increased in both TFTs (Supplementary Fig. 6). This may be attributed to a self-healing effect in which the number of carrier traps decreased slightly over time[6,46]. Besides, V_{on} of the IZO TFT slightly shifted, which would be due to the diffusion of environmental molecules such as oxygen and water because the current passivation layer, PMMA/parylene, could not isolate the device completely[39]. The passivation technique is being studied to further stabilise these devices.

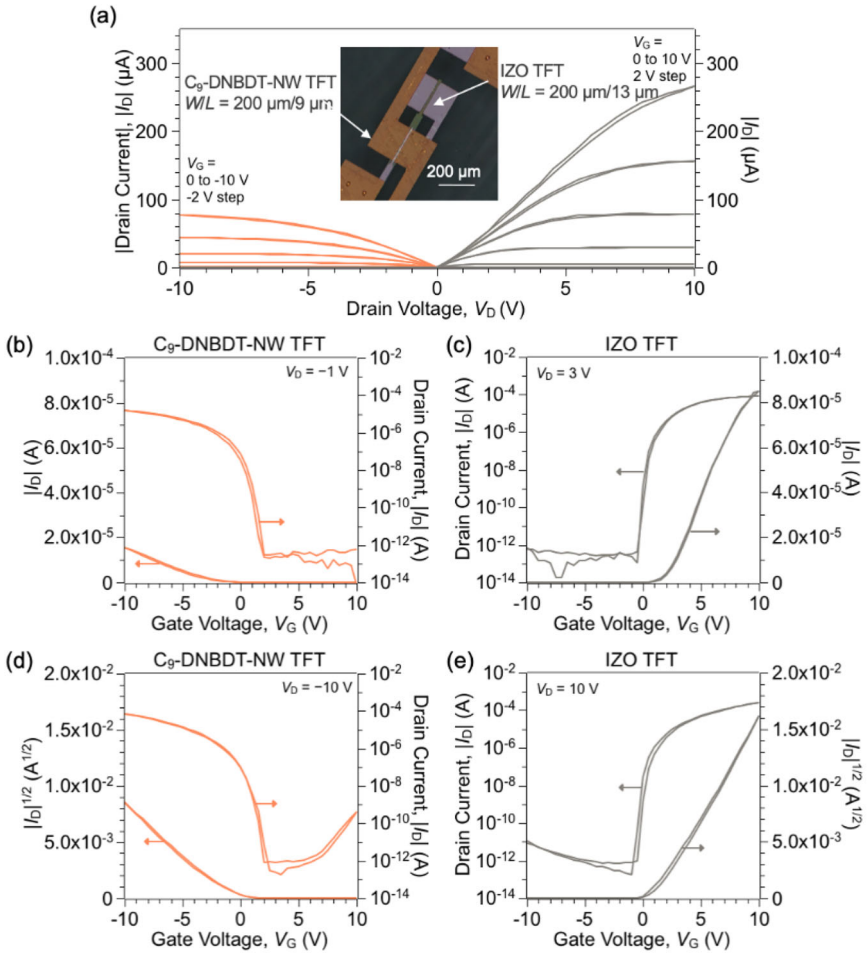

Fig. 2 Electrical performance of C_9-DNBDT-NW- and IZO-based TFTs. a Output performance. The inset shows a micrograph of a complementary inverter with channel width (W)/length (L) = 200 μm/9 μm for the C_9-DNBDT-NW p-channel and 200 μm/13 μm for the IZO n-channel. **b**–**e** Transfer characteristics in the linear region and the saturation region. V_D drain voltage.

Flexibility of the hybrid inverters. The PI substrate was delaminated from the glass support using a laser lift-off (LLO) method to evaluate the flexibility of the as-fabricated inverters. Figure 4a shows a photograph of the circuits on a free-standing PI film and Fig. 4b compares the VTCs obtained before and after delamination at $V_{DD} = 4$, 6, 8, and 10 V. The overlap between the VTCs at each V_{DD} indicated that the LLO process did not adversely affect the electrical performance of the inverter.

The bending stress test was carried out by measuring VTCs by laminating the PI film devices onto the cylindrical surfaces (Fig. 5a, b). With various bending radii (17.5, 12.0, and 6.0 mm), no significant changes were observed. As shown in Fig. 5c–f, both the p- and n-channel TFTs exhibited decent transfer characteristics under the action of a bending stress. The slight V_{on} shift is probably due to system error during measurement[38,47]. The bending stress applied on semiconductors depends not only on the bending radii but also device structure and substrate thickness. The corresponding surface strain (ε) can be calculated using the following equation[45]

$$\varepsilon = \frac{h_s}{2R} \times 100\% \quad (2)$$

where R is the bending radius and h_s is substrate thickness. In principle, when a substrate is bent, there is always a layer with zero bending stress and while the inner surface suffers compression stress, the outer surface suffers tensile stress. In this study, compared with the thickness of PI substrates (~10 μm), the total thickness of the other layers (<500 nm) was much less; hence, the TFTs experienced a tensile force perpendicular to the channels. In other words, the tensile force was applied in the c-axis direction, i.e., the preferred carrier-transport direction in the herringbone packing structure of the C_9-DNBDT-NW single crystal, which might decrease carrier mobility[48]. Meanwhile, amorphous IZO was isotopically stressed. Using Eq. (2), the maximum tensile stress was estimated to be 0.08% with a bending radius of 6 mm, at which the decrease in mobility was small (1%)[48]; this observation is consistent with our results. In addition, the small tensile stress should have negligible effects on the amorphous IZO layer. Therefore, the identical electrical performance of the inverter under bending conditions suggests that this hybrid technology can enrich flexible electronic applications.

Performance of hybrid ring oscillators. Unlike direct calculation by propagation delay, ring oscillators provide a simple and effective way to evaluate the maximum switching speed of larger logic gates. In a ring oscillator, each inverter delays the input signal for a specific time, which is defined as the stage propagation delay (t_p). To simplify, we assume that all inverters have the same property and the same delay time. The delay time at the output can hence be written as

$$T = 2nt_p \quad (3)$$

where n is the stage number and T is the period of the ring

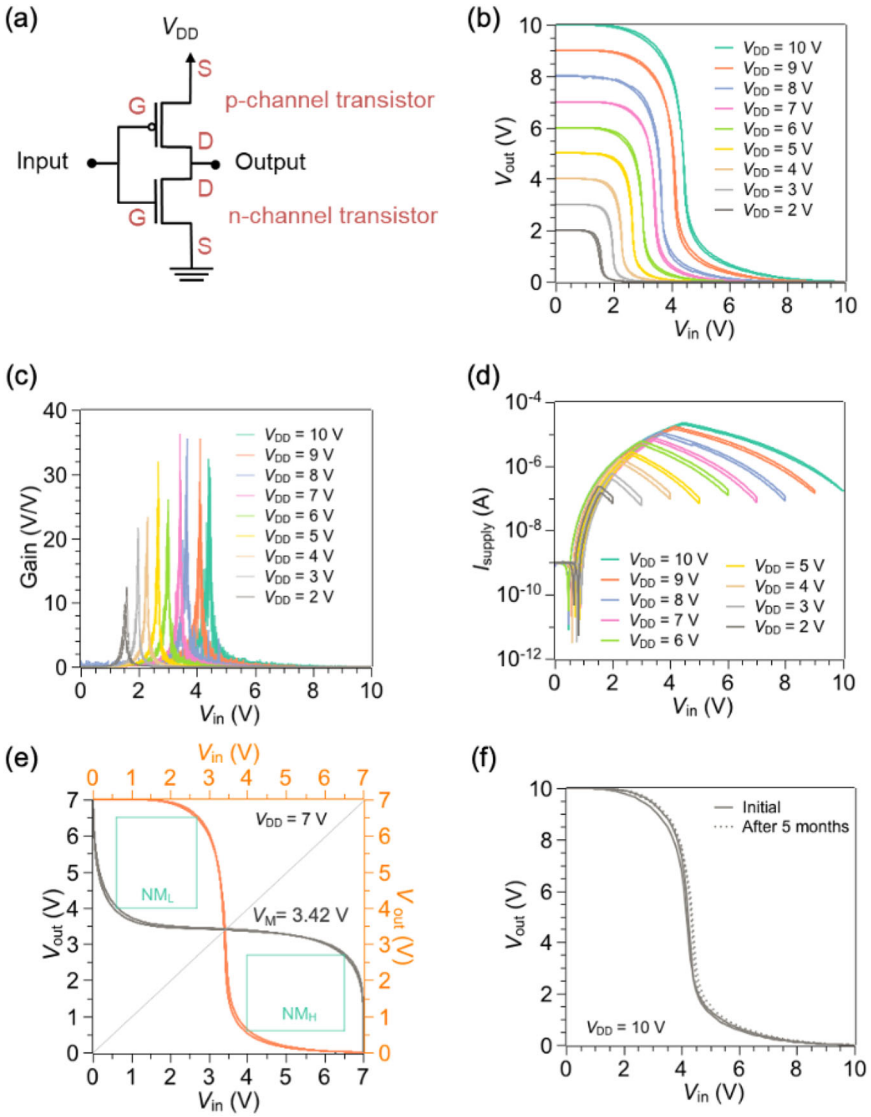

Fig. 3 Electrical performance of the hybrid complementary inverter. a Schematic diagram. **b** Voltage transfer curves (VTCs), **c** voltage gains, and **d** static current at $V_{DD} = 2$–10 V. **e** VTCs at $V_{DD} = 7$ V with noise margins represented by the green rectangles. $V_M = 3.42$ V, $NM_H = 2.5$ V, and $NM_L = 1.9$ V. **f** VTCs before and after exposure to air for 5 months ($V_{DD} = 10$ V).

oscillator. By measuring the operation frequency of the ring oscillator (f_{ROSC}), t_p can be calculated as shown in Eq. (4).

$$f_{ROSC} = \frac{1}{T} = \frac{1}{2nt_p} \quad (4)$$

Five-stage ring oscillators were fabricated by connecting five inverters in a loop to study the propagation delay of the hybrid inverter and the availability of more complex circuits. An optical micrograph of the as-fabricated ring oscillator is shown in Fig. 6a. In each stage, the dimensions were $W/L = 200$ μm/4 μm and $\Delta L = 3$ μm for the p-channel TFT and $W/L = 200$ μm/8 μm and $\Delta L = 1.5$ μm for the n-channel TFT, where ΔL is the gate overlap with each source and drain electrode. The electrical performance of the p- and n-channel TFTs recorded under these conditions is shown in Supplementary Fig. 7. The p-channel TFT exhibited μ_{lin} and μ_{sat}, I_{off}, and I_{on}/I_{off} ratio of 4.4 and 1.1 $cm^2 V^{-1} s^{-1}$, 10^{-13} A, and 10^8, respectively, while the corresponding values for the n-channel TFT were 1.6 and 1.9 $cm^2 V^{-1} s^{-1}$, 10^{-13} A, and 10^9 respectively. Note that, for the p-channel TFT, μ_{sat} value was smaller than μ_{lin} due to an early saturation phenomenon, which has been recently observed in the short-channel, single-crystal OSC-based TFTs and could be attributed to velocity saturation effect, thermal damage during depositing Au and/or the interface diode effect[49,50].

The VTC of a single inverter (Fig. 6b) suggests that even those inverters with short channel lengths exhibit a full rail-to-rail swing, symmetric transition of $V_M \sim 5$ V for both forward and backward voltage sweep, and a high noise margin with an NM_H of 3.2 V and NM_L of 2.9 V. The output signal from the five-stage ring oscillator at a V_{DD} of 10 V is shown in Fig. 6c. In this case, f_{ROSC} was 77 kHz and thus t_p was estimated to be 1.3 μs. We compared several complementary ring oscillators based on solution-processed OSCs or MOSs with respect to t_p (Table 1). As there are only a few studies on plastic substrates, ring oscillators fabricated on rigid substrates were also considered. Because f_{ROSC} is approximately proportional to V_{DD}[51], different devices were compared by converting V_{DD} to 10 V and the corresponding t_p after conversion is defined as $t_{p(10V)}$. Notably, the present $t_{p(10V)}$ lies among the smallest values achieved by solution-processed p- and n-type semiconductors, which underlines the advantage of hybrid complementary circuits based on single-crystal OSC and amorphous MOS. In addition, our circuits can work on flexible, plastic substrates, which is an

advantage beyond ref. [45] demonstrated using a glass substrate due to the necessity of an annealing process at 500 °C. As shown in Supplementary Fig. 8, the complementary ring oscillators with different dimensions were fabricated over the substrate. Considering f_{ROSC} with different TFT dimensions, f_{ROSC} in the current devices was principally dominated by L but subsequently by ΔL. Hence, the future task for increasing f_{ROSC} may include an improved technology of fine patterning, where the reduction of contact resistance should get required for advanced performances.

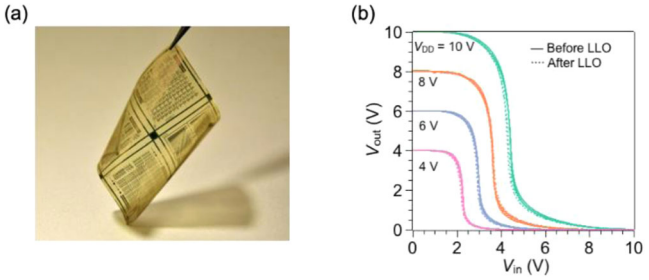

Fig. 4 Properties of the hybrid inverter before and after delamination from glass supports. a Photograph of the hybrid circuits on a free-standing PI film. **b** VTCs of the hybrid complementary inverter with p- and n-channel W/L values of 200 μm/9 μm and 200 μm/13 μm, respectively, before and after delamination.

Conclusion

We have demonstrated organic−inorganic hybrid complementary circuits on plastic substrates by using solution-processed, high-performance semiconductors: p-type C_9-DNBDT-NW single crystals and n-type amorphous IZO. Owing to their high carrier mobilities and air stability, the TFTs and the complementary inverters exhibited excellent electrical characteristics and long-term stability, and the five-stage complementary ring oscillator operated at 77 kHz with a supply voltage of 10 V in air, proving the likeliest approach to high-speed complementary circuits based on the solution-processed semiconductors. Although solution-processed amorphous MOSs are usually sensitive to chemical species such as water and organic solvents, the reliable integration of the OSC-

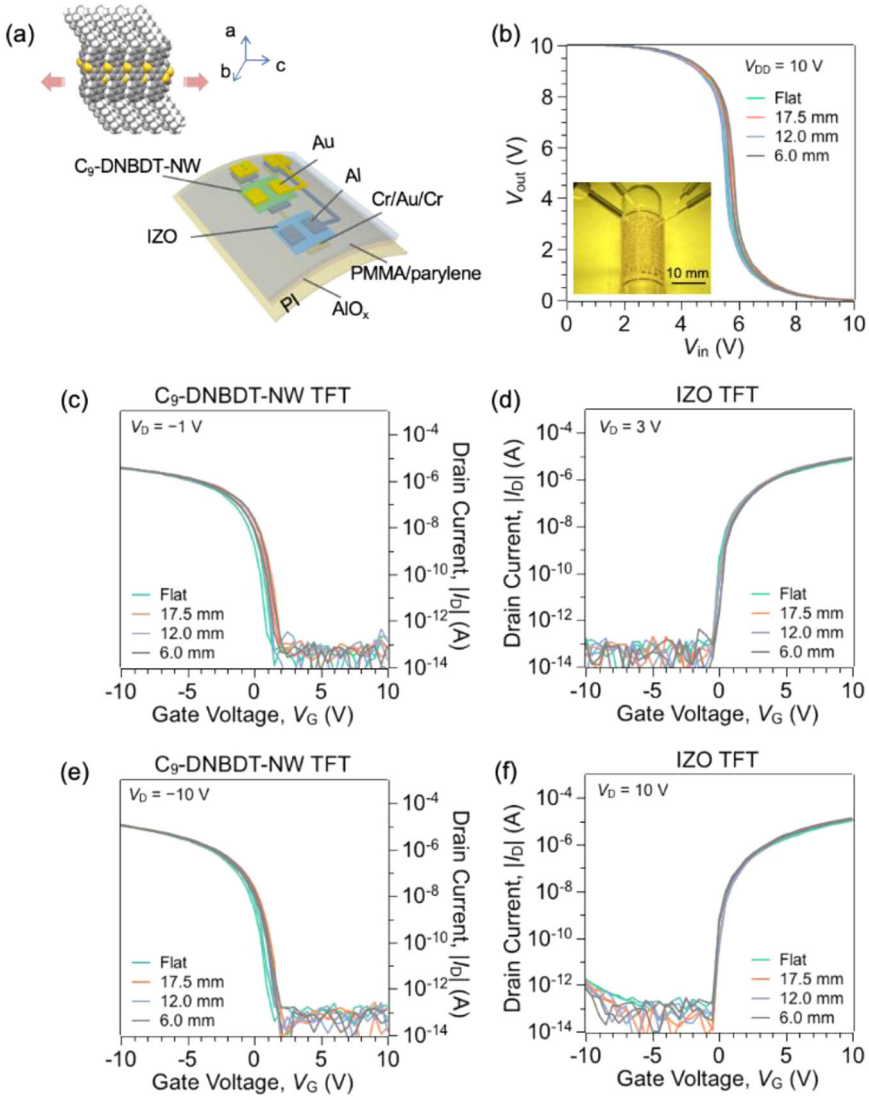

Fig. 5 Electrical performance of a hybrid complementary inverter under bending stress. a Schematic illustration of a device under bending stress. **b** VTCs of the inverter when flat and bent to tensile radii of 17.5, 12.0, and 6 mm. The inset shows the measurement setup with a bending radius of 6 mm. Transfer curves of TFTs based on (**c** and **d**) C_9-DNBDT-NW (W/L = 100 μm/19 μm) and (**e** and **f**) IZO (W/L = 50 μm/24 μm) in the linear and saturation regions under different bending stresses.

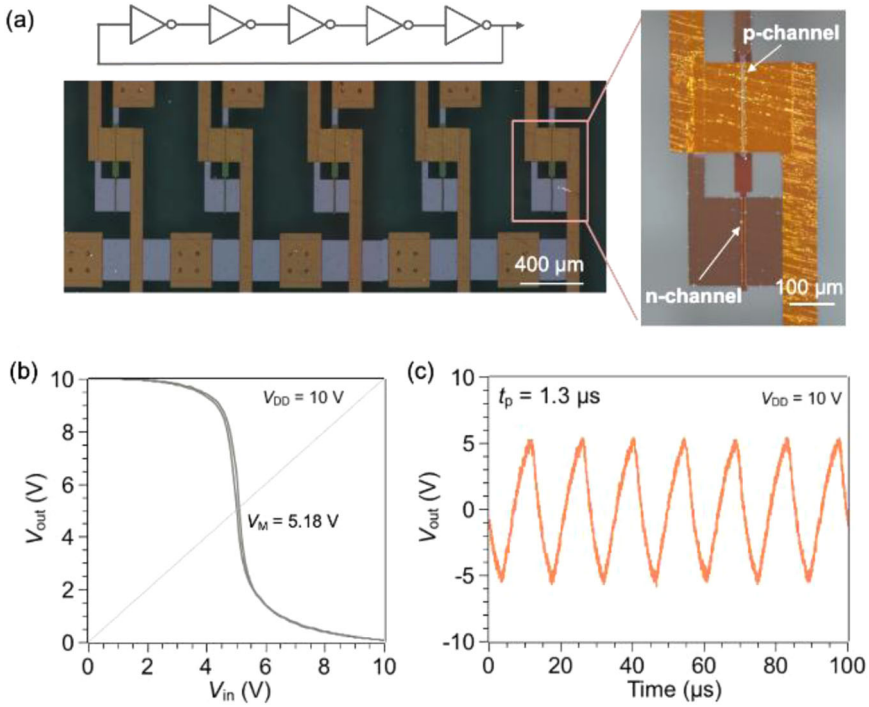

Fig. 6 Properties of a five-stage ring oscillator. a Optical micrograph of a hybrid ring oscillator. The magnified image shows one stage. $W/L = 200$ μm/4 μm and $\Delta L = 3$ μm for p-channel TFT and $W/L = 200$ μm/8 μm and $\Delta L = 1.5$ μm for n-channel TFT, where ΔL is the gate overlap. **b** VTCs of the hybrid inverter with $V_{DD} = 10$ V. **c** Output signal of the ring oscillator at $V_{DD} = 10$ V.

Table 1 Comparison of the stage-propagation delay in ring oscillators based on solution-processed MOSs and/or OSCs.

p-channel material	n-channel material	Substrate	Stage No.	L_p/L_n (μm)	V_{DD} (V)	f_{ROSC} (kHz)	t_p (μs)	$t_{p(10\ V)}$ (μs)	Ref.
C_9-DNBDT-NW	IZO	PI	5	4/8	10	77	1.3	1.3	This work
ActivInk P2100	ActivInk N2200	Glass or PEN	5	2/2	100	~50	2	20	22
C_{10}-DNBDT-NW	BASF GSID 104031-1	Glass	5	30/5	20	22	4.5	9	26
IDT-BT	IZO	Glass	3	5/5	10	3.2	52	52	35
IDT-BT	IZO	Glass	3	5/5	70	1250	0.13	0.93	35
P3HT	ZnO	Si	5	1/1	2	2.2	45	9	34
TIPS-pentacene	BASF GSID 104031-1	PET	5	70/70	100	0.134	746	7460	52
TIPS-PEN	ActivInk N3300	PEN	19	5/5	10	1.0	25	25	53
SWCNT	ZTO	Glass	5	4/4	8	714	0.14	0.11	45
ActivInk P2100	P(NDI2OD-T2)	PEN	5	5/5	10	10	10	10	54
DPPT-TT	P(NDI2OD-T2)	PEN	7	70/70	100	2	31	310	55
$P(T_0T_0TT_{16})$	P(NDI2OD-T2)	Glass	7	2.5/2.5	1.5	0.14	500	75	56
DiF-TES-ADT/PS	TU-3	Parylene	3	52/41	10	0.217	768	768	24
DiF-TES-ADT/PS	TU-3/PαMS	Glass	5	10/10	10	1.465	68.2	68.2	57
MOP-01	TU-3/PαMS	Glass	5	60/55	10	0.09	1065	1065	58

Stage No. stage number, L_p/L_n channel lengths for n-channel TFT and p-channel TFT, V_{DD} supply voltage, f_{ROSC} frequency of ring oscillator, t_p stage propagation delay, $t_{p(10\ V)}$ stage propagation delay at $V_{DD} = 10$ V or converted V_{DD} to 10 V.

based TFTs with the pre-fabricated MOS-based TFTs shown in this paper can be attributed to the following materials viewpoints: (1) An effective protection bilayer for IZO based on a PMMA underlayer, which is solution-processable at low temperature and chemically harmless for IZO, and acts as a barrier of the undesired reaction between IZO and the diradical parylene intermediate during the formation of upper layer; (2) Water-based transferring integration of solution-coated OSC thin films with the pre-fabricated IZO-based TFTs with the help of hydrophobic parylene layer; (3) Damage-free photolithographic processes using the dry-film, photoacid-free photoresist. The scalability of current solution-coating methods can promise further developments of the high-speed complementary circuits for IoT applications, where it is required to reduce the contact resistance and to minimise the channel dimensions and capacitive parasitism, which needs the help of materials science.

Methods

Substrate preparation. All the devices used in this study were fabricated on PI substrates. The PI substrate was prepared by spin-coating polyamic acid (Ube Industries, Ltd.) on a glass supporter (5×5 cm^2) at 2000 rpm for 3 min, followed by thermal curing at 110 °C for 60 min, 150 °C for 30 min, 200 °C for 10 min, 250 °C for 10 min, and 430 °C for 10 min on a hot plate in the air. The PI film was attached to a glass support during fabrication and delaminated using an LLO technique to achieve free-standing films for flexibility evaluation.

Fabrication of n-channel TFTs based on IZO. IZO films were fabricated using a sol-gel method. Initially, In and Zn precursor solutions (0.1 M) were prepared by adding $In(NO_3)_3{\cdot}xH_2O$ (Aldrich) and $Zn(NO_3)_2{\cdot}xH_2O$ (Aldrich) to 2-methoxyethanol, respectively, and stirring at room temperature in the air for more than 6 h. The IZO precursor was then prepared by mixing the In and Zn precursors at an In/Zn ratio of 3/2 and stirring under the conditions described above.

Both n- and p-channel TFTs exhibit a bottom-gate top-contact structure. Gate patterns of IZO-based TFTs were formed by photolithography with a photoresist (TLOR, Tokyo Ohka Kogyo Co., Ltd.). Cr/Au/Cr (5/25/5 nm) was deposited via thermal evaporation, followed by a lift-off process. An AlO_x gate dielectric layer was formed by ALD. Before IZO deposition, the substrate was treated with a UV ozone cleaner (Filgen, Inc., UV253H) for 10 min to remove any organic residues and improve its wettability. The IZO precursor was then spin-coated on the substrate at 500 rpm for 5 s and 5000 rpm for 30 s, followed by soft baking at 150 °C for 5 min and hard baking at 370 °C for 1 h under ambient conditions. The IZO film was patterned with a PDM (Taiyo Ink Mgf. Co., Ltd.), and etched with oxalic acid. S/D electrodes for IZO-based TFTs and gate electrodes for C_9-DNBDT-NW-based TFTs (Al, 45 nm) were deposited by thermal evaporation and patterned by a lift-off process based on PDM[38].

Fabrication of p-channel TFTs based on C_9-DNBDT-NW. After the fabrication of n-channel TFTs, a PMMA/parylene bilayer was fabricated to act as a passivation layer for n-channel TFTs and it doubled as a gate dielectric for p-channel TFTs. The PMMA layer was formed by spin coating a PMMA solution (Mw = 120,000, 0.56 wt.% in butyl acetate) at 500 rpm for 5 s and then 4000 rpm for 30 s, followed by soft baking at 150 °C for 1 h. The parylene layer was deposited by chemical vapour deposition.

C_9-DNBDT-NW was synthesised and purified in-house; initially, a C_9-DNBDT-NW solution was prepared by dissolving 0.02 wt.% C_9-DNBDT-NW in 3-chlorothiophene. The C_9-DNBDT-NW single-crystal layer was once formed by continuous edge casting on a super hydrophilic substrate and then transferred to the top of the PMMA/parylene dielectric layer. More details can be found in our previous reports[7,40,41].

Fine patterns of OSC and Au S/D electrodes were achieved by a two-step patterning process based on a dry film resist with a thickness of 5 µm (PDM, Taiyo Ink Mfg. Co., Ltd.)[42,43]. This process is illustrated schematically in Supplementary Figure 9. A PMMA layer (Mw = 120,000, 5 wt.% in butyl acetate) was formed by spin coating at 500 rpm for 5 s and 1000 rpm for 30 s, followed by baking at 80 °C for 10 min before being laminated with a PDM dry film. The PDM layer was patterned by photolithography and PMMA was patterned using O_2 plasma with patterned PDM as a mask. After etching the OSC or S/D electrodes, PMMA and PDM were stripped together with acetonitrile. For OSC patterning, Au (30 nm) was deposited via thermal evaporation on the entire surface and it acted as a protection layer as well as S/D electrodes. Subsequently, a two-step photolithography process was conducted. Au was etched using an AURUM S-50790 (Kanto Chemical Co. Inc.) instrument and the OSC layer was etched using O_2 plasma. Subsequently, a solid-state laser (Delphi Laser, Inducer-6001-P, 355 nm) was used to create holes in the gate dielectrics for bottom electrodes. Next, Au (60 nm) was deposited by thermal evaporation and patterned by two-step photolithography to form S/D electrodes and conduction terminals for the bottom electrodes. Finally, the substrate was annealed at 110 °C for 1 h to remove the solvent used during fabrication.

Device characterisation. The electrical properties of the fabricated hybrid inverters were measured under ambient and dark conditions. The static properties of the TFTs and the VTCs of the inverters were measured using a semiconductor parameter analyser (Keithley, 4200-SCS). The output signals of the ring oscillators were recorded using an oscilloscope (Tektronix, MDO3014). Micrographs of the complementary inverter and ring oscillator were acquired using an optical microscope. An FIB-SEM (JEOL, JIB-4700F) was used to observe the edge conditions of the gate electrodes in p-channel TFTs.

Carrier mobility (μ) and V_{th} were determined by measuring the dependence of drain current (I_D) on V_G and fitting with the following equations.

In the linear region,

$$I_D = \frac{\mu_{lin} W C_i}{L} V_D (V_G - V_{th}) \quad (5)$$

In the saturation region,

$$I_D = \frac{\mu_{sat} W C_i}{2L} (V_G - V_{th})^2 \quad (6)$$

C_i is determined by capacitance–voltage measurements at 10 kHz. The values of C_i for the ring oscillators used in this study were 88.5 nF cm^{-2} for n-channel (AlO_x, 80 nm) and 13.2 nF cm^{-2} for p-channel (PMMA, ~10 nm; parylene, ~190 nm); for inverters discussed in other parts (excepted the ring oscillators, Fig. 6 and Supplementary Figs. 7–8) 122.5 nF cm^{-2} for n-channel (AlO_x, 63 nm) and 22.1 nF cm^{-2} for p-channel (PMMA, ~10 nm; parylene, ~120 nm).

Data availability

All the data are available within this article and its Supplementary Information, as well as from the corresponding author upon request.

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Author contributions

J.T. and S.W. conceived the study. X.W. designed the integration process, carried out device fabrication, characterisation studies and the related data analysis, and wrote the first draft. S. K. contributed to the process design and data analysis of metal-oxide semiconductors and the passivation process. T.M. contributed to the fabrication and patterning of organic semiconductors. K.T. discussed the IZO preparation process. A.Y. and M.S. contributed to the design of complementary circuits. All authors analysed and interpreted the data and wrote the manuscript.

Competing interests

S.W. is an Editorial Board Member for *Communications Materials* and was not involved in the editorial review, or the decision to publish, this Article. All the other authors have no competing interests to declare.

Additional information

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