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Gate-switchable rectification in isotype van der Waals heterostructure of multilayer $MoTe_2/SnS_2$ with large band offsets

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Despite intensive studies on van der Waals heterostructures based on two-dimensional layered materials, isotype vdW heterojunctions, which consist of two different semiconductors with the same majority carrier, have received little attention. We demonstrate an n–n isotype field-effect heterojunction device composed of multilayer moly ditelluride ($MoTe_2$) and tin disulfide (SnS_2). The carrier transport flowing through the n-$MoTe_2$/n-SnS_2 heterojunction exhibits a clear rectifying behavior exceeding 10^3, even at a moderate source–drain voltage of 1 V in ambient environment. Owing to the large band offsets between the two materials, a potential barrier exceeding ~1 eV is formed, which is verified by comparing a numerical solution of Poisson's equation and experimental data. In contrast to the conventional p–n heterostructure operating by diffusion of the minority carrier, we identify the carrier transport is governed by the majority carrier via the thermionic emission and tunneling-mediated process through the potential barrier. Furthermore, the gate voltage can completely turn off the device and even enhance the rectification. A ternary inverter based on the isotype $MoTe_2/SnS_2$ heterojunction and a SnS_2 channel transistor is demonstrated for potential multivalued logic applications. Our results suggest that the isotype vdW heterojunction will become an able candidate for electronic or optoelectronic devices after suitable band engineering and design optimization.

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INTRODUCTION

Van der Waals (vdW) heterostructures based on two-dimensional (2D) layered materials have been extensively studied owing to its enormous combinations of selectable materials and excellent semiconducting properties. These structures have replaced conventional group IV- or III–V-based materials for applications in electronics and related fields[1–4]. Weak vdW interactions between individual layers and the absence of dangling bonds at the interfaces make it possible to fabricate high-performance devices[5–9]. On the one hand, unisotype vdW heterostructures, namely p–n junction, have only been studied as a building block for diodes or optoelectronic devices with distinct current rectification, gate-tunable polarity behavior, negative differential resistance from the band-to-band tunneling, and photovoltaic effect[10–21]. While there are a variety of choices for n-type vdW materials, there are few natural p-type vdW materials such as black phosphorus[10–15] and WSe_2[7,16–21].

On the other hand, there are few published research works on isotype vdW heterojunction, in which the transport dominated by the same majority carriers in both components. For optoelectronic device, photodetectors made of isotype vdW heterojunctions with WS_2 and MoS_2 were recently reported[22,23]. One of the reasons why isotype heterojunction is not considered for electronic devices is that it has a smaller expected rectifying response than p–n heterojunctions. However, the lack of natural p-type vdW materials has shifted the focus of researchers toward isotype vdW heterojunctions, especially n–n type, because there are enormous candidate materials.

In this study, an isotype heterojunction device combined with a multilayer moly ditelluride ($MoTe_2$) and tin disulfide (SnS_2) is demonstrated. The transistor is fabricated by exfoliating each material and stacking them by the polydimethylpolysiloxane (PDMS) dry transfer method on a Si/SiO_2 (300 nm) substrate (see the details in the Methods section)[24]. The transport properties of individual SnS_2 and $MoTe_2$ channels were measured. It was confirmed that the conductivity of SnS_2 is n type, regardless of its thickness, and $MoTe_2$ exhibits n-type behavior for a thick flake. SnS_2 has a large electron affinity (~5.2 eV) and bandgap (~2.2 eV) in the bulk phase[25], which can form distinct band alignments when combined with other transition metal dichalcogenide (TMD) groups[26–28]. $MoTe_2$, however, has a smaller electron affinity (~3.8 eV) and smaller bandgap (~0.9 eV)[27]. Therefore, a large band offset and a large built-in potential barrier at the heterojunction between $MoTe_2$ and SnS_2 is expected to form. In addition, we measured the Raman spectroscopy of the vdW heterojunction and confirmed the electron transfer from $MoTe_2$ to SnS_2 side according to Anderson's rule.

As a result, the electrical measurement of the $MoTe_2/SnS_2$ heterojunction device clearly exhibits rectification. From the systematic analysis of carrier transport, based on a numerical solution of Poisson's equation and Simmons approximation, we ascribe the rectifying behavior to the large band offsets between the two materials, which creates a large potential barrier at the heterojunction. In addition, we certify the switchable rectification characteristic by varying the gate voltage with a maximum rectification ratio of ~10^3, at a modestly low source–drain voltage of 1 V and in ambient environment (room temperature of 300 K). This value is comparable with that of other p–n unisotype vdW

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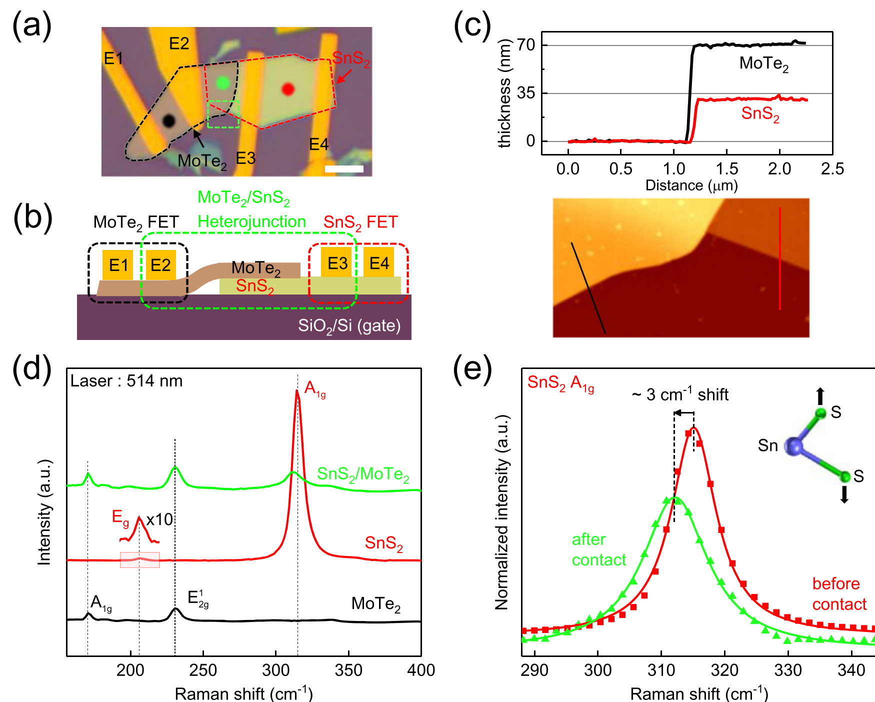

Fig. 1 Heterojunction device structure and Raman spectrum evaluation. **a** The optical image and **b** the schematic side view of the $MoTe_2$/SnS_2 heterojunction device, respectively. The scale bar used is 10 μm. E1 and E2 (E3 and E4) are the electrodes to measure the electrical properties of $MoTe_2$ (SnS_2) individual channels and E2–E3 is for the heterojunction channel. **c** Topographic image for the green dashed box in the optical images, and the respective height profiles. **d** Raman spectra of the samples at different positions. **e** Raman shift in the SnS_2 A_{1g} peak after heterojunction formation.

heterostructure devices from previous reports[17,23,29,30]. Finally, we demonstrate a ternary inverter using the $MoTe_2$/SnS_2 heterojunction and a SnS_2 channel transistor. We emphasize that this is the first experimental study reporting a systematical analysis of the $MoTe_2$/SnS_2 heterojunction device.

RESULTS

Device structure and Raman spectrum of the heterojunction

Figure 1a shows the microscopic image of the multilayer $MoTe_2$/SnS_2 heterojunction device with four Ti/Au electrodes. Figure 1b is the schematic side view of the fabricated device. The four electrodes are used to compare the individual channel and heterojunction channel in a single device, i.e., the electronic properties of $MoTe_2$, SnS_2, and $MoTe_2$/SnS_2 heterojunctions can be examined using electrodes E1–E2, E3–E4, and E2–E3, respectively. Figure 1c shows the atomic force microscope (AFM) image for the green dashed box in Fig. 1a. From the topographic image and the respective height profiles (represented by solid black and red lines), the thicknesses of SnS_2 and $MoTe_2$ are approximately 30 and 70 nm, respectively.

The Raman scattering measurement was performed on different channel areas of the fabricated device. The measured areas were marked with the black ($MoTe_2$), red (SnS_2). and green dots (heterojunction) in Fig. 1a, and each Raman spectrum is shown in Fig. 1d, respectively. We used a 514-nm green laser as the excitation source. On the $MoTe_2$ region (black line), two peaks appear near 171 and 230 cm^{-1}, corresponding to the respective out-of-plane A_{1g} and in-plane E^1_{2g} phonon modes. The bulk inactive B^1_{2g} phonon mode around 290 cm^{-1} is not observed in our $MoTe_2$ thick flake (Supplementary Fig. 1), which agrees with the previously reported observations[31–33]. The spectrum in the SnS_2 region (red line) shows a prominent peak of the A_{1g} mode at ~315 cm^{-1} and a weaker peak of the E_g mode near 206 cm^{-1}, which are also consistent with previous results[34,35]. In the heterojunction region (green), the peaks receive contributions from both $MoTe_2$ and SnS_2, indicating the existence of two distinct materials. Especially, a significant reduction of the SnS_2 Raman peak intensity was observed due to the thick $MoTe_2$ flake (~70 nm) placed on the SnS_2 flake. This, in turn, led to the feeble peak of E_g that is indistinguishable in the overlapped region. In addition, we observe a redshift of ~3 cm^{-1} in the out-of-plane mode (A_{1g}), owing to the phonon softening caused by the electron transfer from $MoTe_2$ to SnS_2[36]. The electron affinity rule (Anderson's rule) accounts for this electron transfer.

Electrical characteristics and the band alignment

Figure 2a, b shows the transfer characteristics of individual $MoTe_2$ and SnS_2 channel FET with electrodes E1–E2 and E3–E4, respectively. A back-gate voltage (V_g) was applied to the heavily n-doped (As dopants) Si substrate with a resistivity of ~0.005 Ω cm. All electronic measurements were carried out under ambient conditions (room temperature of 300 K). The observed linear output curves at different gate voltages for both $MoTe_2$ and SnS_2 FETs in the inset of Fig. 2a, b suggest the sufficiently low contact resistances between Ti/Au metal electrodes and both materials[37,38]. At the source–drain voltage (V_{ds}) of 1 V, n-type dominant ambipolar behavior was observed for the bulk $MoTe_2$[38–41]. We checked the low gate leakage current through SiO_2—300-nm thick—in tens of picoampere level for whole gate voltage ranges as shown in Supplementary Fig. 2. Specifically, $MoTe_2$ FET exhibited ambipolar behavior for an intermediate flake and p-type behavior for a thin flake, as shown in Supplementary Fig. 2. This dependence of change in conductivity on the thickness has been reported in previous studies as well[42,43]. For SnS_2, a typical n-type unipolar was observed[37,44–46]. It is noteworthy that we achieved sufficiently high on/off ratios (~10^5) in both FETs with thick flakes even though they operate in the depletion-mode, i.e., a negative gate voltage for an n-channel transistor is required to turn off the device. Usually, the on/off ratio in a depletion-mode

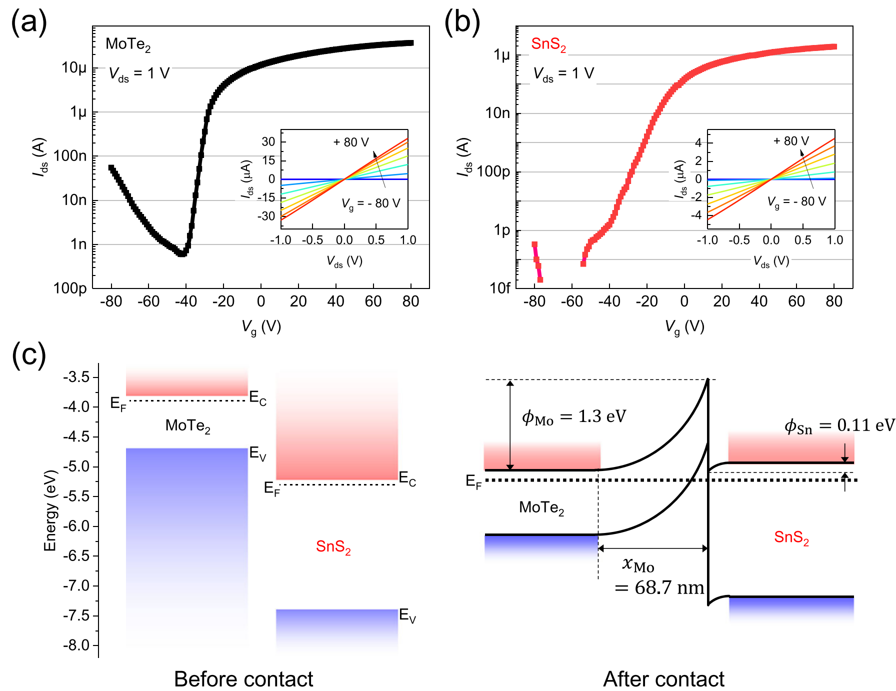

Fig. 2 Electrical characteristics of each device and band diagrams before and after contact. The transfer characteristics of **a** $MoTe_2$ and **b** SnS_2 FETs at $V_{ds} = 1$ V. The insets are the output curves at different gate voltages in the range of −80 to 80 V at steps of 10 V. **c** Energy band alignment of $MoTe_2/SnS_2$ heterojunction before and after contact.

transistor limits the thickness of the channel material, because the gating field weakens gradually, or even entirely lost, as the distance between the gate oxide surface and the channel increases[47]. In other words, a large leakage current flows through the expanding undepleted parts as the channel thickness increases, leading to a poor on/off ratio. In this respect, the high on/off ratio in our devices implies that the carriers in the channel can be fully depleted under the given gate voltage. Especially, a very high on/off ratio reaching 10^7 in the SnS_2 FET was achieved even with a thick flake (~30 nm), as shown in Fig. 2a. This result can be attributed to the larger bandgap of bulk SnS_2 (~2.2 eV) than that of the other TMDs[48]. The small bandgap of bulk $MoTe_2$ (~0.9 eV) accounts for the relatively high off-state current of $MoTe_2$ FET.

Figure 2c shows the band alignment of the $MoTe_2/SnS_2$ heterojunction before and after contact. The conduction band minimum (E_c) and valence band maximum (E_v) values of $MoTe_2$ (SnS_2) were previously reported to be 3.8 eV (5.2 eV) and 4.7 eV (7.4 eV), respectively[26–28]. A very large conduction band offset (ΔE_c) and valence band offset (ΔE_v) of approximately 1.4 and 2.7 eV are achieved between $MoTe_2$ and SnS_2, respectively, compared with other combinations of 2D materials. Majority carrier concentrations per unit area for the respective channels (electron for both materials) at $V_g = 0$ V are estimated by[16], $n_{MoTe_2}(n_{SnS_2}) = \frac{C_{ox}|V_{th}-V_g|}{q} = 2.16\times10^{12}(3.59\times10^{11})\mathrm{cm}^{-2}$, where $q = 1.6\times10^{-19}$C and $C_{ox} = 1.15\times10^{-8}\mathrm{F/cm^2}$ is the capacitance per unit area of the 300-nm-thick SiO_2 gate oxide layer. The threshold voltage (V_{th}) is extracted based on the extrapolation in the linear region method, which finds the gate-voltage axis intercept of the linear extrapolation of transfer curves at the first maximum point of transconductance[49]. The values are −30 and −5 V for $MoTe_2$ and SnS_2 FET, respectively, as shown in Supplementary Fig. 3. We treated both $MoTe_2$ and SnS_2 as nondegenerate semiconductors, to simplify the calculations.

Thus, the Fermi level position was estimated using $n^* = \int_{E_c}^{\infty} f(E)N(E)dE \cong N_c \exp\left(\frac{E_F-E_c}{k_BT}\right)$, where n^* is the number of electrons per unit volume, N_c is the effective density of states in the conduction band, k_B is the Boltzmann constant (1.38×10^{-23} J/K), and T is the temperature (300 K, in this case)[50]. Note that the channels in our devices were completely depleted under given gate voltages, which means the number of unit volumes can be simply calculated by dividing the carrier concentration obtained above by the material thickness ($t_{MoTe2} = 70$ nm, $t_{SnS2} = 30$ nm); $n^*_{MoTe2} = 3.07\times10^{17}\,\mathrm{cm}^{-3}$ and $n^*_{SnS2} = 1.2\times10^{17}\,\mathrm{cm}^{-3}$. N_c is equal to $2\left(\frac{2\pi m^* k_BT}{h^2}\right)^{3/2}$, where m^* is the effective mass of the electron (0.55 m_0 for $MoTe_2$ and 0.43 m_0 for SnS_2)[51–53] and h is the Planck constant (6.63×10^{-34} Js), giving N_c of 1.02×10^{19} and $7.08\times10^{18}\,\mathrm{cm}^{-3}$ for $MoTe_2$ and SnS_2, respectively. Consequently, the difference between the conduction band edge and Fermi level (E_F–E_c) were calculated to be 0.09 eV for $MoTe_2$ and 0.1 eV for SnS_2. From this, the work functions were 3.89 eV (5.3 eV) for $MoTe_2$ (SnS_2).

From these band structures, the predicted band alignments of the heterojunction when these two materials were in contact were schematically described. The smaller work function of $MoTe_2$ allows the electrons in the $MoTe_2$ side to spill over to the SnS_2 side until thermal equilibrium is established, forming a depletion region on the $MoTe_2$ side and an accumulation region on the SnS_2 side. This phenomenon is consistent with the Raman analysis in Fig. 1e. Thus, band bending occurs at the heterojunction, which yields the built-in potential ϕ_{Mo} and ϕ_{Sn} on the $MoTe_2$ and SnS_2 sides, respectively. The total built-in potential (V_{bi}) must be equal to the sum of the potential drops on the two sides ($V_{bi} = \phi_{Mo} + \phi_{Sn}$). It can be calculated from the work function difference between the two materials (~1.41 eV), since the Fermi level is constant and flat throughout the heterojunction at equilibrium. It is worth mentioning that ours is an isotype heterojunction, which is different from the conventional p–n junction heterostructures[15,17,22]. Therefore, the depletion region width on the $MoTe_2$

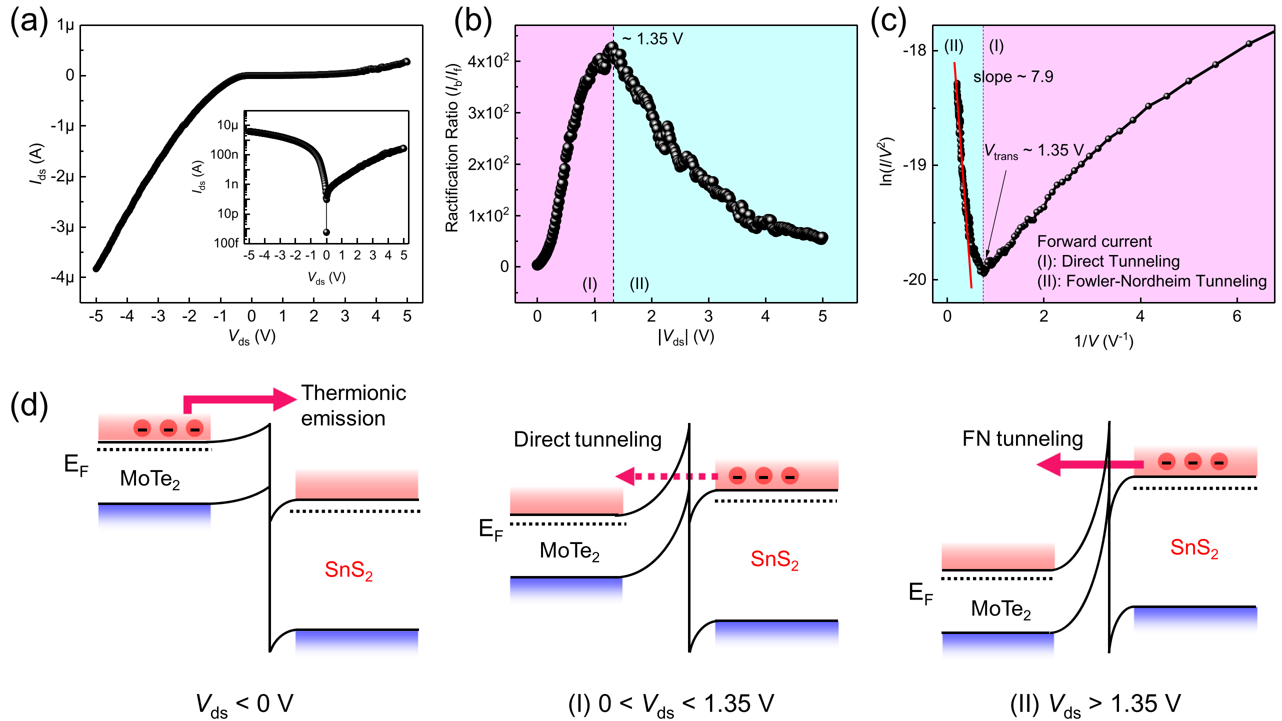

Fig. 3 Investigation on the rectification of the MoTe2/SnS2 heterojunction device. **a** Output characteristic of the $MoTe_2/SnS_2$ heterojunction device. The inset shows the logarithmic scale of the output curve. **b** Rectification ratio, defined by I_b/I_f at the same V_{ds}, with the increasing magnitude of V_{ds}. **c** Fowler–Nordheim plot. **d** Energy band diagrams of the heterojunction at different V_{ds}.

side can be calculated by the following equations[54]:

$$V_{bi} = \phi_{Mo} + \phi_{Sn} = \frac{qN_{d,Mo}x_{Mo}^2}{2\varepsilon_{Mo}} + \phi_{Sn}, \tag{1}$$

$$\sqrt{2\varepsilon_{Sn}N_{d,Sn}k_BT}\sqrt{\left(\exp\left(\frac{q\phi_{Sn}}{k_BT}\right) - 1\right) - \frac{q\phi_{Sn}}{k_BT}} = qN_{d,Mo}x_{Mo}, \tag{2}$$

where $N_{d,Mo} \approx 3.1 \times 10^{17}$ cm^{-3} and $N_{d,Sn} \approx 1.2 \times 10^{17}$ cm^{-3}, calculated by $N_{d,Mo(Sn)} = n_{Mo(Sn)}/t_{Mo(Sn)}$, from the electron majority carrier concentrations and thicknesses of each material. $\varepsilon_{Mo} = 10.1$ and $\varepsilon_{Sn} = 17.7$ are the dielectric constants of $MoTe_2$ and SnS_2, respectively[55,56]. Eqs. (1) and (2) can be solved for ϕ_{Sn}, ϕ_{Mo}, and x_{Mo}. Consequently, we obtained $\phi_{Mo} = 1.3$ eV, $\phi_{Sn} = 0.11$ eV, and $x_{Mo} = 68.7$ nm, as shown in Fig. 2c. This depletion region width is almost similar with the thickness of $MoTe_2$ (70 nm), implying that the $MoTe_2$ layer may be fully depleted after contact with SnS_2 at equilibrium. The barrier height value of 1.31 eV will be used to identify the transport behavior of the junction. We note that the energy band alignment of this device is also similar to that in the previous report, where the band alignment was determined by the combination of X-ray photoemission spectroscopy and ultraviolet photoelectron spectroscopy measurements[28].

Transport mechanism through the heterojunction

To examine the carrier transport through the $MoTe_2/SnS_2$ heterojunction at $V_g = 0$ V, a V_{ds} of up to 5 V was applied to the electrode on the $MoTe_2$ side (E2), and the electrode on SnS_2 (E3) was grounded. The forward (I_f) and backward currents (I_b) are defined as arising when the positive and negative voltages are applied to E2, respectively. As shown in Fig. 3a, the backward current increased rapidly up to a few microamperes with V_{ds}, and the forward current increased only up to a few hundreds of nanoamperes even at high V_{ds}, showing a clear rectifying characteristic. We confirmed the same trend with the other devices, which also exhibited good rectification behavior (Supplementary Fig. 4). The rectification ratio with different V_{ds}, defined as I_b/I_f at the same V_{ds}, is illustrated in Fig. 3b. The ratio behaves significantly differently across $V_{ds} = 1.35$ V. In the small V_{ds} range represented by region (I), the rectification ratio increases until a maximum value of ~4×10^2. It then decreases in region (II), where V_{ds} is larger than 1.35 V. This transitional behavior implies our device has two different transport mechanisms.

We further investigated the transport of forward current using the Simmons approximation[54] to figure out the rectification behavior and found out two distinctive transport mechanisms can explain our device's transport property[57]. Direct tunneling (DT) and Fowler–Nordheim tunneling (FNT) can be expressed by the following relations:

$$I_{DT} \propto V \exp\left(-\frac{4\pi d\sqrt{2m^*\phi}}{h}\right), \tag{3}$$

$$I_{FNT} \propto V^2 \exp\left(-\frac{8\pi d\sqrt{2m^*\phi^3}}{3hqV}\right), \tag{4}$$

where ϕ is the barrier height, d is the tunneling barrier width, h is the reduced Plank constant, and m^* is the effective mass of an electron. With the above equations, we draw the Fowler–Nordheim plot, i.e., $\ln(I/V^2)$ vs. $1/V$ plot, as shown in Fig. 3c. This plot clearly shows the transition from a logarithmic regime at small V_{ds} for DT to a linear regime with a negative slope at high V_{ds} for FNT, representing region I (pink) and region II (blue), respectively. The transition voltage (V_{trans}) of 1.35 V is consistent with the voltage at which RR begins to decrease, indicating that the increased forward current via FNT gave rise to the decrease of the rectification ratio. Moreover, V_{trans} corresponds to ϕ/q, yielding the tunneling barrier height of ~1.35 eV. This value is analogous with the value of $\phi_{Mo} = 1.3$ eV in the previous band diagram analysis. With the slope in the linear regime, $\frac{8\pi d\sqrt{2m^*\phi^3}}{3hq} = 7.9$, where $m^* = 0.43\,m_0$ is the effective mass of electron in SnS_2[51,52], we obtained $d \approx 1.12$ nm.

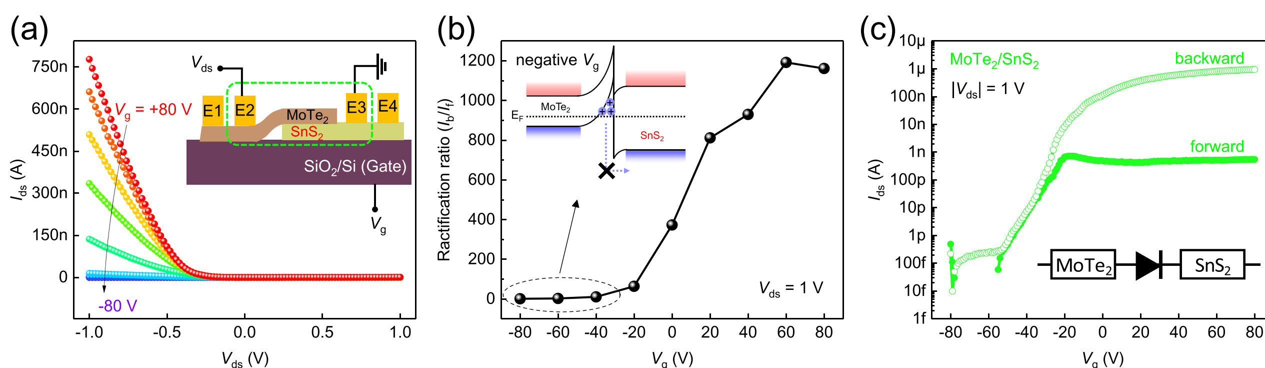

Fig. 4 Gate-voltage dependence of the heterojunction device. **a** Gate dependence of output characteristics of the $MoTe_2/SnS_2$ heterojunction in the range −1 to 1 V. The inset shows the schematic for the electrical measurement on the heterojunction. V_{ds} is applied to E2, which is in contact with $MoTe_2$, and E3, which is in contact with SnS_2, is grounded. **b** Rectification ratio under different gate voltages at $V_{ds} = 1$ V. The inset represents the band alignment at negative voltages. **c** Transfer characteristics of the heterojunction at $|V_{ds}| = 1$ V.

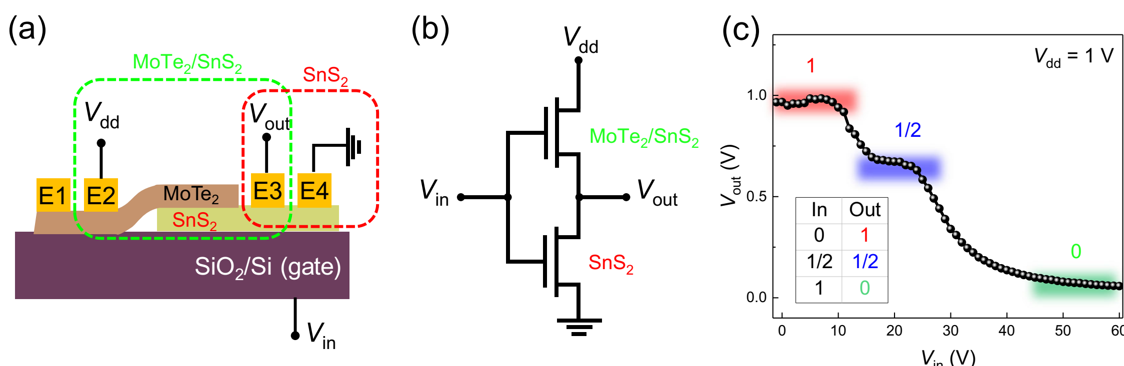

Fig. 5 Application for the ternary inverter. **a** Schematic of the measurement setup for the ternary inverter. V_{dd}, V_{out}, and V_{in} are applied to E2 on $MoTe_2$, E3 on SnS_2, and the back-gate electrode. E4 is grounded. **b** An analog circuit diagram. **c** V_{out} as a function of V_{in} for $V_{dd} = 1$ V.

From these results, the band diagrams of Fig. 3d are used to explain the rectification behavior. Note that only the electron carrier transport is considered because the electron is the majority carrier for both materials. When a negative voltage is applied to the $MoTe_2$ side ($V_{ds} < 0$ V), the electron is transferred from the $MoTe_2$ to the SnS_2 side will face the much lower barrier height or even no barrier at high negative voltages. As a result, the electrons easily contribute to the current by overcoming the potential barrier, even with the small thermal energy via thermionic emission. This results in the rapidly increasing backward current. In contrast, in the range of $0 < V_{ds} < 1.35$ V, the electrons in the SnS_2 side confront the built-in potential barrier, whose height is determined from the conduction band offset between $MoTe_2$ and SnS_2. This barrier blocks the electron transfer from the SnS_2 side to the $MoTe_2$ side, so that the current could be achieved purely by direct tunneling through the trapezoidal barrier. This current is lower than the backward current, causing the rectification property. However, for $V_{ds} > 1.35$ V, the potential barrier becomes narrower, more triangular as shown in Fig. 3d. Consequently, the increased forward current via the FNT reduces the rectification ratio.

Next, we examine the output curves of $MoTe_2/SnS_2$ heterojunction at different gate voltages from −80 to 80 V in steps of 20 V, as shown in Fig. 4a. The simple measurement schematic is in the inset of Fig. 4a. The output curves of the heterojunction device illustrate the gate-tunable rectification behavior. The backward current was decreased as V_g was changed toward negative values, so that the rectification property became imperceptible. Indeed, the rectification ratio at $V_{ds} = 1$ V was less than 10 for $V_g < -20$ V, as shown in Fig. 4b. Notably, the ratio reached up to ~10^3 in a positive V_g range. This value is more than twice the value at $V_g = 0$ V.

To inspect these gate-tunable rectification properties, the corresponding transfer characteristics of the $MoTe_2/SnS_2$ heterojunction device are summarized in Fig. 4c. The transfer curve of the heterojunction on the backward current (green open circle) follows a similar trend with that of SnS_2. The curve on the forward current (green closed circle) also follows that of SnS_2 for $V_g < -20$ V. However, the current variation for $V_g > -20$ V with increasing V_g is negligible, yielding consistent gate-tunable rectification properties. From the transfer curves of the $MoTe_2$ and SnS_2 FET, SnS_2 channel will turn off for $V_g < -20$ V, implying that there are no carriers, and the majority carrier in $MoTe_2$ will change from electron to hole in the negative gate-voltage range. The relevant band diagram is illustrated in the inset of Fig. 4b. In this band diagram, when the negative V_{ds} is applied to the $MoTe_2$ side, the current flow of hole carriers from SnS_2 to $MoTe_2$ would be very low because the SnS_2 channel is depleted. In addition, the majority hole carriers flowing from $MoTe_2$ to SnS_2 upon application of positive V_{ds} to $MoTe_2$ face a large potential barrier caused by the large valence band offset (Supplementary Fig. 5). Consequently, both forward and backward currents are very low for $V_g < -20$ V, suppressing the rectification behavior. In this manner, this device can be viewed as a series connection of $MoTe_2/SnS_2$ heterojunction and two resistors of $MoTe_2$ and SnS_2, whose resistance values can be adjusted by controlling V_g. Note the $MoTe_2/SnS_2$ heterojunction has a lateral configuration. The simple equivalent circuit is shown in the inset of Fig. 4c. The transfer curves of a heterojunction device fabricated with a thin $MoTe_2$ flake was also investigated in Supplementary Fig. 6, indicating the gate dependence was determined by the series

connection of the two materials. Based on this analysis, we deduce that the $MoTe_2/SnS_2$ heterojunction gives rise to the rectification property only when the resistance values of the parts other than the junction is low enough for the heterojunction to dominate the current flow in the series connection.

Ternary inverter

Finally, we applied the $MoTe_2/SnS_2$ heterojunction to a multi-valued logic device by fabricating a ternary inverter with only two n-type FETs. As illustrated in Fig. 5a, the driving voltage (V_{dd}) and input voltage (V_{in}) were applied to the electrode of the $MoTe_2$ side (E2) and Si back-gate electrode. The end of the electrode of the SnS_2 side (E4) was grounded, and then the output voltage (V_{out}) on the other electrode in contact with the SnS_2 side (E3) was measured.

This is the integration of $MoTe_2/SnS_2$ heterojunction with SnS_2 FETs, which their resistance value can be fully controlled by regulating V_{in}. Figure 5b depicts the equivalent circuit of the ternary inverter. The plot of V_{in} vs. V_{out} in Fig. 5c clearly shows three distinct output voltage regions in the range of 0–60 V at $V_{dd} = 1$ V, corresponding to the three logical states. The output voltage (V_{out}) is a voltage drop across SnS_2 FET determined by the fraction of the driving voltages (V_{DD}) that depends on the resistance ratio between SnS_2 and heterojunction channel. The input voltage-dependent resistance values of both channels are exhibited in Supplementary Fig. 7. For $V_{in} < 10$ V, the SnS_2 FET has a smaller current path than that of the $MoTe_2/SnS_2$ heterojunction channel because of the $MoTe_2$ channel part, leading to "logic 1." For $15 < V_{in} < 25$ V, SnS_2 and heterojunction channels have a constant resistance ratio as shown in Supplementary Fig. 7. This implies the voltage drop across the SnS_2 channel is sustained in this region, resulting in the output "logic 1/2"[7,58]. At high V_{in}, SnS_2 FET is completely turned on, whereas the current passing through the heterojunction is restricted by the large potential barrier, and thus the state "logic 0" is achieved.

DISCUSSION

We fabricated a multilayer n-$MoTe_2$/n-SnS_2 isotype heterojunction device. Raman analysis confirmed the electron transfer from $MoTe_2$ to SnS_2 side based on Anderson's rule. The output characteristics of the $MoTe_2/SnS_2$ heterojunction clearly exhibited the rectification behavior. From a systematic analysis based on a numerical solution of Poisson's equation and Simmons approximation, we ascribed the rectification to a potential barrier exceeding ~1 eV, attributed to the large band offsets between the two materials. Unlike the conventional p–n heterostructure operating by diffusion of minority carrier, we confirmed the transport is determined by the majority carriers via thermionic emission and tunneling process through the potential barrier. Furthermore, we certified the switchable rectification characteristic by varying the gate voltage. While the rectification was turned off for the negative V_g, it was enhanced for the positive V_g up to a maximum rectification ratio of $\sim 10^3$ at a modest source–drain voltage of 1 V in ambient environment. This value is comparable with that of other p–n unisotype vdW heterostructure devices reported by previous studies. Finally, we demonstrate the working of the new device by fabricating a ternary inverter using the $MoTe_2/SnS_2$ FET and a SnS_2 channel transistor. This is the first experimental study reporting a systematical analysis for a $MoTe_2/SnS_2$ heterojunction device. The results can be used as guidelines for the optimization and designing of a variety of heterojunction-based customizable electronic or photonic devices.

METHODS

Device fabrication

$MoTe_2/SnS_2$ heterostructure devices were fabricated by the dry transfer method. $MoTe_2$ and SnS_2 were mechanically exfoliated from their commercial bulk forms (HQ graphene, America) using blue tape on PDMS (Gel-Pak, PF-X4–17 mil.) and a highly n-doped (As doped) substrate with a 300-nm-thick SiO_2 layer, respectively. The $MoTe_2$ flakes on PDMS were aligned by a transfer system-mounted microscope, and then transferred on to SnS_2 flakes. The electrodes were patterned by the electron-beam lithography process, and Ti/Au (20/50 nm) metals were deposited by a thermal evaporator at high vacuum pressure (~10^6 Torr).

Device characterization

AFM measurement was performed in ambient environment with tapping mode, to confirm the thickness of the flakes. Raman spectroscopic measurements (Renishaw) were carried out at room temperature using a 514-nm laser as the excitation source with <2 mW power. We used a Keithley-4200SCS parameter analyzer to measure the electrical properties of the $MoTe_2/SnS_2$ heterojunction device and the ternary inverter.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article. Related additional data are available on reasonable request from the authors.

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AUTHOR CONTRIBUTIONS

S.Kim performed the device fabrication and electrical characterization; S.Kim, C.-W. Lee, and S.Seo were involved in writing the manuscript; H.Du, T.Kim, S.Shin, H.Song, H.Kim, and D.Kang contributed to the scientific discussions. All authors have given approval to the final version of the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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