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Lifetime estimation of thin-film transistors in organic emitting diode display panels with compensation

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Oxide semiconductor thin-film transistors (TFTs) are used in the pixel array and gate driver circuits of organic light emitting diode (OLED) display panels. Long-term reliability characteristics of the TFTs are a barometer of the lifetime of OLED display panels. The long-term reliability of the driver TFTs is evaluated in a short time under high voltages and high temperature for an accelerated degradation test. If reliability parameters from the power law or stretched-exponential functions are the same for individual devices and devices in an operating panel, the lifetime of the panel can be accurately estimated. However, since compensation circuits are designed into operating panels, an environmental discrepancy exists between the accelerated test of single devices and the operation of devices in the panel. Herein, we propose a novel compensation stretched-exponential function (CSEF) model which captures the effect of the threshold voltage compensation circuit in the panel. The CSEF model not only bridges the discrepancy between individual devices and panel devices, but also provides a method to accurately and efficiently estimate the long-term lifetime of all display panels that utilize compensation circuits.

Organic light emitting diode (OLED) displays employ thin-film transistors (TFTs) in their active pixel array and in-panel gate driver circuits. Several types of pixel circuits exist depending on the compensation scheme and control signals, but basically all pixel circuits comprise a driver transistor and switching transistor. The driver TFT drives a current through the OLED to control the luminance of the pixel. The current is determined based on the gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) across the driver TFT, which is controlled using the data signal transferred by the switching TFT and voltage on the source node of the driver TFT. A turn-on voltage and data signal are applied to the gate and drain of the switching transistor, respectively, for a time duration of $1/f/N_{scan}$ for each frame time ($=1/f$), where f is the refresh rate and N_{scan} is the number of pixels along the vertical direction of the display. For example, if the $f=120$ Hz and $N_{scan}=2160$ for an ultra-high definition television (UHD TV), signals to the switching transistor will be in the order of 3.8 µs every 8.3 ms. Pixel transistors are fabricated using oxide semiconductors or low-temperature polycrystalline silicon (LTPS). Oxide semiconductors exhibit good large-area uniformity up to generation 11 glass substrates (2940 mm × 3370 mm in size) making them suitable for large-screen displays in OLED TVs[1–3]. Moreover, oxide semiconductors also exhibit ultra-low off-state current ($< 10^{-15}$ A) necessary for low-power energy-efficient displays in smartphones and smartwatches, where they are used in tandem with LTPS[4–7]. During operation of the display panel, the threshold voltage (V_T) of the driver TFT shifts owing to electron trapping in the gate dielectric, and intrinsic defects in the channel material such as peroxy linkage or undercoordinated metal cations[8–13]. Any shift in the V_T (ΔV_T) leads to brightness droop over time or brightness non-uniformity across the panel area. Therefore, ensuring satisfactory long-term reliability of TFTs is crucial with respect to the lifetime of OLED displays. Typically, TFTs are fabricated independently and subjected to harsh stress conditions (higher voltage, higher temperature) than normal operating conditions to accelerate degradation and assess reliability in a reasonable test time. This method is used as a proxy for assessing reliability of TFTs in a panel to estimate the panel lifetime during normal operation. Time dependence of ΔV_T of a single device is generally described using the power law, $\Delta V_T(t) \propto t^b$, or the stretched-exponential function (SEF),

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$$\Delta V_T(t) = \Delta V_{T0}\left[1 - e^{-(t/\tau)^{\beta}}\right] \quad (1)$$

which are used to depict the long-term reliability of the OLED panel[14,15]. If the parameters from $\Delta V_T(t)$ of an individual device were the same as those of TFTs in a OLED panel, then this connection between individual TFTs and panel TFTs would not be an issue. However, in addition to the different voltage conditions between individual TFTs and TFTs in the panel, we discovered that the correlation begins to collapse when the devices and panel circuitry become increasingly more intricate. The most striking difference is that V_T compensation circuits are put in place for the driver TFTs in a panel environment[3,16,17]. Hence, the discrepancy between the accelerated stress measurement of an individual TFT and the long-term reliability of the panel is inevitable. Closing the gap between the reliability test of individual devices and panel devices is challenging; however, minimizing this discrepancy is important for ensuring accurate panel lifetime estimation. In this study, we identify this discrepancy and propose a compensated stretched-exponential function model that correctly captures the degradation of panel TFTs including the effect of the compensation circuit. By using this model, we can accurately estimate the long-term lifetime of display panels in a shorter time than conventional methods.

Results

Identification of inconsistency between individual device and panel device tests

The reliability of oxide semiconductor TFTs is a crucial factor that determines the lifetime of a display panel. The lifetime of display panels (e.g., commercial televisions) operated under normal usage should be 10 years or more. The failure of a display panel may occur due to long-term degradation of the OLED (due to aging and/or chemical damage) or the electronic devices controlling the OLEDs. The lifetime of the display panel is determined based on the failure of the OLED or TFT, whichever occurs earlier. This study focuses on the lifetime of the oxide semiconductor TFT backplane. The critical lifetime of the TFT is realized when the worst-case V_T reaches $V_T(\tau_{life}) = V_T(t=0) + \Delta V_{T,limit}$, where $\Delta V_{T,limit}$ is a predetermined value set depending on the upper limit the compensation circuit can effectively operate and accurately compensate the ΔV_T. Owing to the slow degradation process, accelerating the degradation by testing the devices under high voltages and temperatures in a matter of hours is a common practice. However, the correlation between the accelerated reliability test of a single TFT device and the lifetime of an OLED panel fails when the panel and devices become increasingly complex. Hence, the panel lifetimes are often extrapolated from electrical measurements of panel degradation over months-long test operation. Finding the reason behind this discrepancy and validating a consistent and quantitative correlation between device and panel lifetime is crucial in significantly shortening the panel evaluation time and accurately representing the TFT array in a panel environment.

Figure 1 shows the ΔV_T with respect to TFTs in an operating display panel under different gray levels up to 1500 h at room temperature. The gray level is defined as the digitized brightness level of a pixel, with 0 G being the darkest and 255 G being the brightest level. Gray levels are expressed based on calibrated voltage conditions including gate overdrive voltage V_{OV} (= V_{GS} – V_T) and drain-to-source voltage V_{DS} conditions applied to the driver TFTs. The ΔV_T is higher for higher gray levels because the TFTs are subject to high bias stress conditions. Hence, examining whether the device reliability tests correlate to the reliability of TFTs in the pixel array of a panel is extremely important.

Figure 2 shows the ΔV_T of an InGaZnO (IGZO) TFT device under DC stress using different gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}) conditions. Symbols in Fig. 2 represent the measured data and the lines represent SEF fitting curves. Table 1 shows the SEF parameters (ΔV_{T0}, τ, β) for different bias stress

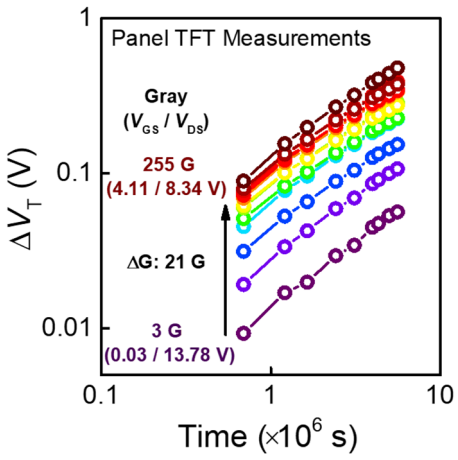

Figure 1. V_T shift of transistors in the display panel subject to different gray levels varying from 3 to 255 G, up to 1500 h in a room temperature ambient. Each gray level is determined based on the gate overdrive voltage (V_{GS} – V_T) and drain-to-source voltage (V_{DS}) applied to the driving transistor, represented in the figure as the first and second numbers in parenthesis, respectively. Difference in gray levels between curves is 21 G apart.

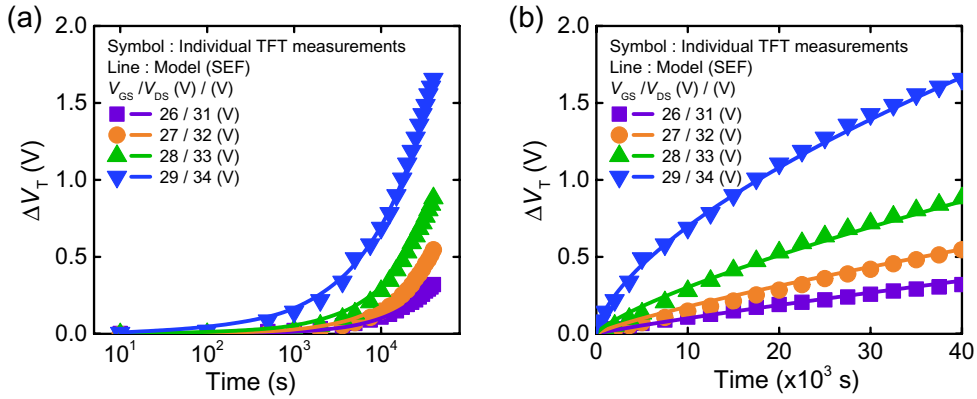

Figure 2. V_T shift of individual transistors for different V_{GS} and V_{DS} combinations, with time x-axis in (**a**) log scale, and (**b**) linear scale. Measurements are represented using symbols and stretched-exponential function (SEF) model values are represented using solid lines.

$\Delta V_{T0} = V_{GS} - V_T$	20 V	21 V	22 V	23 V	24 V	25 V	26 V	27 V	28 V	29 V
τ (s)	1.5×10^7	1.2×10^7	9.7×10^6	9.8×10^6	8.7×10^6	1.0×10^7	8.7×10^6	8.2×10^6	7.6×10^6	7.3×10^6
β	0.90	0.80	0.85	0.90	0.80	0.85	0.90	0.85	0.80	0.75

Table 1. Stretched-exponential function model parameters of an individual IGZO TFT device under DC stress of different bias conditions.

conditions. Generally, the extracted τ and β values differ upon how ΔV_{T0} is defined. ΔV_{T0} is the saturated value of ΔV_T when the TFT has been subject to stress for a sufficiently long time ($t \rightarrow \infty$).

When the N_{OT}-*limited model* is used, we assume that the cause of ΔV_T saturation over time is caused by the finite trap density in the interface and bulk of the gate dielectric (N_{OT}). In this model, ΔV_{T0} is a constant that is irrelevant to the stress voltage and is determined by N_{OT} present in the device. ΔV_{T0} is determined based on the maximum ΔV_T caused by N_{OT} being completely full of trapped charge.

$$\Delta V_{T0} = \frac{qN_{OT} \cdot t_{ox}}{C_{ox}} \tag{2}$$

where q is the elementary charge, C_{ox} is the gate oxide capacitance per area, and t_{ox} is the thickness of the gate dielectric layer. Figure 3a shows the $\Delta V_T(t)$ of the panel TFTs for different gray levels, where $N_{OT} = 3\times10^{17}$ cm^{-3} is assumed which gives $\Delta V_{T0} = 30$ V. All $\Delta V_T(t)$ curves saturate at the same ΔV_{T0} value, where hypothetically all the defect states in the GI are filled with trapped electrons at $t \rightarrow \infty$. The characteristic time τ in the SEF (Eq. 1) can be extracted using the measured $\Delta V_T(t)$ for panel and single individual devices (Eq. 2). Also, τ follows an inverse relationship with ($V_{OV} = V_{GS} - V_T$) as expressed in the following equation:

$$\tau = \left[\sigma_0 \cdot \nu_{th} \cdot f_{MB} \cdot n_s\right]^{-1} = \left[\sigma_0 \cdot \nu_{th} \cdot f_{MB} \cdot C_{ox} \cdot (V_{GS} - V_T)/q \cdot t_{act}\right]^{-1} \tag{3}$$

where σ_0 is the capture cross section, ν_{th} is the thermal velocity, f_{MB} is the Maxwell–Boltzmann distribution function, n_s is the carrier volume density, and t_{act} is the thickness of the active channel layer. The calculated τ (Eq. 3) and the τ extracted from panel and individual device measurements using the N_{OT}-limited model are plotted against ($V_{GS} - V_T$) in Fig. 3b. We discovered that the τ extracted from stress tests of single individual devices agree with the calculations; however, the τ extracted from panel TFTs do not follow the calculated τ-V_{OV} trend, exhibiting noticeably higher values. Hence, the N_{OT}-limited SEF model is not appropriate for predicting the lifetime of TFTs in a display panel.

In the *electric-field-limited model*, the ΔV_T saturates due to the weakening of the electric field across the gate insulator. This is because the V_T shifts positively under stress owing to the trapped charge while V_{GS} is constant, hence decreasing $V_{GS} - V_T(t)$ over time. In the electric-field-limited model, we define

$$\Delta V_{T0} = V_{GS} - V_T(t = 0), \tag{4}$$

$$\Delta V_T(t) = [V_{GS} - V_T(t = 0)] \cdot \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]. \tag{5}$$

Hence, ΔV_{T0} is dependent on the stress V_{GS} and initial V_T of the device. Figure 3c shows the $\Delta V_T(t)$ of the panel TFTs for different gray levels using the electric-field-limited model, where devices subject to low $V_{GS} - V_T(t=0)$ saturates at low ΔV_{T0} values. Figure 3d plots the extracted and calculated characteristic time τ against V_{OV} using the electric-field-limited SEF model. The τ extracted from $\Delta V_T(t)$ of individual devices under reliability tests

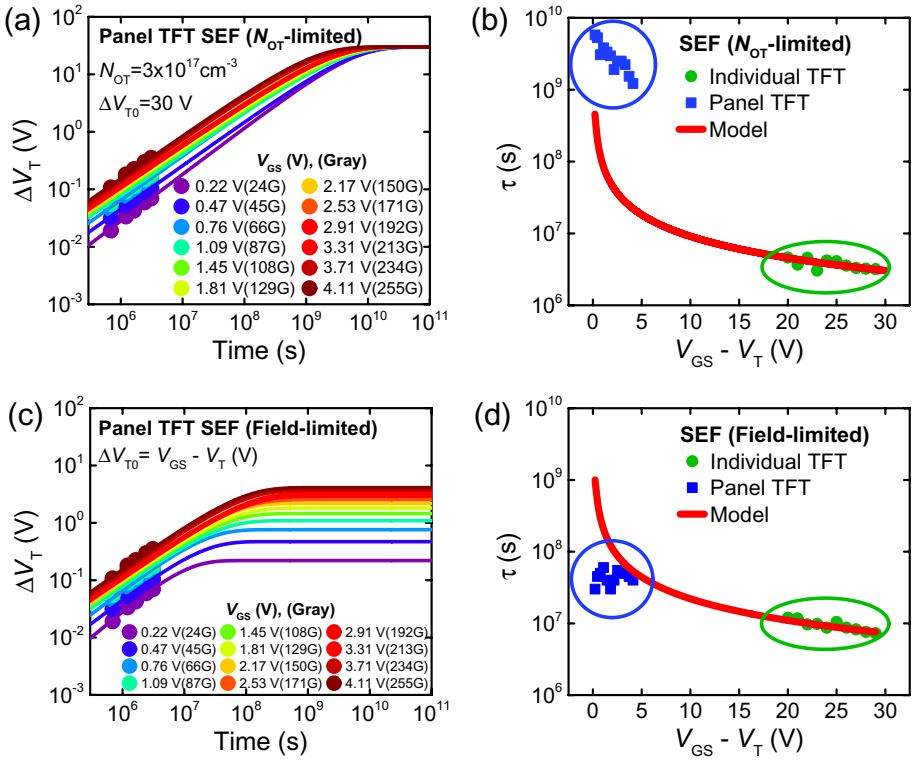

Figure 3. (**a**, **c**) Threshold shift (ΔV_T) of IGZO TFTs in the display panel subject to various bias conditions corresponding to a range of gray levels. Symbols represent measurement values up to 1500 h, while solid lines represent modeling results extended to 10^{11} s using the (**a**) N_{OT}-limited model and the (**c**) electric-field-limited model. (**b**, **d**) Characteristic time constant τ from reliability tests of individual devices (green squares) and devices in a panel (blue circles). τ values are extracted from SEF using the (**b**) N_{OT}-limited model and (**d**) electric-field-limited model. A calculated inverse relationship between τ and V_{OV} is represented by the solid red line. Panel τ values deviate from the inverse relationship under both models.

follow the inverse correlation with V_{OV}. However, τ extracted from panel TFTs do not follow this correlation with the calculated values and exhibit lower values. The field-limited SEF model does not capture the $\Delta V_T(t)$ for panel TFTs and has weak correlation with that of individual TFTs, and hence cannot be used as a prediction model for the panel lifetime. Therefore, both SEF models do not accurately represent the $V_T(t)$ of TFTs in a panel environment, raising the question of whether self-consistency between individual TFT devices and panel TFTs can be achieved. Therefore, if a model could be developed wherein the τ of panel TFTs follows the inverse (V_{GS} – V_T) relation, we could gain confidence that lifetime models between single devices and devices in the panel are consistent. Then, why does the evaluation of TFTs in the panel result in τ values that do not follow the inverse V_{OV} relation? Herein, we propose a novel model to bridge this discrepancy.

Proposed compensated stretched-exponential function model

Primary difference in evaluation conditions between a reliability test for an individual device and devices in the panel is whether the bias conditions are maintained constant or not. Constant voltage is maintained throughout the stress phase of an instability test of a single individual device. However, OLED display panels have a compensation circuit that compensates the varying V_T in real-time, indicating that the bias conditions change dynamically as the V_T of devices in the pixel array shift. Hence, we must first determine whether the SEF fitting is fundamentally appropriate for devices in a panel with dynamic V_T compensation.

When the V_T shifts due to stress or a prolonged period of normal operation, V_T can be represented as $V_T = V_T(t=0) + \Delta V_T(t)$, where $V_T(t=0)$ is the initial V_T and $\Delta V_T(t)$ is the time-dependent V_T shift. For $V_{GS} - V_T$ to be kept constant, the compensation circuit applies $V_{GS} + \Delta V_T(t)$ instead of V_{GS} to the driver TFT. Thus, the SEF can be modified as follows:

$$\Delta V_T(t) = [(V_{GS} + \Delta V_T(t)) - V_T(t=0)]\left[1 - e^{-(t/\tau)^{\beta}}\right] \quad (6)$$

from Eqs. 1 and 4, assuming the electric-field-limited case. The $\Delta V_T(t)$ term is present on both sides of Eq. 6; hence, by rearranging the terms we obtain the *compensated stretched-exponential function* (CSEF), expressed as follows:

$$\Delta V_T(t) = [V_{GS} - V_T(t=0)] \cdot \left[\frac{1}{e^{-(\frac{t}{\tau})^{\beta}}} - 1\right]. \quad (7)$$

CSEF can be used to extract the τ and β from devices in an active panel with V_T compensation. Figure 4a shows the CSEF model fitting to V_T shifts of devices in a panel for various gray levels up to 3600 h at room temperature. First, we implement the CSEF model to devices on the display panel with a constant brightness represented by a gray level ranging from 24 to 255 G. The measured $V_T(t)$ of TFTs in the panel with respect to various constant gray levels are overlaid on top of CSEF model curves with parameters τ and β corresponding to each gray level in Fig. 4a. Table 2 lists the CSEF parameters for various brightness levels. The CSEF parameter τ values from the panel TFTs are plotted against $V_{GS} - V_T$ juxtaposed with those of individual TFT devices on the same plot in Fig. 4b. The modified τ extracted from panel devices now follows the inverse relation with $(V_{GS} - V_T)$, justifying the hypothesis that indeed the compensation was the cause of the discrepancy between panel devices and individual devices. The validity of the CSEF model is proven, having τ extracted from both single individual devices and panel devices being in agreement on a universal τ–V_{ov} curve (Eq. 3). By selecting a SEF model based on the stress/operation concept of the device under test, we can maintain consistency between data obtained from standalone devices and devices within a panel. For TFT devices with no compensation the standard SEF model is used, while for TFT devices in a panel with compensation circuit operation the CSEF model is used.

Verification of the CSEF model via various display data patterns

Having established the CSEF model, it is necessary to verify its validity for TFTs in the panel for various data patterns. To emulate a display operation environment rather than a constant DC stress bias, we select rolling patterns between 5 gray levels and an on and off pattern with a duty cycle of 50%. To model the $\Delta V_T(t)$ for TFTs in the panel subject to different patterns, a systematic approach must be adopted. Figure 5a–c show how the $\Delta V_T(t)$ can be obtained for an arbitrary pattern by adjoining $\Delta V_T(t)$ segments each with a constant gray level for a certain duration. Each pattern segment corresponds to a gray level that is correlated to data bias conditions ($V_{GS,i}$, $V_{DS,i}$) for a particular pattern duration (Δt_i). The $\Delta V_T(t)$ during an arbitrary pattern segment can be expressed as:

$$F(t-t_i) = f_i(t_{i,x} + \Delta t_i) + f_{i+1}(t - t_{i+1,x}), t_i = t_{i-1} + \Delta t_i, t_{i+1,x} \text{ is where } f_{i+1}(t_{i+1,x}) = f_i(t_{i,x} + \Delta t_i) \quad (8)$$

where $F(x)$ represents the $\Delta V_T(t)$ from the panel pattern, and $f_i(t)$ represents the individual $\Delta V_T(t)$ for a specific gray level condition corresponding to the voltage pulse $V_{GS,i}$ between t_{i-1} to t_i ($\Delta t_i = t_i - t_{i-1}$). Each pattern segment uses one set of CSEF parameters corresponding to the constant gray levels, as listed in Table 2. The degradation history of V_T caused by the data pattern up to that current point is reflected, by keeping the final ΔV_T value of

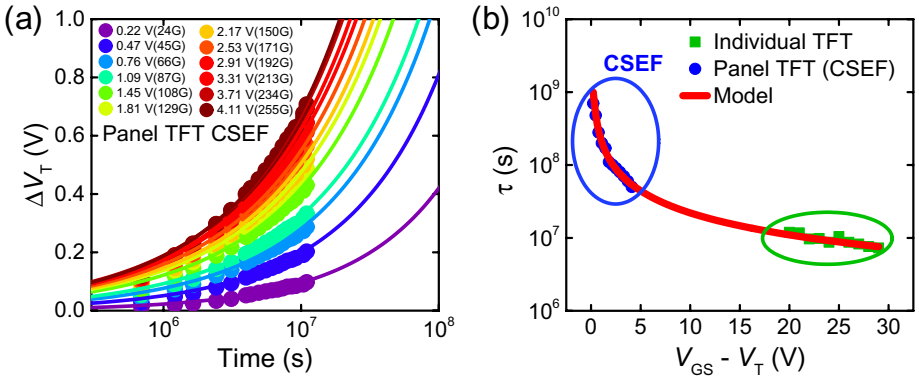

Figure 4. (**a**) ΔV_T of IGZO TFTs in the display panel subject to various bias conditions corresponding to a range of gray levels. Symbols are measured values up to 3,600 h, while the solid lines are fitting curves using the compensated stretched-exponential function (CSEF) model. (**b**) τ values extracted using the CSEF model for TFTs in a panel with compensation (blue circles) and the SEF model for individual TFTs (green squares). All extracted values follow the Inverse relationship between τ and V_{OV} (red solid line).

Brightness	025 G	045 G	066 G	087 G	108 G	127 G	150 G	171 G	192 G	213 G	234 G	255 G
ΔV_{T0} (V)	0.22	0.47	0.76	1.09	1.45	1.81	2.17	2.53	2.91	3.31	3.71	4.11
τ (s)	2.5×10^8	1.7×10^8	1.2×10^8	9.7×10^7	7.8×10^7	6.5×10^7	5.5×10^7	4.8×10^7	4.2×10^7	3.8×10^7	3.4×10^7	3.1×10^7
β	0.63	0.62	0.68	0.68	0.72	0.62	0.73	0.82	0.78	0.78	0.77	0.82

Table 2. Parameters for panel TFTs at various bias conditions each corresponding to a brightness (in gray levels) using the proposed CSEF model.

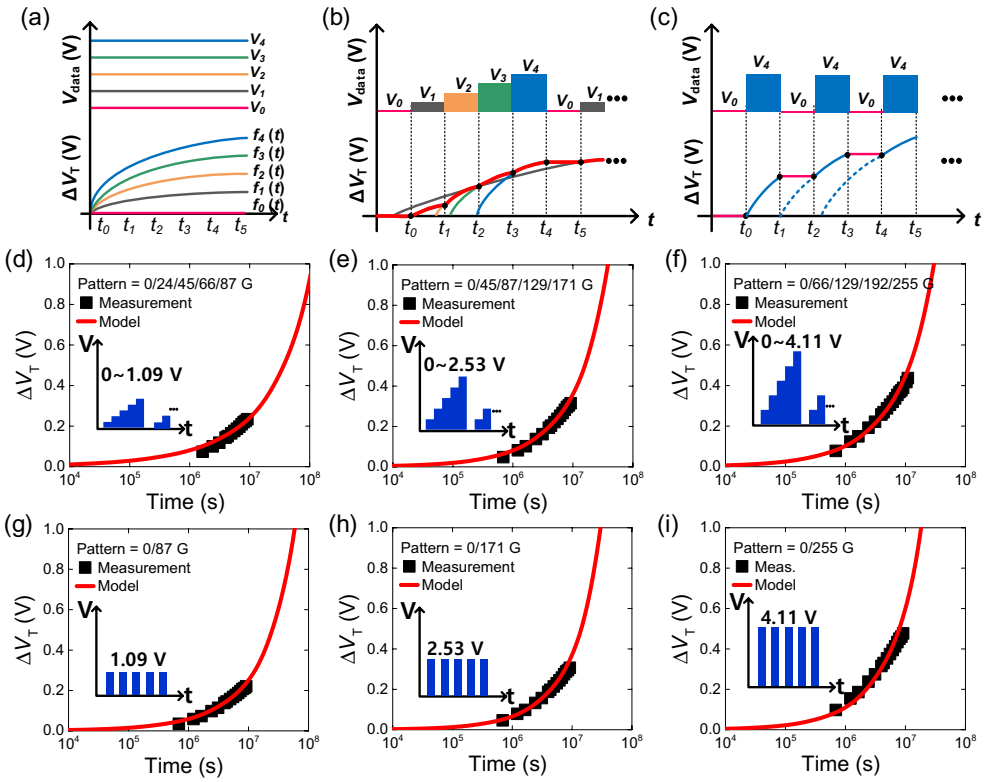

Figure 5. (**a**–**c**) Methodology for modeling the $\Delta V_T(t)$ of TFTs in a display panel subject to arbitrary patterns, such as (**b**) cycling of 5 gray levels, and (**c**) on and off cycling pattern with 50% duty. Estimation of ΔV_T of panel TFTs under a 5–gray pattern (measurement values in square shapes, CSEF model in solid lines) for various gray level combinations: (**d**) 0, 24, 45, 66, and 87 G (V_{GS}=0–1.09 V); (**e**) 0, 45, 87, 129, and 171 G (V_{GS}=0–2.53 V); and (**f**) 0, 66, 129, 192, and 255 G (V_{GS}=0–4.11 V). Estimation of ΔV_T of panel TFTs using the CSEF model (solid line) in comparison to measured values (square shapes) for an ON/OFF pattern cycling between 0 G (V_{GS}=0 V) and (**g**) 87 G (V_{GS}=1.09 V), (**h**) 171 G (V_{GS}=2.53 V), and (**i**) 255 G (V_{GS}=4.11 V), respectively.

the previous segment as the initial value of the current segment. Furthermore, since $\Delta V_T(t)$ is updated and not reset after each segment, the change in degradation rate is also considered. For example, the first few segments can be expressed as:

$$F(t-t_0) = f_1(t-0) \tag{9}$$

$$F(t-t_1) = f_1(\Delta t_1) + f_2\left(t-t_{2,x}\right),\ t_1 = t_0 + \Delta t_1,\ t_{2,x} \text{ is where } f_2\left(t_{2,x}\right) = f_1(\Delta t_1) \tag{10}$$

$$F(t-t_2) = f_2\left(t_{2,x} + \Delta t_2\right) + f_3\left(t-t_{3,x}\right), t_2 = t_1 + \Delta t_2,\ t_{3,x} \text{ is where } f_3\left(t_{3,x}\right) = f_2\left(t_{2,x} + \Delta t_2\right) \tag{11}$$

and so on. By using this method, we can replicate the ΔV_T of panel TFTs experiencing complicated data patterns. Figure 5d–f show the application of the CSEF model using Eq. 8 for a rolling pattern of 5 gray levels for 3600 h using three different gray level combinations. Figure 5g–i show the application of the proposed method on a panel under an alternating on and off pattern with a duty cycle of 50%. We can observe that the $\Delta V_T(t)$ measurements and model results are in good agreement, validating the panel data pattern-dependent CSEF model. We can accurately predict the panel lifetime under arbitrary complex display patterns using CSEF model parameters obtained from measurement data of panel TFTs under various gray level conditions.

CSEF model with V_{T0} variation using empirical V_{T0}-dependent τ model

Owing to the amorphous nature of oxide semiconductors, it is inevitable but to have a statistical variation in device properties across the large glass substrate spanning over 3 m on one side. Based on the verified panel data-dependent CSEF model, we analyze the initial V_T (= V_{T0}) distribution in the CSEF model, specifically by establishing a relation between V_{T0} and τ. Figure 6a shows the ΔV_T of 24 panel devices with variation plotted against V_{T0}. The devices are operated at a constant gray level for 3600 h. Despite maintaining a constant V_{OV} throughout the operation with the help of the compensation circuit, a positive correlation between ΔV_T and V_{T0} can be observed. This shows that devices with high V_{T0} will most likely result in high ΔV_T. Figure 6b–d show the $\Delta V_T(t)$ of 24 devices in the display panel at a constant brightness level (only few selected gray levels are shown).

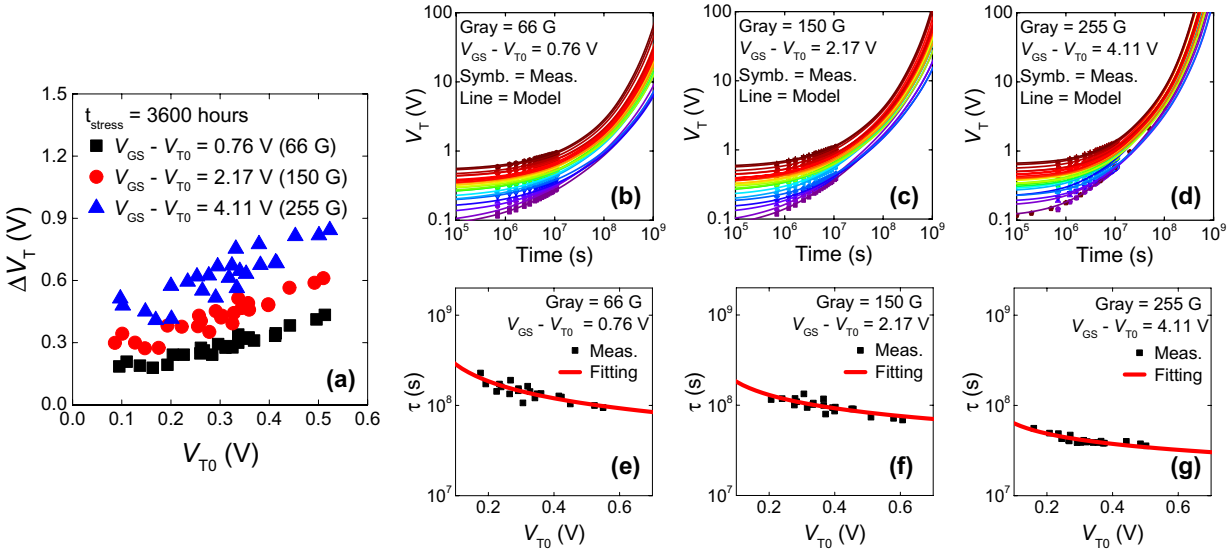

Figure 6. (**a**) Distribution of ΔV_T of 24 devices with V_{T0} variation plotted against V_{T0}. A positive correlation is consistently observed across different gray levels. $V_T(t)$ variation of 24 panel devices operated under selected gray levels: (**b**) 66 G, (**c**) 150 G, (**d**) 255 G. Measurement values are denoted by shapes, and CSEF model curves are shown in solid lines. Extracted τ values from CSEF plotted against V_{T0} of the devices: (**e**) 66 G, (**f**) 150 G, (**g**) 255 G. Fitted empirical functions of τ are shown in red solid lines.

In Eq. 3, any change in V_{T0} does not affect n_s because compensation corrects any $\Delta V_T(t)$ and variation in V_{T0} to ensure that V_{OV} is kept constant. Even under the same intended fabrication process, the local spatial variation in process conditions influence the film properties and the device characteristics, causing variation in V_{T0}. Process factors that vary V_{T0} could also influence the trap properties. Particularly, we assume V_{T0} affects the capture cross-section σ, and an effective V_{T0}-dependent $\tau(V_{T0})$ is introduced. When we use the V_{T0}-dependent $\tau(V_{T0})$ in the CSEF model as in:

$$\Delta V_T(t) = [V_{GS} - V_{T0}] \cdot \left[exp\left(-\left(\frac{t}{\tau(V_{T0})} \right)^{\beta} \right)^{-1} - 1 \right], \tag{12}$$

the model captures the $\Delta V_T(t)$ including V_{T0} variation, which agrees with measured values with respect to different gray levels, as shown in Fig. 6b–d. Average τ and β values obtained from the CSEF model of 24 devices are listed in Table 3. To find the functional form of $\tau(V_{T0})$, variation in τ values are plotted against V_{T0} as shown in Fig. 6e–g. We implement an empirical equation in the form of $\tau = a_0 \cdot {V_{T0}}^{b_0}$, where a_0 and b_0 are used as fitting parameters. These fitting parameters for each brightness level are listed in Table 3. For a higher V_{T0}, τ becomes smaller because $b_0 < 0$ (and $a_0 > 0$) which leads to $\Delta V_T(t)$ increasing rapidly at an earlier timescale. a_0 is smaller and b_0 has a less negative value for a higher ΔV_{T0} which corresponds to a smaller τ value that is less sensitive to V_{T0} at a higher gray level. Our proposed CSEF model can be useful in estimating the lifetimes of display panels including the effect of V_{T0} variation of the TFT devices.

Discussion

Conventionally when evaluating the lifetime of the panel, the power law or SEF are used to model $\Delta V_T(t)$ of TFTs. We have demonstrated that the CSEF model represents driver TFTs more accurately under a V_T compensation scheme compared to the SEF model. Herein, we quantitatively compare the functional form of the power law ($\Delta V_T(t) = a \cdot t^b$), SEF (Eq. 1), and CSEF (Eq. 7). Figure 7a shows the three models as a function of time. Since

Brightness	025 G	045 G	066 G	087 G	108 G	127 G	150 G	171 G	192 G	213 G	234 G	255 G
ΔV_{T0} (V)	0.22	0.47	0.76	1.09	1.45	1.81	2.17	2.53	2.91	3.31	3.71	4.11
Average τ (s)	1.2×10^8	1.0×10^8	1.0×10^8	8.5×10^7	6.8×10^7	6.5×10^7	5.2×10^7	4.2×10^7	3.8×10^7	3.3×10^7	3.1×10^7	2.8×10^7
Average β	0.67	0.63	0.68	0.76	0.73	0.56	0.74	0.82	0.80	0.75	0.72	0.83
a_0 (s V^{-b})	7.1×10^7	6.4×10^7	6.8×10^7	5.9×10^7	5.9×10^7	5.8×10^7	5.9×10^7	5.2×10^7	4.7×10^7	3.7×10^7	2.7×10^7	2.7×10^7
b_0	−0.98	−0.91	−0.63	−0.66	−0.57	−0.51	−0.49	−0.42	−0.53	−0.33	−0.40	−0.38

Table 3. Average of CSEF parameters across 24 TFTs with statistical variation for various brightness levels. Fitting parameters a_0 and b_0 for the empirical functional form of $\tau = a_0 \cdot {V_{T0}}^{b_0}$.

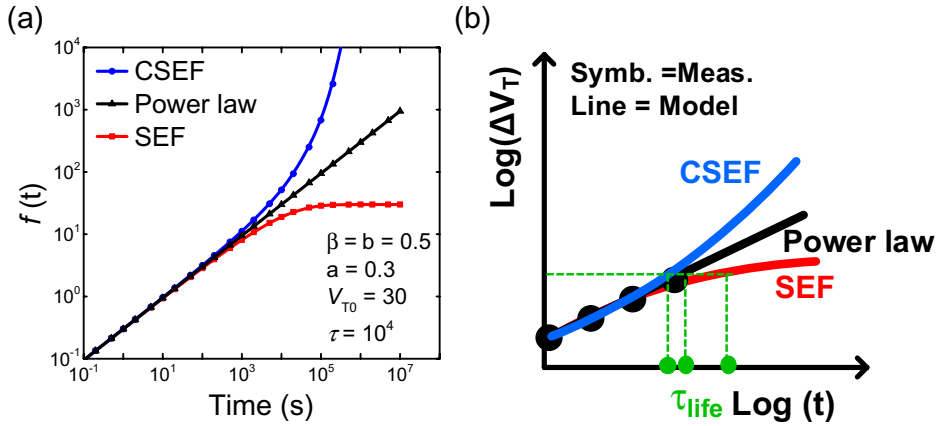

Figure 7. (**a**) Comparison of the functional form between the power law, SEF, and CSEF model. Exponents of time are set equal ($\beta = b = 0.5$). (**b**) Extraction of the panel lifetime using the CSEF model, power law, and SEF.

b and β determine the slope of the functions in a log–log plot, we equate them to be the same value, $b = \beta$. We note that when $t \ll \tau$, the functions approximately overlap. When $t \ll \tau$ and $0 < \beta < 1$ are satisfied, the SEF can be approximated by the power law, as in asymptotic power laws[18,19]. The power law is not based on physical parameters; it is a mathematical approximation of the SEF. Because the power law has a simple form, it is often widely employed in the industry instead of SEF. Conversely, when time becomes comparable to or larger than τ, the curves differ from one another in the following order: $\Delta V_{T,CSEF} > \Delta V_{T,powerlaw} > \Delta V_{T,SEF}$, where SEF saturates at $\Delta V_{T,SEF}(t \rightarrow \infty) = \Delta V_{T0}$. For TFTs in display panels, we observe that the CSEF describes and reproduces the panel measurement data, and CSEF parameters follow the same $V_{OV}{}^{-1}$ relation as followed by the SEF parameters of individual TFTs. As shown in Fig. 7b, when the panel lifetime is short, the selection among the three models may have less importance. However, as a longer product lifetime is desired, and the TFTs and circuit schemes become increasingly sophisticated, stable, and robust, the SEF or power law underestimates the ΔV_T when extrapolated beyond measurement data, thus posing the risk of overestimating the lifetime of the display panel.

The stress conditions for reliability evaluation with respect to individual TFTs and panel TFTs are different in voltage and temperature levels, as well as operating methods. Hence, a discrepancy is observed in ΔV_T progression. Moreover, owing to the absence of an appropriate model, panels are subject to long testing times of up to thousands of hours. We have proposed a novel CSEF model that captures the $\Delta V_T(t)$ of TFTs in a panel with V_T compensation circuits. The proposed CSEF model is verified by comparing the measurement data of $\Delta V_T(t)$ up to 3600 h. Additionally, the efficacy of the proposed model is proven by accurately estimating the $\Delta V_T(t)$ of TFTs in a panel with respect to different data patterns. We can shorten the panel lifetime evaluation time to the amount of time required to extract CSEF parameters from panel TFTs at various gray levels, estimate the lifetime of panels under various arbitrary display rolling patterns, and extend the range of lifetime estimation far beyond conventional extrapolation methods. Furthermore, the CSEF model does not overestimate the panel lifetime as opposed to the widely-used power law or the standard SEF. Thus, using the CSEF model for estimation would be more rigorous, especially for panels with long lifetimes.

Methods

Self-aligned top-gate structure amorphous IGZO TFTs are fabricated herein[10]. First, a bottom metal layer is deposited on the glass substrate to serve as a light shield, followed by the deposition of a SiO_2 buffer layer via plasma-enhanced chemical vapor deposition (PECVD). The semiconductor active layer is formed via DC sputtering of a-IGZO (In:Ga:Zn = 1:1:1), followed by gate stack formation comprising a SiO_2 gate insulator formed by PECVD, and a Cu gate formed via sputtering. During patterning of the gate stack, the dry etch and plasma treatment forms the highly conductive source/drain access regions. Interlayer dielectric is deposited by the PECVD of SiO_2, and contact holes are formed for Cu S/D electrodes to fill via sputtering. The source node of the driver TFT is electrically connected to the light shield layer. A SiO_2 passivation layer is deposited by PECVD. Width and length of the devices are 18 μm and 8.5 μm, respectively. Electrical properties are measured using a semiconductor parameter analyzer (4156C, Agilent). V_T of the individual TFTs are extracted where $I_D = 5$ nA from the saturation current characteristics at $V_{DS} = 10$ V. Stress conditions for the reliability tests of the standalone individual TFTs are $V_{GS} = 20$–30 V and $V_{DS} = V_{GS} + 5$ V to ensure saturation operation at room temperature. Stress time is 4×10^4 s and recovery time is 10^4 s.

For the panel evaluation, $V_T(t)$ of the driver TFT in the pixel is recorded for 3600 h, for constant brightness of various gray levels and different test data patterns. V_T of the driver TFT is obtained from a read-out circuit in the panel. The change in V_T is compensated during operation using an external compensation circuit[2]. The panel region is divided into different sections, wherein each section of the panel is subject to either a constant gray level or rolling test patterns. For constant gray levels, the brightness of the white color is varied from 0 to 255 G, with increments of 21 G. For rolling test data patterns, an ON/OFF pattern and a rolling 5-level pattern are used.

CSEF parameters are extracted from the measurement data of panel TFTs by using:

$$\ln\left[\ln(1+\frac{\Delta V_T(t)}{\Delta V_{T0}})\right] = \beta(\ln(t) - \ln(\tau)), \tag{13}$$

which is a rearrangement of Eq. 7. When the left-hand side of Eq. 13 is plotted against $\ln(t)$, τ and β can be found from the x-axis intercept and slope, respectively.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

J.P., S.C., S.O., and D.H.K. designed this work and wrote the main part of the manuscript. J.P., S.C., and C.K. performed device characterization and modeling. H.J.S., Y.S.J., and J.U.B. contributed to the design, fabrication, and characterization of the OLED display panels. J.P., S.C., H.J.S., Y.S.J., J.U.B., S.O., and D.H.K. discussed the results. The manuscript was written through the contributions of all authors. All authors have given approval to the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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