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# Ternary logic decoder using independently controlled double-gate Si-NW MOSFETs

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**A ternary logic decoder (TLD) is demonstrated with independently controlled double-gate (ICDG) silicon-nanowire (Si-NW) MOSFETs to confirm a feasibility of mixed radix system (MRS). The TLD is essential component for realization of the MRS. The ICDG Si-NW MOSFET resolves the limitations of the conventional multi-threshold voltage (multi-$V_{th}$) schemes required for the TLD. The ICDG Si-NW MOSFETs were fabricated and characterized. Afterwards, their electrical characteristics were modeled and fitted semi-empirically with the aid of SILVACO ATLAS TCAD simulator. The circuit performance and power consumption of the TLD were analyzed using ATLAS mixed-mode TCAD simulations. The TLD showed a power-delay product of 35 aJ for a gate length ($L_G$) of 500 nm and that of 0.16 aJ for $L_G$ of 14 nm. Thanks to its inherent CMOS-compatibility and scalability, the TLD based on the ICDG Si-NW MOSFETs would be a promising candidate for a MRS using ternary and binary logic.**

Scalability is one of the most important concerns in complementary metal–oxide–semiconductor (CMOS) device and circuit design[1]. Over the past several decades, the metal–oxide–semiconductor field-effect transistor (MOSFET) has been continuously scaled down to achieve higher performance and higher packing density with lower cost. An undesirable consequence of this aggressive down-scaling has been the appearance of adverse short-channel effects (SCEs), as well as increasingly challenging fabrication limits. To mitigate the SCEs, and continue further down-scaling, innovative device structures such as FinFETs, gate-all-around (GAA) FETs and a nanosheet (NS) based FET, have been introduced[2–6]. These new device structures have been able to suppress the off-state current ($I_{off}$), which is fatal to the power consumption of a chip in the stand-by state. However, even with the above structural innovations, there are still limits that require device and process parameters to be continuously optimized.

Another approach to improving on-state current ($I_{on}$) and chip performance has focused on the use of new materials, such as strained Si/SiGe and III–V compound semiconductors[7–9]. Although the new materials have advantages, silicon is still the most attractive material when CMOS-compatibility with low-cost is considered[10].

In the meanwhile, multi-valued logic (MVL) has also been considered promising architecture to overcome the MOSFET scaling limitations from a circuit point of views. The MVL system can reduce the burden of circuit complexity inherent to binary-based logic circuits, by converting a multiple-output Boolean function into a single-output multiple-valued function[11,12]. In one particular case, a ternary-based logic circuit reduced the total cost and power consumption by minimizing the number of required inputs, resulting in the simplification of metal interconnection, compared to other MVL systems[13].

In spite of these potential advantages, the practicality of ternary logic design heavily relies on the availability of the device and circuitry, which must be compatible with present-day binary CMOS technologies[12]. Binary operation has been the mainstay of modern computing system. To take full advantage of ternary logic, a mixed radix system (MRS) using both ternary and binary logic would be more suitable, rather than exclusively using ternary logic. To implement a MRS, conversion from a ternary code to a binary code is essential and vice versa[14–16]. This requires a ternary logic decoder (TLD). Logic blocks such as a ternary logic multiplexer (TLM), a TLM-based half adder and comparator can be implemented based on the TLD[17].

To realize a TLD, a logic scheme for multi-threshold voltage (multi-$V_{th}$) is necessary[18]. There have been two approaches used to implement a multi-$V_{th}$ scheme. One uses physical methods, by tuning the work-function of a metal gate[19] and by modulating the channel or body doping concentration by ion implantation[20]. The other utilizes electrical methods, applying back bias to a body in the MOSFET or potential redistribution in a gate electrode[21]. However, the aforementioned methods have several challenging issues. The gate work-function

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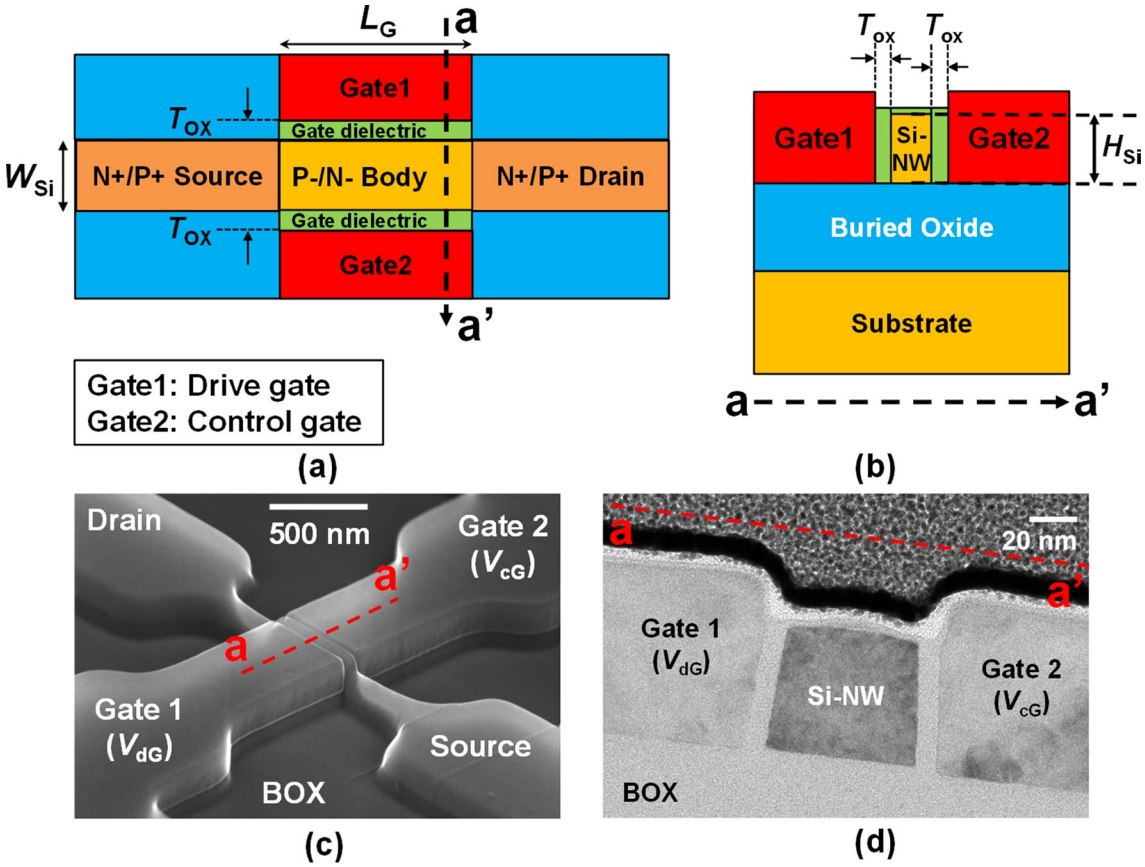



**Figure 1.** Overall structure of the ICDG Si-NW MOSFET. **(a)** Cross-sectional schematic of the ICDG Si-NW MOSFET along with the channel direction. **(b)** Cross-sectional schematic of the ICDG Si-NW MOSFET along with the gate direction. **(c)** SEM image of the fabricated ICDG Si-NW MOSFET. **(d)** Cross-sectional TEM image of the fabricated ICDG Si-NW MOSFET along with the gate direction.

engineering increases process complexity, and limits the spectrum of potential materials, which can lead to a work function variation (WFV) problem given the variability in grain size[22]. Adjustment of $V_{th}$ by ion implantation also involves issues with complementary dopants, accurate depth and concentration control, diffusivity, implantation-induced damages, and random dopant fluctuations. Moreover, channel doping concentration has little effect on $V_{th}$ control for a thin gate dielectric and a fully-depleted thin-body channel[23–25].

With the electrical approach, additional static back bias in the bulk planar MOSFET increases parasitic capacitance and leakage, which can degrade device performances. In any case, fine tuning the $V_{th}$ is not an easy task, because $V_{th}$ modulated by applied static back bias does not follow a linear relationship. In addition, the static back bias can degrade $I_{off}$ and subthreshold swing (*SS*). For the gate electrode potential redistribution method, another challenging issue has been observed, an increase in static power consumption[21].

In another approach, a previous study attempted to control $V_{th}$ dynamically by using the four-terminals of an independently controlled double-gate (ICDG) FinFET[26–31]. Such a novel device could mitigate the abovementioned problems by allowing multi-$V_{th}$. But, there have been no reports of using ICDG devices for TLD so far. A primary goal of the present work is to demonstrate a TLD composed of ICDG silicon-nanowire (Si-NW) MOSFETs, and to confirm the feasibility of manufacturing a MRS chip. Because of their inherent CMOS-compatibility and simplicity, the proposed TLD would be a promising option for realizing a mixed radix circuit.

## Results and discussion

Supplementary Fig. S1 shows a simplified sequence of the experimental details. N-channel ICDG Si-NW MOSFETs were fabricated, modeled, and fitted semi-empirically with the aid of SILVACO ATLAS TCAD simulator[32]. Thereafter, a P-channel ICDG Si-NW MOSFET was regenerated as a counter-part of the N-channel by simulations. Following device-level simulations, further analyses of the TLD circuit performance and power consumption were conducted using ATLAS mixed-mode TCAD simulations to predict the TLD behaviors at an elementary circuit level, as an extension. All of the abbreviations and nomenclature of variables are summarized in Supplementary Table S1.

Fabrication process of the ICDG Si-NW MOSFET is summarized in Supplementary Fig. S2. Figure 1 shows a schematic of the ICDG Si-NW MOSFET and scanning electron microscopy (SEM) and transmission electron microscopy (TEM), images of the fabricated ICDG Si-NW MOSFET. The fabricated ICDG Si-NW MOSFET was composed of two gates, a drive gate and a control gate, positioned at each sidewall of the Si-NW to control the current flowing in the Si-NW. The drive gate turns the channel on or off. The control gate modulates threshold

voltage as a body electrode does in a conventional bulk-MOSFET. The fabricated device had a Si-NW width ($W_{Si}$) of 70 nm, a gate length ($L_G$) of 500 nm, a Si-NW height ($H_{Si}$) of 50 nm and a gate dielectric thickness ($T_{ox}$) of 10 nm. The dimensions of the modeled device were the same as the fabricated device. Source, body, and drain doping concentration were set to $1 \times 10^{20}$ cm$^{-3}$, $1 \times 10^{15}$ cm$^{-3}$, $1 \times 10^{20}$ cm$^{-3}$, respectively. Various models such as Schockly-Read-Hall (SRH), bandgap narrowing (BGN), Fermi–Dirac (FERMI), energy balance model (EBM), non-local band-to-band tunneling (BTBT), trap-assisted tunneling (TAT), and quantum effect (QUANTUM for electrons and P.QUANTUM for holes) were utilized for the simulations. The P-channel ICDG Si-NW MOSFET was modeled in the same manner as the N-channel device, except for the doping polarity and $H_{Si}$. The dopant of the P-channel device was the opposite that of the N-channel device, and the $H_{Si}$ was doubled considering the difference in carrier mobility of electrons and holes.

Figure 2(a) and (b) show the $I_D$-$V_{dGS}$ characteristics of the measured and simulated N-channel ICDG Si-NW MOSFET, respectively. The $I_D$–$V_{dGS}$ curves are shown for various $|V_{cGS}|$. Measured and simulated $I_D$–$V_{DS}$ characteristics of N-channel ICDG Si-NW MOSFET are superimposed for $V_{cGS} = 0.4$ V (Fig. 2c) and $V_{cGS} = -1.5$ V (Fig. 2d) on the log-scaled $y$-axis and linear-scaled $y$-axis. They (measured and simulated) are very similar to each other. Because individual gate addressing is possible thanks to the use of two local gates, the channel potential of the Si-NW can be controlled independently[33]. One of the two gates is used to sweep the gate voltage of the drive gate while a constant voltage is applied to the other gate, which is the control gate to precisely tune the channel potential of the Si-NW. A shift in $V_{th}$ and its multiple values by $V_{cGS}$ are shown in Fig. 2e. The $V_{th}$ shift by $V_{cGS}$ has linear relationship. The results are consistent with the previously reported data[26–31]. As the $|V_{cGS}|$ increased, the $I_D$-$V_{dGS}$ curve shifted rightward in parallel and the $V_{th}$ was increased. Herein, leakage current is defined as off-state current at $V_{dGS}$ of 0 V. The measured leakage current from the fabricated ICDG Si-NW NMOSFET was decreased from 10 pA to 300 fA as the $|V_{cGS}|$ was increased from 0.4 V to 1.5 V. Figure 2f shows the symmetrically overlaid $I_D$-$V_{dGS}$ curves of the simulated N-channel and P-channel ICDG Si-NW MOSFET. Here, there is a wide overlapped region between the N-channel device and the P-channel device. This wide overlapped region stably creates a intermidiate output signal (output '1'), which enables the TLD. It becomes wider as the applied $|V_{cGS}|$ increases.

Note that there are negative ternary inverters (NTI) and positive ternary inverters (PTI) in ternary logic. Its output state becomes '0' or '2' when the input state is '1'[18] as shown in Fig. 3b. The proposed TLD was composed of NTI, PTI, and negative ternary NOR (NTNOR)[18]. To implement the TLD, the characteristics of NTI and PTI should be confirmed.

As shown in Fig. 3a, the ternary inverter circuitry is similar to a typical binary inverter except for the use of the control gates. The complementary circuit shown in Fig. 3a can become both the NTI and the PTI by adjusting $V_{cGN}$ and $V_{cGP}$. As shown in Fig. 3c, the voltage transfer curve (VTC) is shifted in parallel as $|V_{cGNS}|$ increases from 0.4 V to 2.1 V and $|V_{cGPS}|$ decreases from 2.0 V to 0.3 V. For the NTI, an input voltage ($V_{in}$) of 0.5 V (state '1') is transformed to a $V_{out}$ of 0 V (state '0') because $|V_{th}|$ in the P-channel device is higher than that of the N-channel device. In contrast, the $V_{in}$ of 0.5 V (state '1') is converted to a $V_{out}$ of 1 V (state '2') in the case of the PTI, due to the higher $|V_{th}|$ of the N-channel device.

Figure 3d shows the $I_{VDD}$ and $P_{VDD}$ characteristics versus the $V_{in}$. The $I_{VDD}$ increased and decreased exponentially as the N-channel and P-channel devices started to turn on and turn off, respectively, at a certain voltage. Peak points of the $I_{VDD}$ curve at a certain voltage, were shifted as the $|V_{cGNS}|$ and $|V_{cGPS}|$ changed. $P_{VDD}$ can be obtained by multiplying the $I_{VDD}$ by $V_{DD}$ for various $V_{in}$, as shown in the 2nd $y$-axis in Fig. 3d. We can average $P_{VDD}$ for three states with a different weighting factor: $w_0$ for state '0', $w_1$ for state '1' and $w_2$ for state '2'. This is represented by $< P_{VDD} >_{avg} = (w_0 \cdot P_{VDD}|_{state=0} + w_1 \cdot P_{VDD}|_{state=1} + w_2 \cdot P_{VDD}|_{state=2})/(w_0 + w_1 + w_2)$. This averaged $P_{VDD}$ is approximated to $(1/3) \cdot w_1 \cdot P_{VDD}|_{state=1}$ under the condition of $w_0 = w_1 = w_2$, because the $P_{VDD}|_{state=2}$ and $P_{VDD}|_{state=0}$ are much smaller than the $P_{VDD}|_{state=1}$. It should be noted that $I_{VDD}$ for state '1' is much larger than that at the state '0' and '2'. When the curve (green line) of a typical binary inverter in Fig. 3d is shifted to the NTI or the PTI, the $P_{VDD}|_{state=1}$ decreases. Accordingly, the total $P_{VDD}$ decreases.

A 1-to-3 TLD circuit was designed to examine the feasibility of the ICDG Si-NW MOSFET for the TLD. The TLD consisted of 10 complementary ICDG Si-NW MOSFETs. Figure 4a shows the TLD logic circuit and its VTCs for an output '0', output '1', and output '2' versus the $V_{in}$. The NTNOR CMOS circuitry was the same as the typical binary NOR except for the use of the control gates. The device models for the NTNOR were identical to the device models described in Fig. 2. As shown in the VTC graph in Fig. 4a, the TLD stably accepts voltage near 0.5 V as an input then it produces the third output voltage (output '1'). The behaviors of the TLD were verified using the ATLAS mixed-mode TCAD simulations, as shown in Fig. 4b and c. Voltage levels of 1 V ($V_{DD}$), 0.5 V (half $V_{DD}$), and 0 V ($V_{SS}$) are equivalent to a logic value of '2', '1', and '0', respectively. Figure 4d shows a diagram of the state transition with propagation delay time. Note that the transition time is related to on-current of a MOSFET. According to the result of Fig. 4d, $t_2$ ('1' → '0') was almost the same as $t_5$ ('2' → '0') because both the $t_2$ and $t_5$ depend on the on-current of an n-channel pull-down transistor ($I_{on,\,'0'}$). Likewise, $t_3$ ('1' → '2') was the same as $t_6$ ('0' → '2') because both the $t_3$ and $t_6$ depend on the on-current of a p-channel pull-up transistor ($I_{on,\,'2'}$). $t_1$ and $t_4$ are dominated by on-current ($I_{on,\,'1'}$) at an intermediate state. $I_{on,\,'1'}$ is defined as the drain current at $V_{dGS} = V_{DD}/2$. As shown in Fig. 2f, the $I_{on,\,'1'}$ was smaller than the $I_{on,\,'0'}$ and $I_{on,\,'2'}$. Therefore, $t_1$ and $t_4$ were longer than the other transition times ($t_2$, $t_3$, $t_5$, and $t_6$). Additionally, the difference between $t_1$ and $t_4$ was arisen from a slight disparity of $I_D$ between $I_{on,\,'1'}$ of a p-channel MOSFET and an n-channel MOSFET. The delay time ($\tau_d$) is dominated by the longest transition time ($t_1$). To reduce the delay time, $I_{on,\,'1'}$ modulated by $|V_{cGS}|$ should be maximized as large as possible.

Based on SILVACO ATLAS TCAD simulator, the scaling analysis was implemented by reducing device dimensions ($L_G$, $W_{Si}$, $H_{Si}$, and $T_{ox}$). The detailed information of those is shown in Supplementary Table S2. Figure 5 shows a quantitative analysis of gate capacitance ($C_{gg}$) and $I_{on,\,'1'}$. Figures 5a and b show the $C_{gg}$-$V_{dG}$ characteristics depending on $L_G$ under certain $V_{cG}$ conditions which were optimized for $V_{th}$-modulation. Optimization of

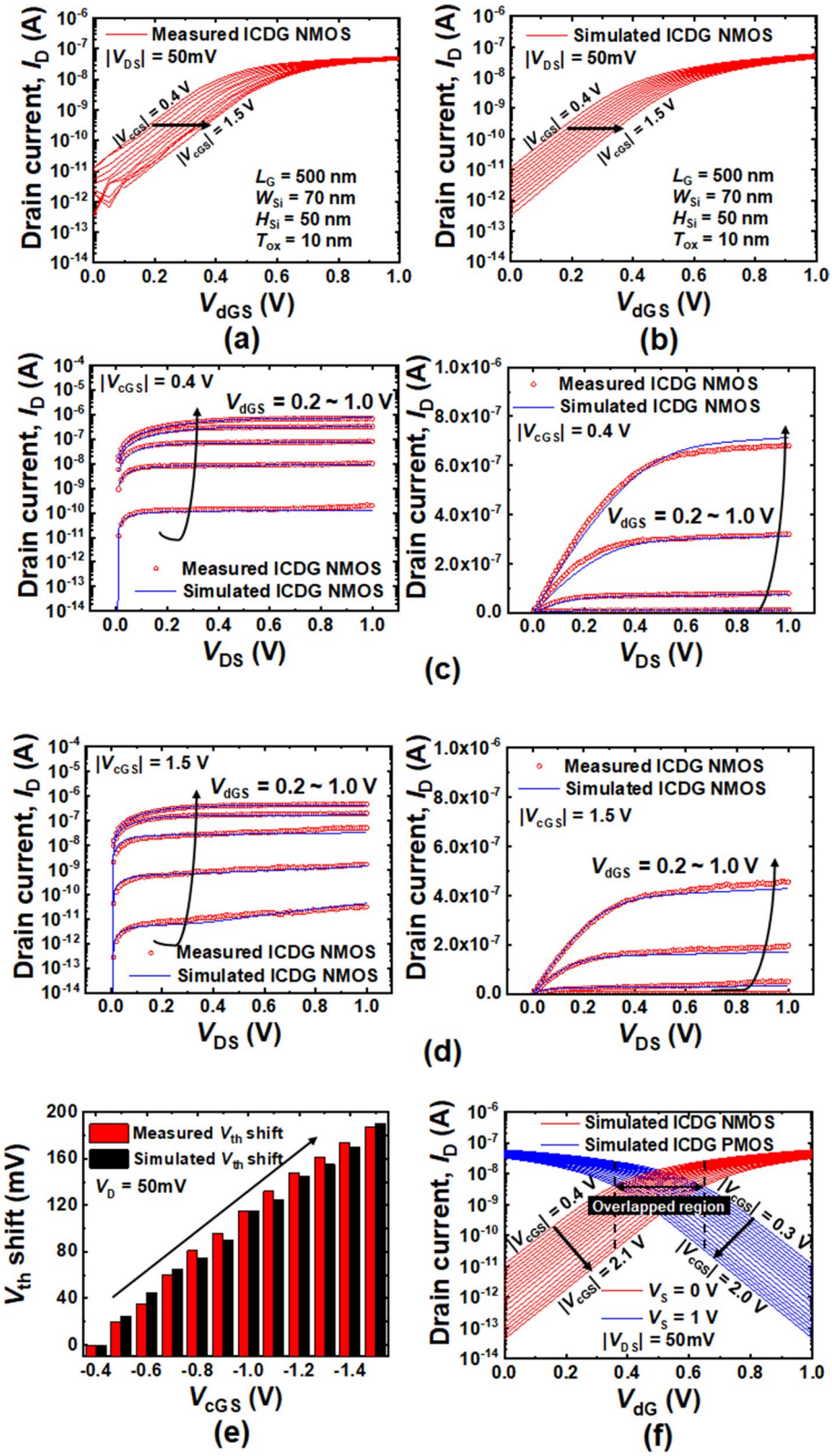
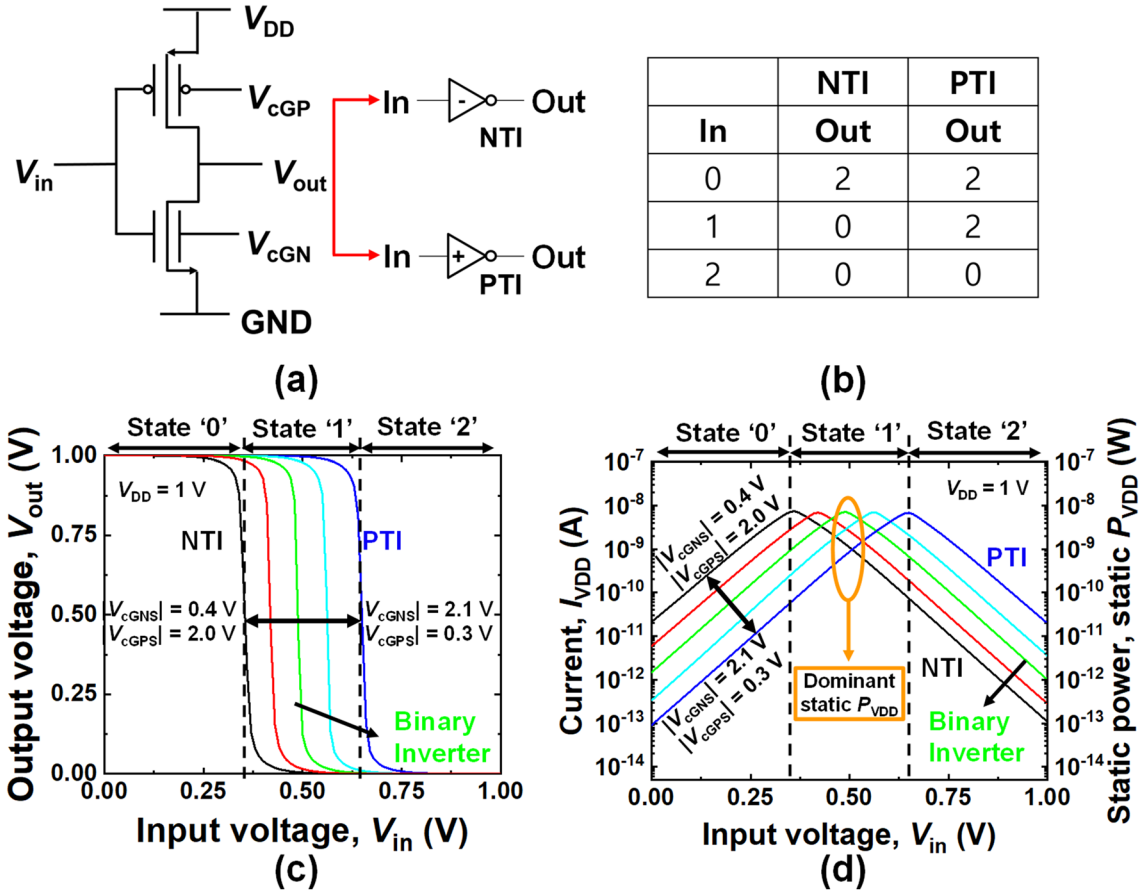



**Figure 2.** **(a)** Measured $I_D$-$V_{dGS}$ characteristics from the fabricated ICDG NMOS for various $|V_{cGS}|$. **(b)** Semi-empirically simulated $I_D$-$V_{dGS}$ characteristics according to various $|V_{cGS}|$. Superimposition of measured and simulated $I_D$-$V_{DS}$ characteristics of N-channel for **(c)** $|V_{cGS}|$= 0.4 V and **(d)** 1.5 V on the log-scaled *y*-axis and linear-scaled *y*-axis. **(e)** Linear $V_{th}$ shift by $V_{cGS}$. **(f)** Simulated $I_D$-$V_{dGS}$ characteristics of both ICDG NMOS and PMOS for various $|V_{cGS}|$.



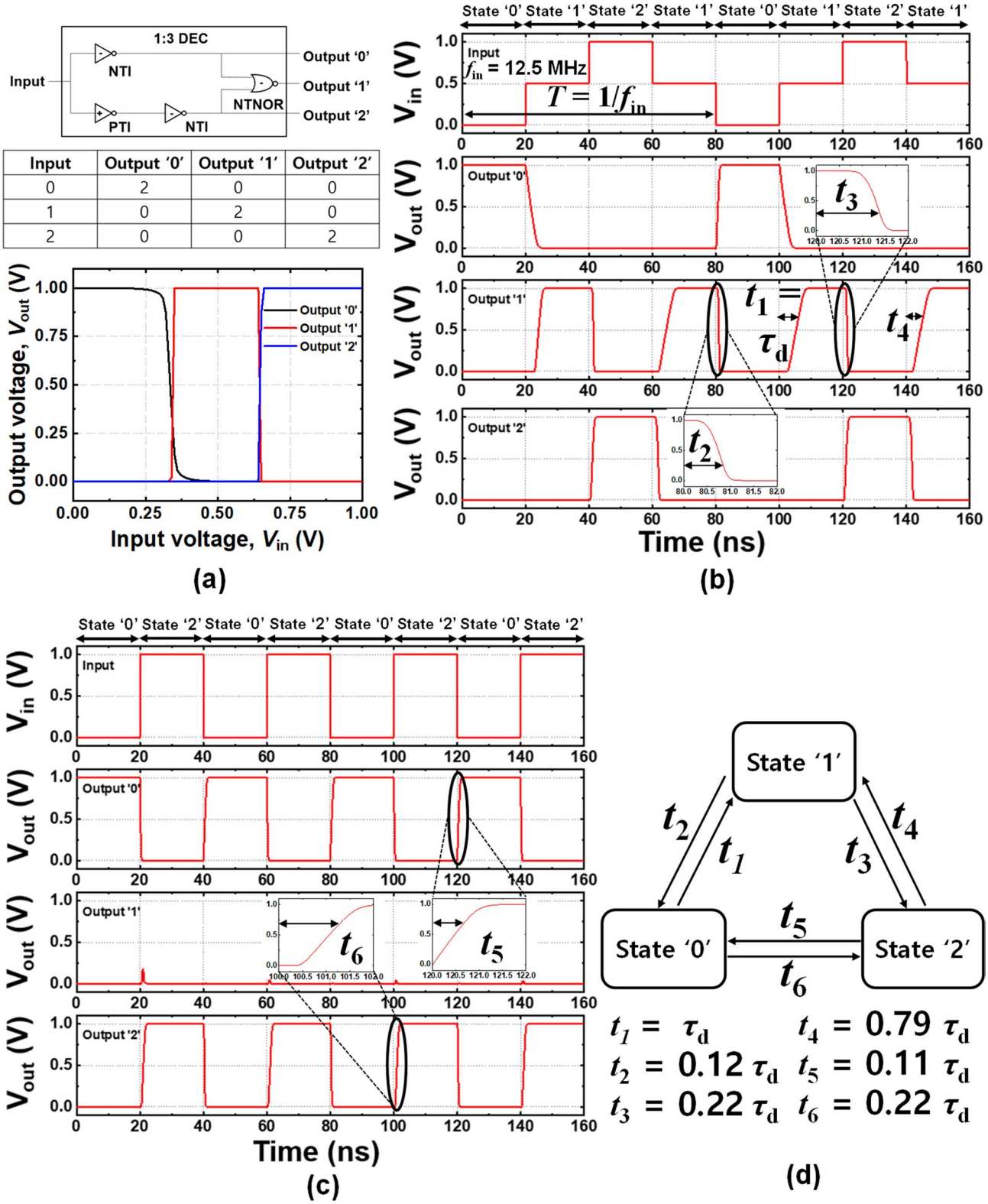

| | NTI | PTI |
|---|---|---|
| In | Out | Out |
| 0 | 2 | 2 |
| 1 | 0 | 2 |
| 2 | 0 | 0 |

**Figure 3.** **(a)** Complementary inverter circuits composed of ICDG NMOS and PMOS with each control gate. They can serve as the NTI and the PTI by adjusting $V_{cGN}$ and $V_{cGP}$. **(b)** Truth table of the NTI and PTI. **(c)** Input–output voltage transfer curves (VTCs) of the inverter circuit for various $|V_{cGNS}|$ and $|V_{cGPS}|$. **(d)** Current ($I_{VDD}$) from the $V_{DD}$ node to the ground node versus input voltage ($V_{in}$) and power consumption ($P_{VDD}$) versus input voltage ($V_{in}$).

$V_{th}$-modulation according to $V_{cG}$ can be performed with consideration of two conflicting demands: maximization of speed and minimization of static power consumption. Increment of $I_{on,'1'}$ through the $V_{cG}$ modulation can result in boosting speed of the ternary logic decoder (TLD). But, excessive increment of $I_{on,'1'}$ can adversely increase the static power consumption ($P$) of the TLD owing to a parallel shift of $V_{th}$, which provokes increment of leakage current. Thus, the optimization of $V_{cG}$ can be done with a well-known figure of merit, power-delay product ($PDP$) owing to the abovementioned trade-off relationship. The magnitude of $C_{gg}$ for N-channel and P-channel ICDG Si-NW MOSFETs was decreased as $L_G$ was decreased. As shown in Fig. 4c and d, as $L_G$ was decreased, $C_{gg}$ was continuously decreased, while $I_{on,'1'}$ was maintained by $V_{th}$-modulation. It means that delay time ($\tau_d$) of the TLD circuit is decreased by down-scaling.

Figure 6a and b show two transient current responses for an $L_G$ of 500 nm and an $L_G$ of 14 nm, respectively at input voltage frequency ($f_{in}$) of 12.5 MHz. The $f_{in}$ of 12.5 MHz was used from $T = 1/f_{in} = 80$ ns as shown in Fig. 4b first graph. When the input voltage signal abruptly switched from one state to another, charges were transferred from the power supply to the gate capacitors or load capacitors. And $|I_{VDD}|$ rapidly increased and temporarily overshot, thereafter it began to stabilize. As shown in Fig. 6b, the pulse width needed to induce the overshoot was significantly reduced by down-scaling from $L_G = 500$ nm to $L_G = 14$ nm. The stabilized $|I_{VDD}|$ depended on the applied $V_{in}$ (state of input). The magnitude of the stabilized $|I_{VDD}|$ for the input voltage of 0.5 V (state '1') was much higher than that for the other states, like the $|I_{VDD}|$ of the NTI and PTI shown in Fig. 3d. For an $L_G = 500$ nm, a total $P_{VDD}$ of 6.37 nW was calculated by integrating $V_{DD} \times |I_{VDD}(t)|$ with respect to the 2 cycle time ($2\,T = 160$ ns) and dividing it by the same time, i.e., $(\text{total } P_{VDD}) = [V_{DD} \cdot \int_{0\,ns}^{160\,ns} |I_{VDD}(t)|dt]/(160\,ns)$.

The TLD was evaluated in terms of $\tau_d$, $P$, and $PDP$. These values were semi-empirically extracted from the simulations, which were based on the fabricated device. Theoretically, $\tau_d$ can be reduced by $V_{th}$ engineering by biasing the control gate, as well as by device down-scaling. The above three metrics were changed by reducing the gate length ($L_G$), as summarized in Table 1. As shown in Fig. 4d, the propagation delay times, $t_1$ from state '0' to state '1' and $t_4$ from state '2' to state '1' were longer than the other transition times ($t_2$, $t_3$, $t_5$, and $t_6$) because $I_{on,'1'}$ is smaller than $I_{on,'0'}$ and $I_{on,'2'}$. In this work, the $\tau_d$ of TLD is predominantly governed by the longest transition time, $t_1$ ($t_1 > t_4$).




| Input | Output '0' | Output '1' | Output '2' |
|---|---|---|---|
| 0 | 2 | 0 | 0 |
| 1 | 0 | 2 | 0 |
| 2 | 0 | 0 | 2 |

**Figure 4.** **(a)** 1-to-3 ternary logic decoder circuit composed of NTI, PTI and NTNOR and the VTCs of output '0', output '1' and output '2'. **(b)** Transient ternary responses of output '0', output '1', output '2' versus time ($f_{in}$ = 12.5 MHz). **(c)** Transient binary responses for direct alteration between states '2' and '0'. **(d)** Diagram of state transition with propagation delay time.

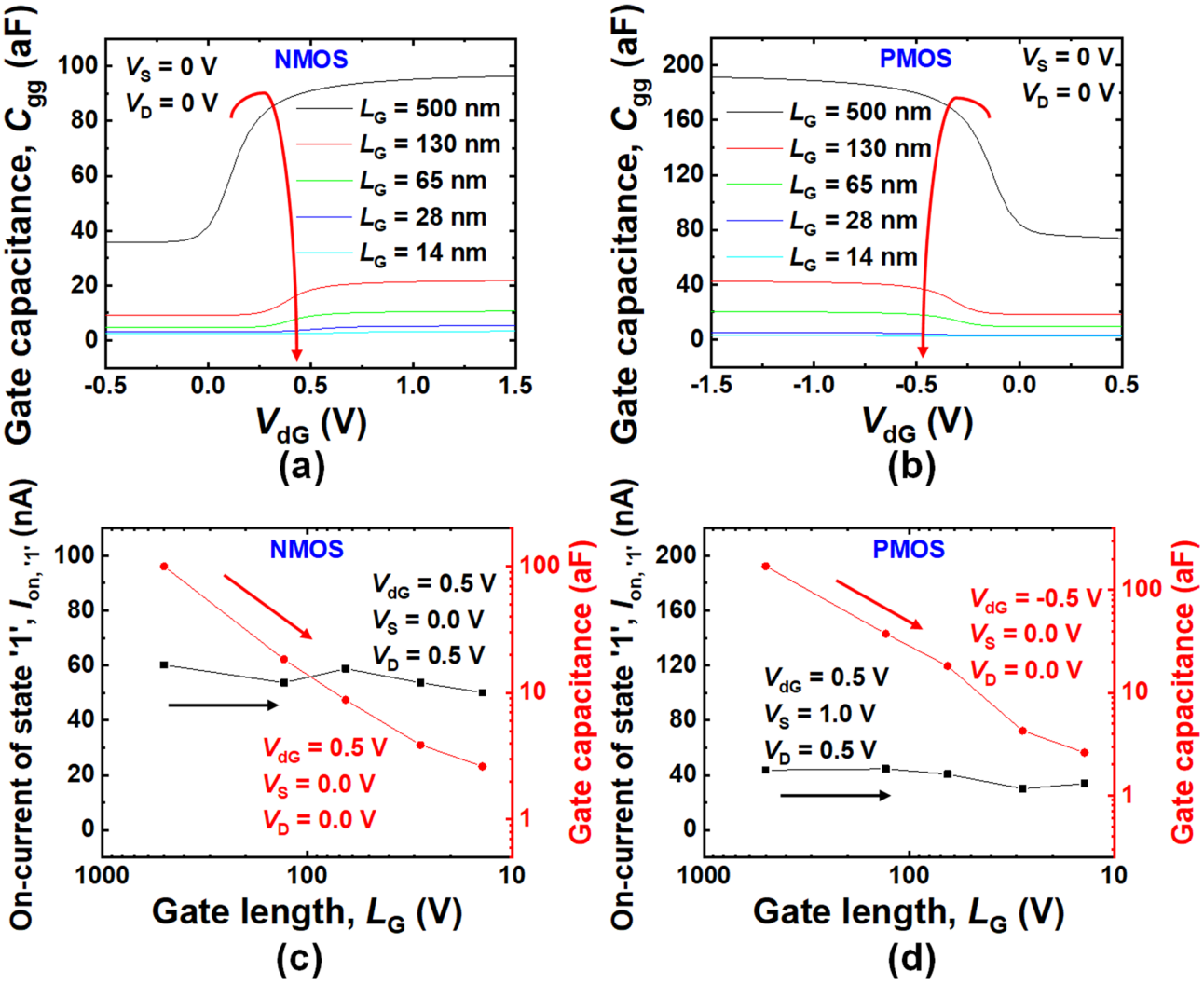



**Figure 5.** The $C_{gg}$-$V_{dG}$ characteristics of ICDG **(a)** NMOS and **(b)** PMOS depending on gate length ($L_G$) reduction. $I_{on,\ '1'}$ and $C_{gg}$ of ICDG **(c)** NMOS and (d) PMOS according to gate length reduction.

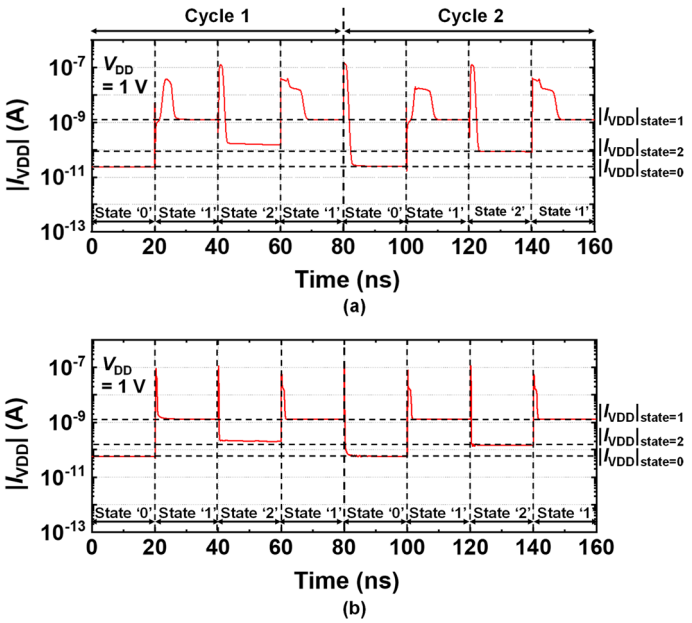



**Figure 6.** Transient response of $I_{VDD}$ versus time for **(a)** $L_G$ = 500 nm and **(b)** $L_G$ = 14 nm.

| Gate length ($L_G$) [nm] | Delay ($\tau_d$) [ns] | Possible operating frequency [GHz] | Power ($P$) [nW] (at $f_{in}$ [MHz]) | $PDP$ [aJ] |
|---|---|---|---|---|
| 500 | 5.57 | 0.045 | 6.37 (12.5) | 35.48 |
| 130 | 0.95 | 0.263 | 2.68 (48.1) | 2.55 |
| 65 | 0.44 | 0.568 | 2.20 (96.2) | 0.97 |
| 28 | 0.18 | 1.389 | 2.14 (223.2) | 0.39 |
| 14 | 0.085 | 2.941 | 1.90 (446.4) | 0.1615 |

**Table 1.** Power and delay time according to gate length scaling.

| | Type of devices | $V_{th}$-modulation | Number of transistors | Power ($P$) [nW] | Delay ($\tau_d$) [ps] | $PDP$ [aJ] |
|---|---|---|---|---|---|---|
| [18] | MOSFETs | Body Ion Implantation | 10 | 0.444 | > 23,000 | 10.2 |
| [35] | CNTFETs | Diameter Engineering | 16 | 11,800 | 8.24 | 97.2 |
| [36] | MOSFETs | CMOS Double Pass Logic | 12 | 13,000 | 140 | 1820 |
| [37] | CNTFETs | Diameter Engineering | 11 | 10,400 | 7.06 | 73.4 |
| [38] | CNTFETs | Diameter Engineering | 10 | 250,000 | 7.18 | 1795 |
| [39] | CNTFETs | Diameter Engineering | 9 | 9100 | 4.18 | 38.0 |
| This work | ICDG Si-NW MOSFETs | Electrical Control Bias | 10 | 1.90 | 85 | 0.16 |

**Table 2.** Benchmarking table of ternary logic decoder.

The possible operating frequency was calculated from $f = 1 / (4\tau_d)$[34]. Following a constant field scaling scenario with a scaling factor of $K$ (> 1), $f_{in}$ is proportional to $K$ for the down-scaling[1]. Therefore, the $f_{in}$ for a short $L_G$ becomes $f_{in}$·long $L_G$/short $L_G$. For example, an $f_{in}$ of 12.5 MHz for an $L_G$ of 500 nm can be increased to 48.1 MHz with an $L_G$ of 130 nm. $\tau_d$ was directly extracted and $P$ was extracted for each $f_{in}$ predicted by the abovementioned scaling rule for an $L_G$ of 500 nm, 130 nm, 65 nm, 28 nm, and 14 nm, as shown in Table 1. The $\tau_d$ of 5.57 ns for $L_G$ of 500 nm was drastically reduced to 0.085 ns for an $L_G$ of 14 nm. And the $P$ of 6.37 nW for an $L_G$ of 500 nm was also reduced to that of 1.90 nW for $L_G$ of 14 nm. In addition, the $PDP$ of 0.16 aJ was extracted from $P$ of 1.9 nW and $\tau_d$ of 0.085 ns for $L_G$ of 14 nm. The performance metrics of the proposed TLD are compared with the existing implementations, as shown in benchmarking Table 2[18,35–39].

The $SS$ of the ICDG Si-NW MOSFET in this experiment was approximately 120 mV/dec, due to the poor interface quality of the TEOS used as the gate oxide. This can be decreased to sub-80 nm/dec replacing the thermally grown oxide or using a high-$k$ dielectric material. Further improvement in the $SS$ will additionally reduce $\tau_d$ and $P$.

In this study, a ternary logic decoder (TLD) to allow the conversion from a ternary code to a binary code and vice versa has been demonstrated with independently controlled double-gate (ICDG) silicon-nanowire (Si-NW) MOSFETs. Feasibility of the TLD was explored by use of semi-empirical circuit-level simulations based on the measured device-level ICDG Si-NW MOSFET characteristics. Because the ICDG Si-NW MOSFET is not only suitable for a multi-$V_{th}$ scheme but also CMOS-compatible for mass-production, the proposed TLD would be a promising candidate to realize a MRS. Direct demonstration of the TLD with fully fabricated circuits is left as a further work.

## Methods

**Electrical measurements.** A semiconductor parameter analyzer (B1500A) was used to characterize the fabricated ICDG Si-NW MOSFETs. The transfer characteristics of the fabricated N-channel ICDG Si-NW MOSFET were measured at a constant $V_{DS}$ of 50 mV, whereas the $V_{dGS}$ was swept from 0 to 1 V.

**Device modeling.** The ICDG Si-NW MOSFETs were modeled and fitted with the SILVACO ATLAS TCAD simulator. A various physical models such as Schockly-Read-Hall (SRH), Bandgap Narrowing (BGN), Fermi–Dirac (FERMI), non-local Band-to-Band Tunneling (BTBT) and Trap-Assisted Tunneling (TAT) were involved.

**Circuit simulation for ternary logic decoder.** Using the experimentally modeled devices, the operation, performance, and power consumption of the TLD were verified using the ATLAS mixed-mode TCAD simulations. To simulate the transient response of the TLD, $V_{DD}$ and $V_{SS}$ were set to 1 V and 0 V respectively.

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## Author contributions
S.-J. Han, J.-K. Han, G.-J. Yun, and Y.-K. Choi conceived the idea and designed the experiment. S.-J. Han and J.-K. Han measured the electrical characteristic of the fabricated devices and conducted the SILVACO ATLAS TCAD simulations. S.-J Han and M. Seo conducted the down-scaling analysis. M.-S. Kim, J.-M. Yu, I.-W. Tcho, and G.-B. Lee analyzed experimental data. S.-J. Han and Y.-K Choi prepared the manuscript.

## Competing interests
The authors declare no competing interests.

## Additional information
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