


# Wafer-scale organic-on-III-V monolithic heterogeneous integration for active-matrix micro-LED displays

Received: 13 March 2023

Accepted: 10 October 2023

Published online: 01 November 2023

 Check for updatesLei Han<sup>1,2</sup>, Simon Ogier<sup>3</sup>, Jun Li<sup>1,2</sup>, Dan Sharkey<sup>3</sup>, Xiaokuan Yin<sup>1,2</sup>, Andrew Baker<sup>3</sup>, Alejandro Carreras<sup>3</sup>, Fangyuan Chang<sup>4</sup>, Kai Cheng<sup>5</sup> & Xiaojun Guo<sup>1,2</sup> 

The organic thin-film transistor is advantageous for monolithic three-dimensional integration attributed to low temperature and facile solution processing. However, the electrical properties of solution deposited organic semiconductor channels are very sensitive to the substrate surface and processing conditions. An organic-last integration technology is developed for wafer-scale heterogeneous integration of a multi-layer organic material stack from solution onto the non-even substrate surface of a III-V micro light emitting diode plane. A via process is proposed to make the via interconnection after fabrication of the organic thin-film transistor. Low-defect uniform organic semiconductor and dielectric layers can then be formed on top to achieve high-quality interfaces. The resulting organic thin-film transistors exhibit superior performance for driving micro light emitting diode displays, in terms of milliampere driving current, and large ON/OFF current ratio approaching  $10^{10}$  with excellent uniformity and reliability. Active-matrix micro light emitting diode displays are demonstrated with highest brightness of 150,000 nits and highest resolution of 254 pixels-per-inch.

Recent intensive research and development in micrometer scale III-V semiconductor light emitting diodes (micro-LEDs) shows great promise of creating a technology platform to overcome the limits of existing semiconductor displays for higher brightness, finer resolution, better endurance, more innovative form factors and functions<sup>1–9</sup>. However, a fundamental challenge is efficient and reliable heterogeneous integration of massive arrays of micro-LEDs with transistor pixel circuits for active-matrix (AM) addressing<sup>5,10,11</sup>.

Currently, the popularly used architecture, referring to the existing semiconductor display technologies, takes the light-emitting element as the front-plane and the thin-film transistor (TFT) circuit as the back-plane for integration<sup>12</sup>. Due to strict process conditions required for III-V LEDs, direct monolithic heterogeneous integration of III-V

LEDs onto the TFT backplanes is not feasible. Therefore, the epitaxially grown LED elements are detached from the sapphire or silicon substrates and then transferred onto the TFT backplanes. Using this type of approach, it is difficult to achieve high resolution arrays with reliable electrical conduction between all the TFTs and LEDs<sup>13–19</sup>. As a result, significant effort on redundancy design and post-process repairing is required<sup>20,21</sup>.

The other possible solution is to reverse the structure, but monolithic integration of the TFT array on top of the micro-LED plane also meets a fundamental difficulty. For the industry established inorganic TFTs, a high processing temperature ( $>350$  °C) is needed to form low defect density semiconductor/dielectric layers and interfaces for low leakage current and reliable high current driving<sup>22–24</sup>. Although

<sup>1</sup>School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, P. R. China. <sup>2</sup>National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University, Shanghai 200240, P. R. China. <sup>3</sup>SmartKem Ltd., Neville Hamlin Building, Thomas Wright Way, NetPark, Sedgefield TS21 3FG, UK. <sup>4</sup>School of Design, Shanghai Jiao Tong University, Shanghai 200240, P. R. China. <sup>5</sup>Enkris Semiconductor, Inc., Nanopolis Suzhou, 99 Jinji Avenue, Suzhou Industrial Park, Suzhou, Jiangsu province 215124, P. R. China.  e-mail: [x.guo@sjtu.edu.cn](mailto:x.guo@sjtu.edu.cn)

there were reported low temperature processed metal oxide TFT, the performance and stability were generally degraded<sup>25,26</sup>. The micro-LED pixels require the driving TFT to provide large current in the level from hundreds of microamperes to milliampere, and meanwhile have low enough leakage current to maintain good dark state<sup>1,27</sup>. The high-temperature TFT processes might cause cracks of the multi-layer metal contacts on top of the LED plane, resulting in increase of contact resistance and even failure of electrical connection<sup>28</sup>. The complex pixel circuit composed of at least 2 TFTs and one capacitor (2T-1C) and multi-layer interconnection make the AM TFT array even more difficult to be transferred from the original glass substrate onto the micro-LED plane.

Compared to the inorganic counterparts, the organic TFT (OTFT), using solution processed organic semiconductor (OSC) and dielectric layers, has advantage of forming high-quality channel layer and semiconductor/dielectric interfaces with facile processing at low temperature (<150 °C or even lower)<sup>12,29,30</sup>. Therefore, it could be directly fabricated onto the micro-LED plane without affecting integrity of the underneath layers. However, the large step profiles on the micro-LED plane surface due to presence of thick metal contacts and deep via structures cause difficulties to form thin and uniform OSC and dielectric layers on top by solution processing. Moreover, both the emitted light and the randomly trapped charges at the heterogeneous material interfaces might cause electrical performance fluctuations of the OTFTs.

This work develops an organic-last integration (OLI) technology to effectively address the above challenges of directly making high-performance OTFTs and large-scale circuits directly on top of non-even substrate surface. A thick polymer planarization layer and a metal shielding layer are deposited subsequently. The former is to smoothen the micro-LED plane surface, and the latter is to protect influence of light illumination on the OTFT on top. A “post-OTFT” via process is proposed to make the OTFT-to-micro-LED via interconnection after fabrication of the OTFT, so that the surface is intact before deposition of the OSC layer. Low-defect uniform OSC and dielectric layers can then be formed on top at low temperature (<150 °C) with high-quality metal-semiconductor and semiconductor-dielectric interfaces. The resulting OTFTs exhibit superior performance of milliampere driving current, low leakage current and large ON/OFF current ratio approaching  $10^{10}$  with excellent uniformity and reliability. AM micro-LED displays are finally demonstrated, with the highest resolution of 254 PPI and the highest brightness >150k nits, which are the best results so far among all reported TFT-driven AM micro-LED displays<sup>13,14,16–19,31</sup>.

## Results

### Organic-last integration structure

Figure 1a illustrates the proposed OLI structure with the OTFT AM array being directly fabricated on top of the micro-LED plane. The micro-LED plane is fabricated on a 4-inch sapphire substrate using the industry standard metal-organic chemical vapor deposition (MOCVD) processes, containing layers of n-doped GaN (N-GaN), multi-quantum-well (MQW), p-doped GaN (P-GaN) and ITO electrode. The OTFT is in a top-gate bottom-contact (TGBC) structure with a metal shielding layer underneath. The detailed process flow is described in Supplementary Fig. 1. To make an AM array, a micrometer-scale thick metal interconnect layer on the micro-LED plane is needed for the power supply ( $V_{DD}$ ) and ground ( $V_{SS}$ ) lines to support large current loading. The large topography of the thick metal layer causes a high risk of electrical shorts at the crossover edges between the power interconnects and the data interconnects on top. To address this issue, a thick polymer planarization layer is deposited onto the micro-LED plane before fabrication of the metal layer for both the data interconnects and the bottom shielding of the OTFTs. The subsequently deposited buffer layer provides a suitable surface energy for uniform crystallization of

the OSC channel and form a high-quality back-channel interface. As shown by the scanning electron micrograph (SEM) in Fig. 1b, the large step (~2.2  $\mu\text{m}$ ) is smoothened with this planarization layer for data interconnects on top, which brings excellent electrical insulation properties between the two metal layers at the crossover regions (Supplementary Fig. 2).

To connect the micro-LED contact to the drain of the OTFT, the conventional “pre-OTFT” via process is forming the via interconnection first and the OTFT afterwards (the upper of Fig. 1c). However, due to the thick planarization and buffer layers, formation of deep via structures would interrupt the subsequent crystallization of the OSC layer and continuity of the solution deposited passivation layer on top. Moreover, the plasma-based dry etching for making the via would induce damages to the buffer layer surface and ion charge trapping, which in turn affect the crystallization and charge distribution of the OSC channels, respectively.

A “post-OTFT” via process is developed in this work, where the OTFT-to-micro-LED via is fabricated after fabrication of the OTFT (the bottom of Fig. 1c). Therefore, the buffer layer surface can be maintained to be fully planar and free of ion charge trapping before OSC deposition, and this enables the best OSC crystallization process and uniform electrical characteristics. The passivation layer covers all the device areas after completing the OTFT processes. For the integration, the planarization, buffer, OSC, gate insulator, and passivation layers are all deposited with spin-coating processes. The metal electrodes and interconnects are formed through sputtering and then patterning with photolithography and wet-etching. The via and OSC patterning are completed with dry etching. All the processes can be done with existing III-V micro-LED fabrication facilities. Such low temperature (<150 °C) OLI processes can thus be well compatible with micro-LED processes for direct fabrication of the AM array on top without affecting the micro-LED performance (Supplementary Fig. 3).

### Electrical performance

To drive micro-LED displays, the driving OTFT needs to provide high current in a limited pixel area for both bright luminance and high resolution. For that, in addition to improving the OSC channel mobility, the channel length needs to be minimized for high-density integration and large channel width to length ratio ( $W/L$ ). Most of previously reported high mobility OSCs used top-contact device structures with long channel lengths ( $L > 50 \mu\text{m}$ )<sup>32–37</sup>. Due to the vulnerability of the OSC layers, it is challenging to process fine-resolution metal electrodes on top for shorter channel devices. Moreover, since the channel resistance decreases at shorter channel lengths, the contact resistance is becoming more significant, therefore this is often a bottleneck for further performance improvements in OTFT devices<sup>38–40</sup>.

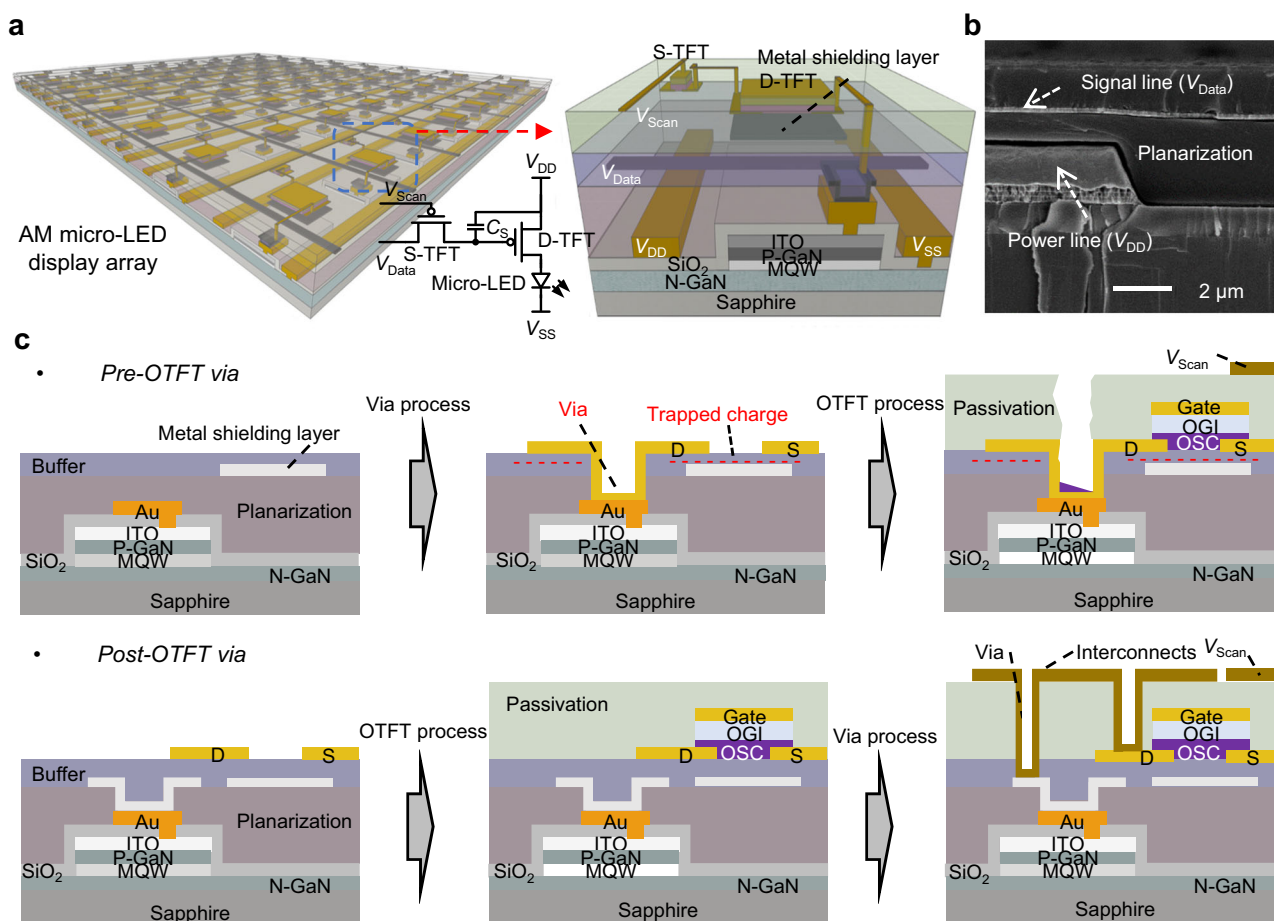
In this work, the TGBC architecture is chosen for its compatibility with fine-resolution metal electrode processes and larger injection area at the contact regions for smaller contact resistance<sup>39,40</sup>. Figure 2a illustrates the structure and the material stack for the fabricated OTFT on top of the micro-LED plane. A blended solution of small molecule OSC and polymer semiconductor binder in tetralin solvent is used to form the channel of high carrier mobility. The small molecule OSCs own merits of highly crystalline structures and purity for high mobility and low trap density, but face challenges of achieving uniform crystallization over large area. Adding polymer semiconductor binder of good miscibility and energy level matching with the small molecule OSC is beneficial for controlling crystallization and obtaining uniform morphology<sup>27,41–43</sup>. As a result, both the device performance and uniformity can be greatly improved compared to that of the devices using the pure small molecule OSC (Supplementary Fig. 4). The self-assembly monolayer (SAM) interfacial layer on the gold source/drain electrodes minimizes the energy barrier for hole injection in ON-state, and suppresses minority charge injection for low leakage current<sup>27,44</sup>.

Choosing a proper SAM layer can also help to improve the OSC crystallization on top for high-quality metal-semiconductor interface. Different SAMs are used to modify the contact electrode surface, resulting in various surface morphologies of the OSC layer (Supplementary Fig. 5). The measured  $I_D$ - $V_{GS}$  curves and extracted mobility values of the fabricated devices using different SAMs prove that 3-Fluoro-4-Methoxythiophenol (3-F, 4-OMeBT) is the most suitable SAM for high apparent mobility due to improved crystallization of the OSC film on the contact electrodes (Supplementary Fig. 6). With electrode treatment of the selected SAM, the contact resistance of the devices is significantly reduced (Supplementary Fig. 7).

In the bi-layer structure gate dielectric with overall thickness of around 550 nm, the CYTOP layer forms a non-polar low-trap interface with the OSC layer for high mobility and suppressed charge trapping, and the polymer sputtering resistant layer (SRL) can sustain the gate metal sputtering process and wet etching process on top for low gate dielectric leakage current<sup>45-47</sup>. The measured typical transfer ( $I_D$ - $V_{GS}$ ) and output ( $I_D$ - $V_{DS}$ ) of the OTFT with  $L = 3.7 \mu\text{m}$  and  $W = 1370 \mu\text{m}$  in a corbino structure are presented in Fig. 2b, showing typical field effect transistor behaviors with negligible hysteresis, large ON-state current of about 1 mA and high ON/OFF ratio near  $10^{10}$ . The non-ideal output characteristics in the saturation regime is due to relatively small gate dielectric capacitance (about  $4.6 \text{ nF/cm}^2$ ), and can be improved by adopting high- $k$  polymer dielectric material for stronger electrostatic

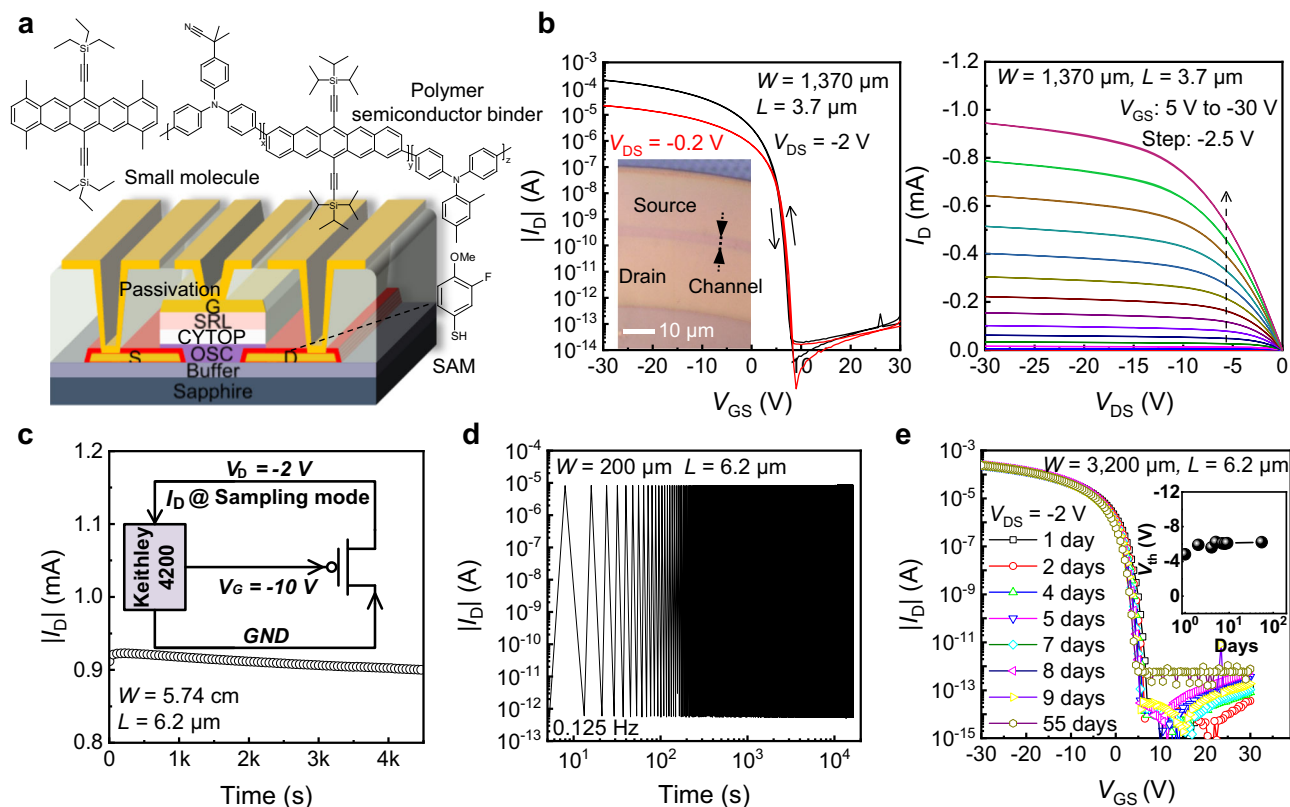
control of the channel from the gate. The negligible contact resistance, as characterized by the transmission line measurement (TLM) method on devices of five channel lengths (Supplementary Fig. 8), enables the device to maintain a high apparent mobility value of  $2.6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at such a short channel for large ON-state current.

The operational stabilities of the OTFTs are vital for AM micro-LED driving. In the pixel circuit, the two type OTFTs are operated in different modes, and thus require different designs. For the pixel driving OTFT, large channel width is needed to provide the required large driving current for micro-LEDs. Therefore, a wide channel ( $W = 5.74 \text{ cm}$ ,  $L = 6.2 \mu\text{m}$ ) OTFT is used to characterize its constant current bias stress stability. At a continuous stress current of nearly 1 mA for 4,500 s, the device presents negligible change of the output current (Fig. 2c). A narrower channel OTFT ( $W = 200 \mu\text{m}$ ,  $L = 6.2 \mu\text{m}$ ) is adopted to characterize the operational stabilities for pixel switches. Figure 2d shows that, after continuous dynamic switching for  $10^4$  s, the device maintains the high ON/OFF ratio. Negative bias stress (NBS) and positive bias stress (PBS) stability are also characterized, and at both cases the devices show negligible shift after 2 hours continuous bias stress (Supplementary Fig. 9). The excellent operational stabilities of the devices are attributed to the low trap channel interface between the low polar gate insulator (GI) layer and the OSC channel of smooth surface<sup>27</sup>. After being stored in ambient atmosphere with a relative humidity (RH) up to 84% for 55 days, the fabricated OTFT on the micro-



**Fig. 1 | Organic-last integration (OLI) structure.** **a** Illustration of the proposed OLI structure with the organic thin film transistor (OTFT) active-matrix (AM) array being directly fabricated on top of the micro-LED plane. The pixel driving circuit is based on 2T-1C (T: Transistor C: Capacitor) and contains driver TFT (D-TFT), switch TFT (S-TFT), storage capacitor ( $C_s$ ), micro-LED, signal lines ( $V_{Scan}$ ,  $V_{Data}$ ) and power lines ( $V_{DD}$ ,  $V_{SS}$ ). Specifically, micro-LED is composed of N-doped GaN (N-GaN), multi-quantum-well (MQW), P-doped GaN (P-GaN), indium tin oxide (ITO)

electrode. **b** Scanning electron micrograph (SEM) of the crossover structure between the power line and the data interconnect with a thick polymer planarization layer. **c** Illustration of the advantages with the proposed “post-OTFT” via compared to the conventional “pre-OTFT” via process for electrical connection between the OTFT and the micro-LED, and the OTFT contains source (S)/drain (D) electrodes, organic semiconductor (OSC) layer, organic gate insulator (OGI) layer and gate electrode.



**Fig. 2 | Electrical performance of the fabricated OTFT on top of the micro-LED plane.** **a** The structure and the material stack for the fabricated OTFT in a top-gate bottom-contact (TGBC) architecture. **b** The measured transfer ( $I_{\text{D}}-V_{\text{GS}}$ ) and output ( $I_{\text{D}}-V_{\text{DS}}$ ) of the device with channel width ( $W$ ) of 1370  $\mu\text{m}$  and channel length ( $L$ ) of 3.7  $\mu\text{m}$ . **c** The measured evolution of drain current at a continuous stress of nearly 1 mA for 4500 s with a wide channel OTFT ( $W = 5.74 \text{ cm}$ ,  $L = 6.2 \mu\text{m}$ ). **d** The

measured ON/OFF current under continuous dynamic switching for 10<sup>4</sup> s with a narrower channel OTFT ( $W = 200 \mu\text{m}$ ,  $L = 6.2 \mu\text{m}$ ). **e** The measured storage stability of device under high relative humidity (RH) atmosphere, indicating the robustness of passivation layer. Inset shows the evolution of threshold voltage ( $V_{\text{th}}$ ) during 55 days.

LED plane exhibited negligible change of the measured electrical characteristics (Fig. 2e), indicating the excellent storage stability. After storage for 180 days in the ambient, the slight increased leakage current can recover to the original level with a short-term low-temperature annealing (Supplementary Fig. 10). Such a variation of leakage current doesn't affect the display driving, since it remains in the very small level of 10<sup>-12</sup> A. In practical application, a better encapsulation instead of using a simple thin polymer dielectric layer can be used to protect the intrinsic part from moisture influence.

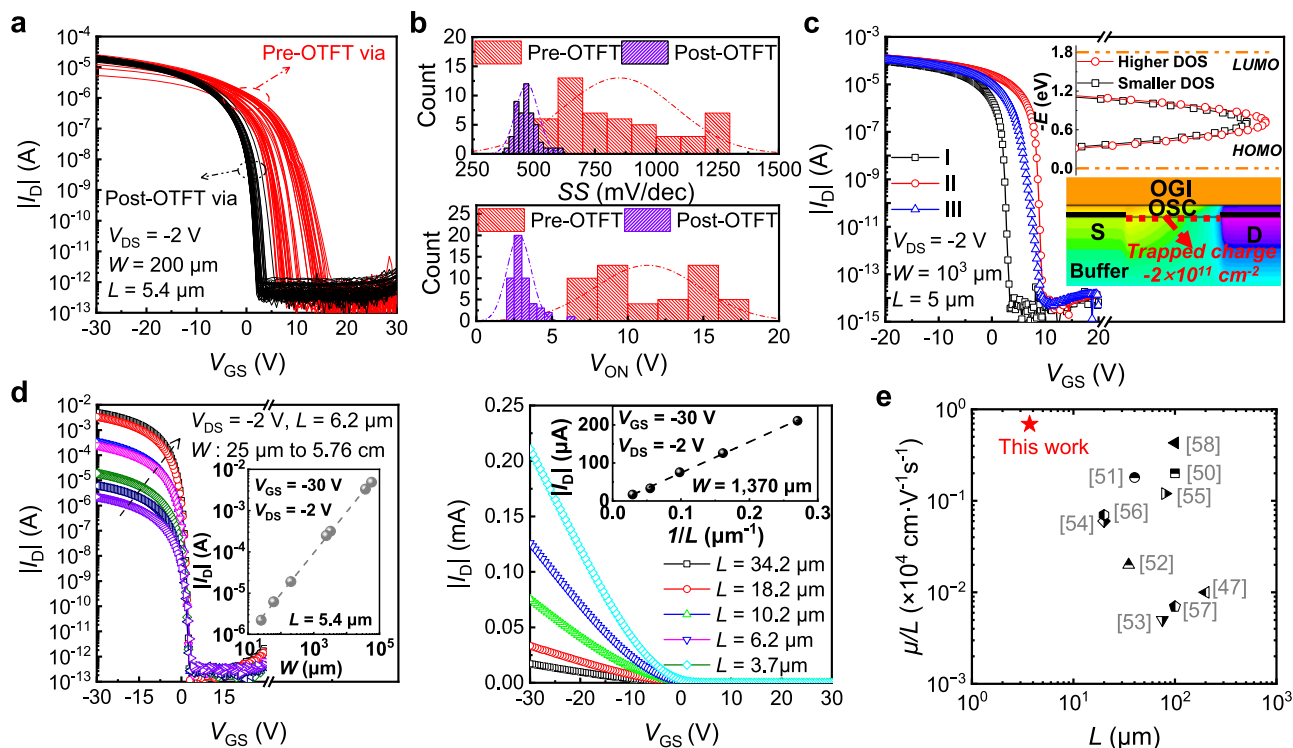
### Uniformity and scalability

The measured transfer characteristics ( $I_{\text{D}}-V_{\text{GS}}$ ) for 100 devices on 4-inch size wafer of 3 samples based on the “post-TFT” and “pre-OTFT” via processes are compared in Fig. 3a. The uniformity in terms of the turn-on voltage ( $V_{\text{ON}}$ ) and the subthreshold swing (SS) are greatly improved with the “post-OTFT” via (Fig. 3b). The large fluctuation of  $V_{\text{ON}}$  ranging from 6.5 V to 17.5 V with the pre-OTFT via is caused by dry-etching induced random ion charge trapping into the buffer layer. The SS is related to the sub-gap trap states at the channel interface. A large spread of SS values with the “pre-OTFT” via process is ascribed to uncontrollable OSC crystallization caused by the plasma etching process-induced surface roughening of the buffer layer (Supplementary Fig. 11). With the “post-OTFT” process, the buffer layer is intact before fabrication of the OTFT, and thus both charge trapping and surface roughening by the plasma dry etching is suppressed. Specifically, the roughness of buffer layer without RIE process is decreased from 9.70 nm to 0.94 nm, greatly improving uniformity and morphology of OSC layer because the thickness of OSC layer is around

30 nm, proven by the polarized optical micrographs in Supplementary Fig. 12. As a result, the OTFTs can be fabricated onto the micro-LED plane to have reliable electrical connections to the underneath micro-LEDs and achieve excellent uniformity of both  $V_{\text{ON}}$  and SS, which is as well as that with the devices on glass substrate (Supplementary Fig. 13). TCAD simulation also reveals that presence of charge trapping in the buffer layer causes shift of  $V_{\text{ON}}$ , and variation of the sub-gap trap density of states (DOS) causes change of the SS (Fig. 3c). Detailed simulation setting is included in “Methods” section.

With the “post-OTFT” via process, the fabricated OTFTs on the micro-LED plane achieve uniform electrical characteristics, so that the extracted current at the same electrical bias shows excellent linearity with both the channel width ( $W$ ) and the inverse of the channel length ( $1/L$ ) in a wide range (Fig. 3d). Such a scalability brings great convenience for device and circuit designs of different purposes, which require various geometries and dimensions for the current driving and pixel switch OTFTs.

There have been significant efforts on improving the operation frequency of OTFTs by making ultra-scaled channels, reducing the gate to source/drain overlaps and adopting inorganic high- $k$  gate dielectric layers<sup>48–50</sup>. To drive micro-LED displays, achieving large driving current in a limited pixel area is more important. Therefore, the ratio of the apparent mobility to the channel length ( $\mu/L$ ) is chosen as the figure-of-merit to evaluate the current driving capability of the device excluding influence the GI capacitance. Moreover, it is preferred to being compatible with existing spin-coating processes for large-area integration on top of the micro-LED plane. Figure 3e compares the  $\mu/L$  value versus  $L$  (representing the capability for high



**Fig. 3 | Uniformity and scalability of the fabricated OTFTs based on the post-OTFT via structure.** **a** The measured transfer characteristics ( $|I_b|$ - $V_{GS}$ ) for 100 devices on 4-inch size wafer of 3 samples based on the “post-TFT” and “pre-OTFT” via processes. **b** The statistical distribution of the extracted turn-on voltage ( $V_{ON}$ ) and subthreshold swing (SS) values of the OTFTs. **c** Transfer characteristics ( $|I_b|$ - $V_{GS}$ ) obtained using TCAD device simulations on condition of different sub-gap density of state (DOS) profiles and interfacial charge trapping (I: Without interfacial

trapped charge and low sub-gap DOS of  $10^{15} \text{ cm}^{-3} \text{ eV}^{-1}$ ; II: With trapped charge and low sub-gap DOS of  $10^{15} \text{ cm}^{-3} \text{ eV}^{-1}$ ; III: With trapped charge and high sub-gap DOS of  $2 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ , which are shown in the inset. **d** Measured transfer characteristics ( $|I_b|$ - $V_{GS}$ ) of devices with different channel width ( $W$ ) and channel length ( $L$ ), and linear relationship between the extracted ON-state current (Measured  $I_b$  when biased at  $V_{GS} = -30 \text{ V}$  and  $V_{DS} = -2 \text{ V}$ ) and  $W/L$ . **e** Comparison of  $\mu/L$  versus  $L$  among reported OTFTs with solution-processed OSC and OGI layers<sup>45, 51–59</sup>.

integration density) of the device in this work to previously reported results of OTFTs made of solution-processed OSC and GI layers. The device in this work has the largest  $\mu/L$  at the smallest layout footprint for high-resolution integration.

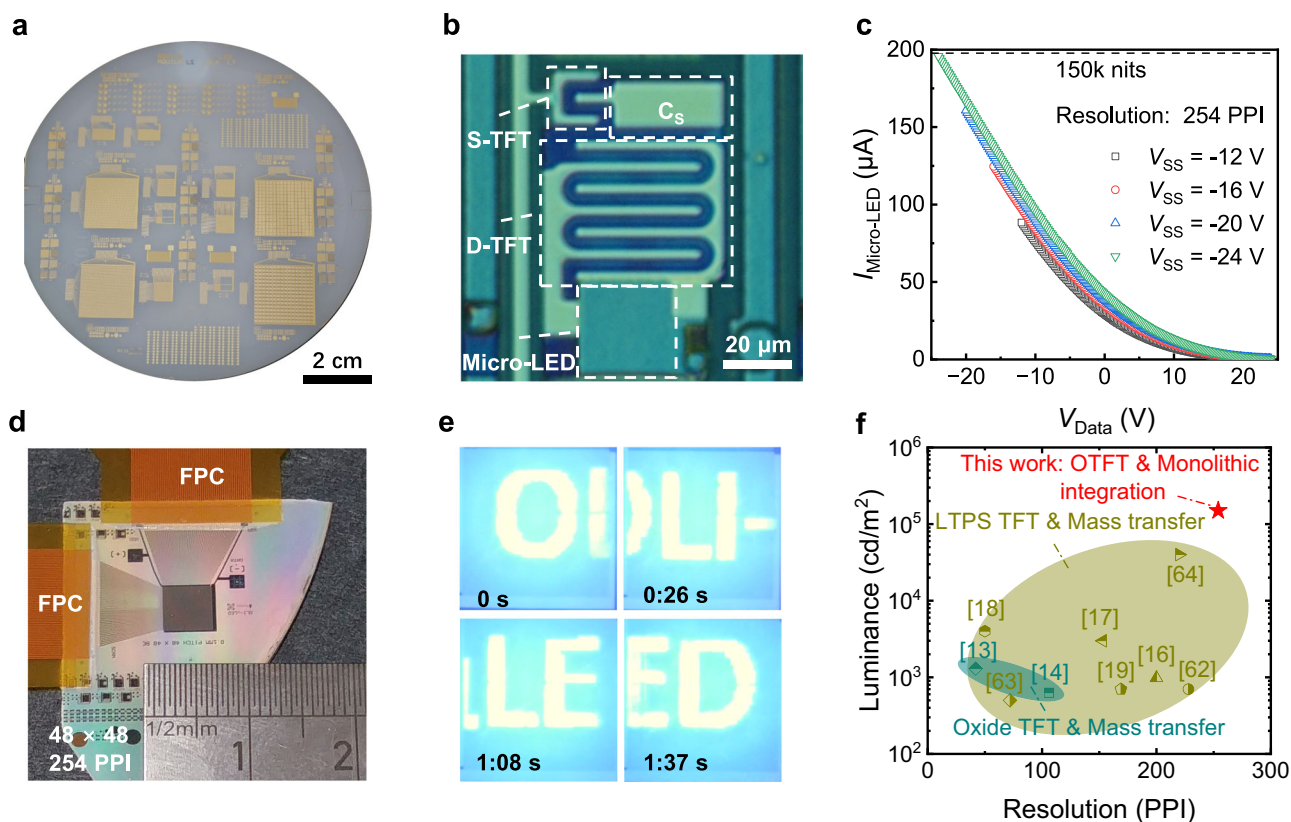
### Display integration

AM micro-LED arrays of different resolution using the 2T-1C pixel design (ranging from 25.4 PPI to 254 PPI) were fabricated on 4-inch sapphire wafer based on the proposed OLI integration approach, as shown in Fig. 4a. The optical micrograph of the fabricated 254 PPI pixel with a pixel size of  $100 \mu\text{m} \times 100 \mu\text{m}$  is given in Fig. 4b. The area of the micro-LED is  $28 \mu\text{m} \times 26 \mu\text{m}$ , and the driver TFT (D-TFT) with a dimension of  $330 \mu\text{m}/2.5 \mu\text{m}$  occupies an area of  $56 \mu\text{m} \times 42 \mu\text{m}$  by using a multi-finger layout design. A maximum driving current close to 0.2 mA in a pixel area of  $100 \mu\text{m} \times 100 \mu\text{m}$ , corresponding to a bright luminance near 150k nits (Supplementary Fig. 14), can be reached by modulating the supply voltage ( $V_{SS}$ ) and the data voltage ( $V_{Data}$ ) (Fig. 4c). Figure 4d presents the photo of the  $48 \times 48$  254 PPI AM micro-LED panel being connected to an external driving system through flexible printed circuit (FPC) bonding. Firework and words “O” “L” “I” “L” “E” “D” were dynamically displayed at a frame rate of 60 Hz (Supplementary Movie 1). The snapshots captured from the video are given in Fig. 4e (the bright background is caused by light scattering in the sapphire substrate layer, and can be suppressed by optical structure design). This is the firstly reported high resolution OTFT driven AM micro-LED display in the literature. Certainly, TFTs with a higher mobility like that of metal oxide TFTs or even polycrystalline silicon TFTs in the display industry would be more preferred to driving AM micro-LED displays. However, these inorganic TFTs normally require complex vacuum-based deposition and high-temperature annealing

processes, which would bring significant thermal and mechanical stresses to the underneath layers of micro-LEDs for monolithic integration. Moreover, additional expensive facilities are required to be added to complete the processes. The OTFTs, using low-temperature solution processed OSC and polymer dielectric layers, can have minimal influence to the underneath layers, and only need to adding simple solution coating facilities (e.g. spin-coating). This work shows that, even with an OTFT of mobility less than  $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , such an OLI approach enables to achieve a display panel of the highest luminance and resolution among the reported TFT-driven AM micro-LED displays (Fig. 4f). By increasing the OSC mobility and gate insulator capacitance, and adopting shorter channel device design, the display performance can be much improved further.

### Discussion

An organic-last-integration (OLI) technology is developed for wafer-scale heterogeneous integration of high-performance OTFTs and high-density active-matrix arrays on non-even substrate surface using solution-based approaches. A “post-OTFT” via process is proposed to form low-defect uniform organic semiconductor and dielectric layers on top to achieve high-quality interfaces. The resulting OTFTs exhibit superior performance for driving micro-LED displays, in terms of milliampere driving current, and large ON/OFF current ratio approaching  $10^{10}$  with excellent uniformity and reliability. The first OTFT-driven active-matrix micro-LED displays are demonstrated with highest brightness of 150,000 nits and highest resolution of 254 pixels-per-inch. This work would open a route for realizing active-matrix micro-LED displays through direct fabrication of high-density OTFT arrays onto the micro-LED plane with fully compatible processes. It is expected to apply the similar strategy in this work to higher mobility



**Fig. 4 | Display integration and demonstration.** **a** Photo image of the fabricated AM micro-LED arrays on 4-inch sapphire substrate based on the proposed OLI integration approach. **b** Optical micrograph of high-resolution (254 PPI) pixel with multi-finger source/drain design. **c** The measured driving current passing through micro-LED under different voltages for high luminance, with highest luminance of 150,000 nits. **d** Photo image of the  $48 \times 48$  254 PPI AM micro-LED panel being

connected to an external driving system through flexible printed circuit (FPC) bonding. **e** The snapshot images captured from the video, which dynamically displayed the words “O” “L” “I” “L” “E” “D” through the 254 PPI AM micro-LED display at a frame rate of 60 Hz. **f** Comparison of the resolution and brightness of the AM micro-LED display using the monolithic OLI approach with previously reported ones based on inorganic TFTs<sup>13,14,16–19,60–62</sup>.

small molecule OSCs for continuous improving the device performance, which is worth further investigation. The device performance can also be improved by reducing the channel length and adopting high- $k$  dielectric materials to enlarge the gate dielectric capacitance.

## Methods

### Materials for the OTFT

All the layers except for metal layers were based on organic materials by solution process. From bottom to top, acrylate polymer dielectric was used for buffer layer due to its surface energy and reduced roughness. 3-Fluoro-4-Methoxythiophenol (3-F, 4-OMeBT) self-assembled monolayer (SAM) molecule was dissolved in isopropanol to modify the source-drain (S-D) electrodes for smaller injection barrier. OSC ink was composed of small molecule (triethyl(2-(1,4,8,11-tetramethyl-13-[2-(triethylsilyl)ethynyl]pentacen-6-yl)ethynyl)silane) and polymer semiconductor binder dissolved in tetralin at the weight ratio of 0.4%:0.8%:98.8%. Organic gate insulators consist of CYTOP (CTL-809M) and sputter resistant layer (SRL). TRUFLEX™ PV was exploited for passivation layer.

All the electrodes (S-D, top gate, and interconnect) were based on Au except for bottom gate. Mo/Al/Mo was chosen for bottom gate with a larger thickness for better light blocking property.

### Monolithic integration process of OTFT circuit with micro-LED

Following metallization of the thick Au layer, the substrate was re-planarized using a thick layer of TRUFLEX™ planarizer (a UV crosslinkable acrylate polymer) deposited by spin coating and cured under broadband (i.g,h line) UV light in air ( $4200 \text{ mJ/cm}^2$ ). A light  $\text{O}_2$  plasma

treatment was conducted to increase surface energy of substrate with high topography for improving wettability of planarization layer onto substrate. Also, a thiol-based adhesion promoter was applied by spin coating in IPA to aid adhesion of the planarizer to the Au areas. Following crosslinking the wafer was baked at  $150^\circ\text{C}$  for 60 min. To form vias down to the Au contact pads, a Si813 resist was spin coated on top of the planarizer and baked on a hotplate. It was then exposed using a Heidelberg MLA direct lithography system (405 nm exposure) and developed in 2.38% TMAH developer in water to form the resist mask for the vias. The vias were then formed by dry etching (RIE  $\text{O}_2$ , Oxford plasma lab 800+) for 7.5 minutes. Following etching the sample was flood exposed to UV and the remaining protective resist removed in TMAH developer.

A Mo/Al/Mo tri-layer was deposited by sputtering for the back-gate layer. It was patterned by photolithography and wet etching (Phosphoric/Acetic/Nitric acid in water) to form the electrodes for the back gate of the transistor. The layer also acts as a light blocking layer to prevent doping of the OSC by light. After this a base-layer dielectric (TRUFLEX™ base-layer) was spin coated and cured in a similar way to the planarizing layer. Following this, the Au (50 nm thick) source-drain (S-D) electrodes were deposited by sputtering and patterned by photolithography and wet etching (KI/I in water). After patterning the source/drain electrode, the sample was exposed to a light plasma treatment to increase the surface energy of the base-layer followed by spin coating of the self-assembled monolayer (SAM) and OSC with baking at  $100^\circ\text{C}$  for 1 minute following the spin coating. The organic gate insulator (OGI) layers were composed of CYTOP and an acrylate polymer-based sputter resistant layer (SRL)<sup>47</sup>. Specifically, CYTOP was

firstly spin coated at the speed of 1,500 rpm for 20 s and baked at 50 °C, 100 °C for 20 s and 60 s, respectively. SRL was spin coated directly onto CYTOP layer at speed of 500 rpm for 10 s and then 1,250 rpm for 180 s and then UV cured using broadband wavelength mercury lamp (4,200 mJ/cm<sup>2</sup>) under N<sub>2</sub> flow and finally baked at 120 °C for 5 minutes. The measured contact angle of the SRL solution with added surfactant on top of the hydrophobic CYTOP surface is 43°, showing good wetting property<sup>47</sup> (Supplementary Fig. 15). Then the gate metal (GM, 50 nm Au) was deposited by sputtering and patterned by photolithography. Following resist strip (flood-expose-develop) the samples were etched (RIE, O<sub>2</sub>/Ar) to remove the areas of OSC/OGI/SRL that were not covered by the gate metal. Etching proceeded into the base-layer but was stopped short of the back-metal layer. Then the passivation layer (TRUFLEX™ PV) was deposited by spin coating and baked at 115 °C for 1 minute. It was crosslinked by UV curing (4,200 mJ/cm<sup>2</sup>) and then baked for a further 5 minutes at 120 °C. Via holes were patterned in a similar way to the planarization layer, and the etching was continued until the via reached the back-gate layer. In this way the vias could connect back-gate, SD, GM and interconnect metals. Lastly, the interconnect layer (50 nm Au) was deposited by sputtering and patterned using photolithography and wet etching.

### Device characterization

All the electrical test were conducted based on a semi-automatic probe station (Wentworth) connected to a Keithley SCS 4200 parameter analyzer in an air atmosphere.

Constant current bias stability was tested based on the following condition:  $V_G$  and  $V_D$  were set to be -10 V and -2 V, respectively. Test mode of Keithley SCS 4200 parameter analyzer was changed from sweeping mode to sampling mode with frequency about 1 s and maximum number of 4096 to continuously collect drain current ( $I_D$ ).

Dynamic switching stability was characterized based on sweeping mode and the bias condition was as follows: Gate terminal was set to be 'Voltage list sweep' and the applied voltages were +20 V/-20 V. Drain was biased at -2 V and drain current was collected at each gate voltage.

Ambient stability was tested based on the same device with channel width to length ratio ( $W/L$ ) of 3200 μm/6.2 μm. There was no pre-annealing process before each test and device was stored in dark, atmospheric environment with relative humidity (RH) ranging from 32% to 84% for next test. Test was conducted based on the following conditions:  $V_G$  was set to be 'Voltage linear sweep' mode with voltage ranging from +30 V to -30 V and  $V_D$  was set to be 'Voltage bias' mode with value of -2 V. Drain current ( $I_D$ ) was measured at each gate voltage ( $V_G$ ) for transfer ( $I_D|V_{GS}$ ) characterization.

### Extraction of device parameter

Contact resistance of device is extracted based on transmission line measurement (TLM) method and the mechanism is shown below:

$$R_{\text{Total}} = R_C + R_{\text{Channel}} = \frac{\partial V_D}{\partial I_D} \quad (1)$$

$$R_C = \text{Intercept}(R_{\text{Total}}, L) \quad (2)$$

Where  $R_{\text{Total}}$  represents total resistance in OTFT, equaling to the sum of channel resistance ( $R_{\text{Channel}}$ ) and contact resistance ( $R_C$ ),  $V_D$  and  $I_D$  are the voltage and current at the drain terminal, respectively,  $L$  is the channel length. Linear regime was chosen for conducting  $R_C$  extraction and  $V_D$  was set to be -2 V. Transfer characteristics ( $I_D|V_{GS}$ ) of devices with channel length ( $L$ ) ranging from 3.3 μm to 33.8 μm were measured when  $V_D$  is set to be -2 V. The extracted total resistance ( $R_{\text{Total}}$ ) is normalized by multiplying channel width ( $W = 1$  cm). The y-intercept ( $L = 0$  μm) of the curves represents the extrapolated normalized contact resistance ( $W \cdot R_C$ ), where channel resistance ( $R_{\text{Channel}}$ ) equals to zero.

Linear mobility is extracted based on transconductance ( $g_m$ ) according to the formula below:

$$\mu = \frac{L \cdot g_m}{WC_{\text{diel}} \cdot V_D} = \frac{L}{WC_{\text{diel}} \cdot V_D} \cdot \frac{\partial I_D}{\partial V_{GS}} \quad (3)$$

Where  $L$ ,  $W$ ,  $C_{\text{diel}}$ , and  $V_D$  represent channel length, channel width, unit area capacitance of dielectric layer and applied drain voltage, respectively.

### AM micro-LED driving

AM micro-LED panels were connected to the display driver system using a FPC interconnect and anisotropic conductive film (ACF), with bonding achieved after aligning and hot-bar bonding (Myachi bonder).

The display driver system was composed of a FPGA control system and 2 × 48-way driver boards to amplify voltages (up to +/24 V). It is controlled by Labview control software. The system can display images or video which are converted to greyscale from.avi files. Frame rate can be controlled up to 120 Hz and individual line times and gate pulse durations can be adjusted to optimize the display.

### Luminance test

2T-1C circuit test structure was designed for luminance test using Spectroscan Spectroradiometer PR670 system. The received light intensity was firstly calculated by multiplying aperture area with the measured luminance and then normalized by real pixel area for extracting the equivalent pixel luminance.

For high luminance test, luminance-current conversion efficiency was firstly measured with excellent linearity (-756 nits/μA) for panel with resolution of 254 PPI, as shown in Supplementary Fig. 14. Then driving current passing through the micro-LED was measured and multiplied by luminance-current conversion efficiency for luminance extrapolation.

### Film characterization

Scanning electron micrograph (SEM) was taken by exploiting ZEISS ULTRA PLASS system with electron energy of 5 kV.

The AFM measurement was done in tapping mode by exploiting a Bruker NanoMan, Dimension V atomic force microscope system.

### Device simulation

Device simulation is based on a commercial numerical device simulator ATLAS vended by SILVACO to verify the increased sub-gap density of state (DOS) and fixed charge carrier on device performance. Principle of device simulation is based on solving the Poisson's equation, the carrier continuity equations, and the drift-diffusion transport equations at each node of user-defined two-dimensional (2D) mesh. The channel length and the channel width are set to be 5 μm and 1000 μm, respectively. Fixed charge with concentration of  $-2 \times 10^{11}$  cm<sup>-2</sup> was introduced at buffer/OSC interface by using interface model. The total density of states (DOS) in the bandgap is modeled with two tail bands (donor-like and acceptor-like) using exponential distribution and two deep level bands (acceptor-like and donor-like) using Gaussian distribution. Donor-like deep states with Gaussian distribution is set as variable with different peak concentration (Higher DOS:  $C_{\text{peak}} = 2 \times 10^{17}$  cm<sup>-3</sup>eV<sup>-1</sup> Lower DOS:  $C_{\text{peak}} = 1 \times 10^{15}$  cm<sup>-3</sup>eV<sup>-1</sup>).

### Performance comparison

Apparent mobility to channel length ( $\mu/L$ ) is compared among literature-reported OTFTs with both solution-processed OSC and OGI layers. Device materials and key figure-of-merits are also summarized in Supplementary Table 1.

AM micro-LED display driven by TFT technologies is set as standard for comparison in Fig. 4f. The detailed information is included in Supplementary Table 2.

## Data availability

The 1) Electrical performance of the fabricated OTFT on top of micro-LED; 2) Uniformity and scalability of the fabricated OTFTs based on the post-OTFT via structure; 3) Display integration and demonstration data generated in this study are provided in the Supplementary Information/Source Data file. Source data are provided with this paper.

## References

- Huang, Y. et al. Mini-LED, micro-LED and OLED displays: present status and future perspectives. *Light Sci. Appl.* **9**, 105 (2020).
- Wu, T. et al. Mini-LED and Micro-LED: promising candidates for the next generation display technology. *Appl. Sci.* **8**, 1557 (2018).
- Lee, V. W., Twu, N. & Kymissis, I. Micro-LED technologies and applications. *Inf. Disp.* **32**, 16–23 (2016).
- Pust, P., Schmidt, P. & Schnick, W. A revolution in lighting. *Nat. Mater.* **14**, 454–458 (2015).
- Shin, J. et al. Vertical full-colour micro-LEDs via 2D materials-based layer transfer. *Nature* **614**, 81–87 (2023).
- Templier, F. GaN-based emissive microdisplays: a very promising technology for compact, ultra-high brightness display systems. *J. Soc. Inf. Disp.* **24**, 669–675 (2016).
- Xiong, J. et al. Augmented reality and virtual reality displays: emerging technologies and future perspectives. *Light Sci. Appl.* **10**, 216 (2021).
- Sheen, M. et al. Highly efficient blue ingan nanoscale light-emitting diodes. *Nature* **608**, 56–61 (2022).
- Lin, J. & Jiang, H. Development of MicroLED. *Appl. Phys. Lett.* **116**, 100502 (2020).
- Meng, W. et al. Three-dimensional monolithic micro-LED display driven by atomically thin transistor matrix. *Nat. Nanotechnol.* **16**, 1231–1236 (2021).
- Hwangbo, S. et al. Wafer-scale monolithic integration of full-colour micro-LED display using MoS<sub>2</sub> transistor. *Nat. Nanotechnol.* **17**, 500–506 (2022).
- Guo, X. et al. Current status and opportunities of organic thin-film transistor technologies. *IEEE Trans. Electron Devices* **64**, 1906–1921 (2017).
- Lin, Y. et al. Active-matrix micro-LED display driven by metal oxide TFTs using digital PWM method. *IEEE Trans. Electron Devices* **68**, 5656–5661 (2021).
- Um, J. et al. Active-matrix GaN  $\mu$ -LED display using oxide thin-film transistor backplane and flip chip LED bonding. *Adv. Electron. Mater.* **5**, 1800617 (2019).
- Tamaki, M. et al. LTPS TFT full color microLED display with redundant pixel design and covering micro-reflector array. *SID Symp. Dig. Tech. Pap.* **52**, 29–32 (2021).
- Nakamitsu, S. et al. High PPI micro LED display for small and medium size. *SID Symp. Dig. Tech. Pap.* **50**, 137–140 (2019).
- Tamaki, M. et al. A 3.9-inch LTPS TFT full color microLED display with novel driving and reflector cavity process. *SID Symp. Dig. Tech. Pap.* **51**, 111–114 (2020).
- Kim, J. et al. PWM pixel circuit with LTPS TFTs for micro-LED displays. *SID Symp. Dig. Tech. Pap.* **50**, 192–195 (2019).
- Sugiura, N. et al. 12.1-inch 169-ppi Full-Color Micro-LED Display Using LTPS-TFT Backplane. *SID Symp. Dig. Tech. Pap.* **50**, 450–453 (2019).
- Liu, Y. & Li, Y. Development of microLED display technology and applications. *SID Symp. Dig. Tech. Pap.* **53**, 654–657 (2022).
- Paranjpe, A., Montgomery, J. & Lee, S. Manufacturing solutions for micro-LED displays. *SID Symp. Dig. Tech. Pap.* **50**, 169–172 (2019).
- Chen, W. et al. Oxygen-dependent instability and annealing/passivation effects in amorphous In–Ga–Zn–O thin-film transistors. *IEEE Electron Device Lett.* **32**, 1552–1554 (2011).
- Fuh, C. et al. Effect of annealing on defect elimination for high mobility amorphous indium-Zinc-Tin-oxide thin-film transistor. *IEEE Electron Device Lett.* **35**, 1103–1105 (2014).
- Lee, S. et al. Improved reliability of low-temperature polysilicon TFT by post-annealing gate oxide. *IEEE Electron Dev. Lett.* **24**, 174–176 (2003).
- Wang, M. et al. High performance gigahertz flexible radio frequency transistors with extreme bending condition. *In 2019 IEEE International Electron Devices Meeting (IEDM)*. p. 8.2.1-8.2.4 (IEEE, 2019).
- Yao, R. et al. Low-temperature fabrication of sputtered High-*k* HfO<sub>2</sub> gate dielectric for flexible a-IGZO thin film transistors. *Appl. Phys. Lett.* **112**, 103503 (2018).
- Han, L. et al. Eliminating leakage current in thin-film transistor of solution-processed organic material stack for large-scale low-power integration. *Adv. Electron. Mater.* **8**, 2200014 (2022).
- Tull, B. et al. Micro-LED microdisplays by integration of III-V LEDs with silicon thin film transistors. *SID Symp. Dig. Tech. Pap.* **48**, 246–248 (2017).
- Klauk, H. Organic thin-film transistors. *Chem. Soc. Rev.* **39**, 2643–2666 (2010).
- Reese, C. et al. Organic thin film transistors. *Mater. Today* **7**, 20–27 (2004).
- Yang, J. et al. Active-matrix micro-light-emitting diode displays driven by monolithically integrated dual-gate oxide thin-film transistors. *J. Mater. Chem. C* **10**, 9699–9706 (2022).
- Duan, S. et al. Solution-processed centimeter-scale highly aligned organic crystalline arrays for high-performance organic field-effect transistors. *Adv. Mater.* **32**, 1908388 (2020).
- Duan, S. et al. Scalable fabrication of highly crystalline organic semiconductor thin film by channel-restricted screen printing toward the low-cost fabrication of high-performance transistor arrays. *Adv. Mater.* **31**, 1807975 (2019).
- Zhou, Z. et al. Inch-scale grain boundary free organic crystals developed by nucleation seed-controlled shearing method. *ACS Appl. Mater. Interfaces* **10**, 35395–35403 (2018).
- Zhang, Z. et al. Marangoni-effect-assisted bar-coating method for high-quality organic crystals with compressive and tensile strains. *Adv. Funct. Mater.* **27**, 1703443 (2017).
- Minemawari, H. et al. Inkjet printing of single-crystal films. *Nature* **475**, 364–367 (2011).
- Diao, Y. et al. Solution coating of large-area organic semiconductor thin films with aligned single-crystalline domains. *Nat. Mater.* **12**, 665–671 (2013).
- Xu, Y. et al. Contact thickness effects in bottom-contact coplanar organic field-effect transistors. *IEEE Electron Device Lett.* **34**, 535–537 (2013).
- Liu, C., Xu, Y. & Noh, Y. Contact engineering in organic field-effect transistors. *Mater. Today* **18**, 79–96 (2015).
- Han, L. et al. Reducing contact resistance in bottom contact organic field effect transistors for integrated electronics. *J. Phys. D* **53**, 014002 (2019).
- Hunter, S., Chen, J. & Anthopoulos, T. D. Microstructural control of charge transport in organic blend thin-film transistors. *Adv. Funct. Mater.* **24**, 5969–5976 (2014).
- Zhao, K. et al. Vertical phase separation in small molecule: polymer blend organic thin film transistors can be dynamically controlled. *Adv. Funct. Mater.* **26**, 1737–1746 (2016).
- Niazi, M. et al. Solution-printed organic semiconductor blends exhibiting transport properties on par with single crystals. *Nat. Commun.* **6**, 8598 (2015).
- de Boer, B. et al. Tuning of metal work functions with self-assembled monolayers. *Adv. Mater.* **17**, 621–625 (2005).
- Kitahara, G. et al. Meniscus-controlled printing of single-crystal interfaces showing extremely sharp switching transistor operation. *Sci. Adv.* **6**, eabc8847 (2020).
- Veres, J. et al. Low-*k* insulators as the choice of dielectrics in organic field-effect transistors. *Adv. Funct. Mater.* **13**, 199–204 (2003).



47. Lowman, I. et al. *Sputter Protective Layer for Organic Electronic Devices*. US2021/019157A1 (2021).
48. Yamamura, A. et al. High-speed organic single-crystal transistor responding to very high frequency band. *Adv. Funct. Mater.* **30**, 1909501 (2020).
49. Zschiechang, U. et al. Stencil lithography for organic thin-film transistors with a channel length of 300 nm. *Org. Electron.* **61**, 65–69 (2018).
50. Hoppner, M. et al. High-frequency operation of vertical organic field-effect transistors. *Adv. Sci.* **9**, 2201660 (2022).
51. Paterson, A. et al. Addition of the lewis acid  $Zn(C_6F_5)_2$  enables organic transistors with a maximum hole mobility in excess of  $20\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . *Adv. Mater.* **31**, 1900871 (2019).
52. Panidi, J. et al. Remarkable enhancement of the hole mobility in several organic small-molecules, polymers, and small-molecule-polymer blend transistors by simple admixing of the lewis acid P-Dopant  $B(C_6F_5)_3$ . *Adv. Sci.* **5**, 1700290 (2018).
53. Feng, L. et al. All-solution-processed low-voltage organic thin-film transistor inverter on plastic substrate. *IEEE Trans. Electron Devices* **61**, 1175–1180 (2014).
54. Tang, W. et al. Highly efficient all-solution-processed low-voltage organic transistor with a micrometer-thick low-K polymer gate dielectric layer. *Adv. Electron. Mater.* **2**, 1500454 (2016).
55. Fukuda, K. et al. Fully Solution-processed Flexible Organic Thin Film Transistor Arrays With High Mobility And Exceptional Uniformity. *Sci. Rep.* **4**, 3947 (2014).
56. Bai, J. et al. Bar-coated organic thin-film transistors with reliable electron mobility approaching  $10\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ . *Adv. Electron. Mater.* **6**, 1901002 (2020).
57. Venkateshvaran, D. et al. Approaching disorder-free transport in high-mobility conjugated polymers. *Nature* **515**, 384–388 (2014).
58. Li, J., Sun, Z. & Yan, F. Solution processable low-voltage organic thin film transistors with high-k relaxor ferroelectric polymer as gate insulator. *Adv. Mater.* **24**, 88–93 (2012).
59. Yuan, Y. et al. Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method. *Nat. Commun.* **5**, 3005 (2014).
60. Lee, S. et al. 9.4-Inch 228 PPI flexible micro-LED Display. *J. Soc. Inf. Disp.* **29**, 360–369 (2021).
61. Jung, H. et al. Active matrix micro-LED stretchable display and technical challenges. *SID Symp. Dig. Tech. Pap.* **53**, 517–520 (2022).
62. Kim, H. et al. High brightness active matrix micro-LEDs with LTPS TFT backplane. *SID Symp. Dig. Tech. Pap.* **49**, 880–883 (2018).

## Acknowledgements

We are grateful to Enkris Semiconductor, Inc. for providing epitaxial wafers, Xiangneng Hualei Optoelectronic Corporation for providing LED manufacturing process. We are grateful for the financial support from Shanghai Municipal Commission of Science and Technology

Foundation under Grant No. 21511101304 (X.G.) and National Science Fund for Excellent Young Scholars under Grant No. 61922057 (X.G.).

## Author contributions

X.G. conceived of the idea and supervised the work. S.O. and X.G. designed the overall experiments. L.H., D.S., A.B., and A.C. carried out experiments and collected related data. L.H., S.O., and X.G. analyzed all the data and co-wrote the paper. K.C. fabricated the micro-LED wafers. X.Y. and J.L. assisted in checking the pixel design. F.C. designed the structure of OLI integration array. All authors discussed the results and commented on the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

**Supplementary information** The online version contains supplementary material available at <https://doi.org/10.1038/s41467-023-42443-8>.

**Correspondence** and requests for materials should be addressed to Xiaojun Guo.

**Peer review information** *Nature Communications* thanks Hocheon Yoo and the other, anonymous, reviewer(s) for their contribution to the peer review of this work. A peer review file is available.

**Reprints and permissions information** is available at <http://www.nature.com/reprints>

**Publisher's note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

**Open Access** This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

© The Author(s) 2023