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Perspective

# Hybrid chips to enable a sustainable internet of things technology: opportunities and challenges

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**Abstract**
A new technological approach is needed for the development of emerging electronic components and systems within the Internet of Things (IoT) era. New advancements and innovations are required in architectural design and hybrid systems heterogeneous integration to address the challenge of widespread IoT deployment, its power demands and sustainability. Hybrid chips are one of the emerging technologies that can help overcome the current limitations in terms of energy consumption, performance and sustainability that could shape the future of electronic systems for targeted applications. Hybrid chips combine different materials and manufacturing technologies on the same substrate or package using advanced flexible heterogeneous integration techniques, with the focus of merging the advantages of each unit or technology toward enhanced performance and new levels of emerging functionalities. The categorization of hybrid chips spans across rigid hybrid chips that follow a multi-chiplet approach, semi-flexible chips that integrate flexible units with semi-rigid ones such as thinned silicon integrated circuits, and lastly, flexible chips in which all components are inherently flexible. This perspective article analyzes technical challenges that arise concerning the development of sustainable materials and processing technologies, complex heterogeneous integration, as well as advanced packaging architectures, standardization, and reliability testing. The economic implications for the semiconductor technology transition to hybrid chips is presented in terms of manufacturing costs, economic feasibility, and market readiness. Key insights and future application opportunities are provided, while recent advancements in the field are summarized. This perspective article suggests that by addressing these challenges, hybrid chips have the potential to transform electronic components and systems across a wide range of industries and use case scenario. The advancement of hybrid chip technologies by enhancing the collaboration between industry and academia as well as policymakers will be a crucial part in the realization of required sustainability goals within the worldwide Chips Act initiative, while ensuring the technological progress has the right balance between improved performance and sustainability.

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## 1 Hybrid chips as a paradigm shift toward sustainable electronics

New materials, advanced manufacturing, and research and development (R&D) on semiconductors have propelled world's economic growth enhancing citizens prosperity and comfort. Semiconductor chips, electronic components and systems are at the center of this technological innovation. R&D in semiconductor technologies has supported the abrupt development of human civilization reported the last 60 years. Semiconductors have become so ubiquitous in technological innovations that they are mistakenly considered by most people as a commodity. The COVID-19 pandemic and chip supply problems have focused attention on this key technology, whose market is expected to exceed $1 trillion USD by 2030. Only in 2021, the semiconductor industry delivered a record 1.15 trillion chips, with global revenues exceeding $500 billion, and dozens of new chip designs entering the market. However, continuous innovation in design and production is essential to keep semiconductor goods competitive, making this one of the most research-intensive sectors. It is estimated that 20% of revenue in the semiconductor value chain is spent on R&D. Many more innovations will be driving the digital transformation in the next decade.

However, conventional silicon chips are lacking in one area: sustainability. The high manufacturing temperatures and costs associated to silicon chips fabrication and the creation of electronic wastes (e-wastes) due to their limited recyclability, is not just a drawback for business but also harmful for the environment. While the semiconductor supply chain is working to achieve net-zero carbon emissions, the sector is still a long way from meeting the emissions targets outlined in the United Nations' 2016 Paris Agreement. A co-optimization strategy should be pursued in order to enhance performance, safety and security while minimizing resources consumption, costs, and environmental impact. This approach should handle associated environmental issues such as greenhouse gas emissions, human and environmental toxicity [1], while concepts such as the use of sustainable materials and fabrication processes, and assuring minimal environmental footprint throughout the device life cycle should be prioritized.

Customers nowadays demand intelligence in every object connected within the Internet of Things (IoT) network, however this requires IoT edge data processing that urges for better and more energy efficient hardware performance. To handle the data deluge in IoT, new technologies such as artificial intelligence (AI) and machine learning (ML) are required for resource-efficient deployment of smart, sustainable IoT systems. The majority of IoT devices are based on conventional silicon chips that integrate sensors, actuators and communication modules, microcontrollers, power management and data processing units. These chips are fabricated using inorganic materials processed on silicon substrates, which makes recycling challenging thus these chips are potentially harmful for the environment if not retrieved. Since conventional scaling of CMOS technology is no longer viable, industry must now innovate across all elements of system design for IoT devices to keep Moore's law at pace within a sustainable way. New advancements and innovations are required on materials, processes, chips' architectural design and hybrid systems heterogeneous integration to address the challenges of sustainable IoT widespread deployment [2].

Hybrid chips are one of the emerging technologies that can help to overcome the current limitations in terms of energy consumption, sustainability, and performance that could shape the future of electronic systems for targeted applications (Fig. 1). Hybrid chips combine different materials and manufacturing technologies on the same substrate or package through advanced flexible, heterogeneous integration techniques with the focus of merging the advantages of each unit or technology toward enhanced performance and new levels of emerging functionalities. The categorization of the field of hybrid chips spans across (a) rigid hybrid chips that follow a multi-chiplet approach, (b) semi-flexible hybrid chips that integrate flexible units (evaporated or printed on flexible substrates) with semi-rigid ones such as thinned silicon integrated circuits (ICs), and lastly (c) flexible hybrid chips in which all components are inherently flexible. Figure 1 illustrates the overall structure of the perspective manuscript and depicts how the different topics are inter-related. Specifically, Fig. 1 depicts an overview of hybrid chips categories indicating the main features of each technology addressing sustainability (Sect. 2), and integration/packaging technologies (Sect. 3). The manuscript also addresses the opportunities (Sect. 4) and challenges (Sect. 5) that should be addressed by each technology. Key recent advancements of hybrid chips (Sect. 6) are also presented toward market applications. It is noted that semi-flexible (category b) and flexible (category c) hybrid circuits could adopt a multi-chiplet architecture incorporating therefore technological inputs of category a (Figs. 1 and 2).

Regarding category (a) of hybrid chips, recent advances have been reported such as "multi-die" or "multi-chiplets" design approach toward "System-on-a-Chip" (SoC) integration and recently "System-in-a-Package" (SiP) approach. [3] The SiP approach offers significant flexibility, as chiplets can be mixed and matched depending on the application, leading to a scalable and customizable solution. Reduced system-level costs are offered by a multi-chiplet approach

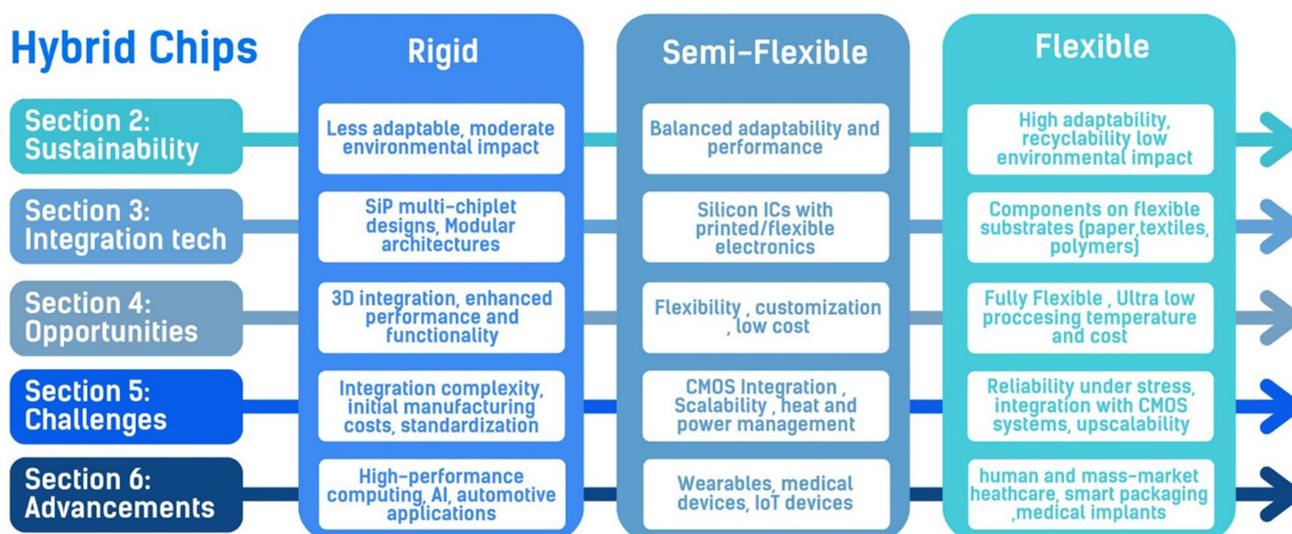


**Fig. 1** Illustration of the overall structure of this perspective article. The core differences between rigid, semi-flexible and flexible hybrid chips are presented addressing key technological pillars, namely sustainability aspects (Sect. 2) and integration/packaging issues (Sect. 3), while opportunities (Sect. 4) and challenges (Sect. 5) are compared focusing on market exploitation (Sect. 6)

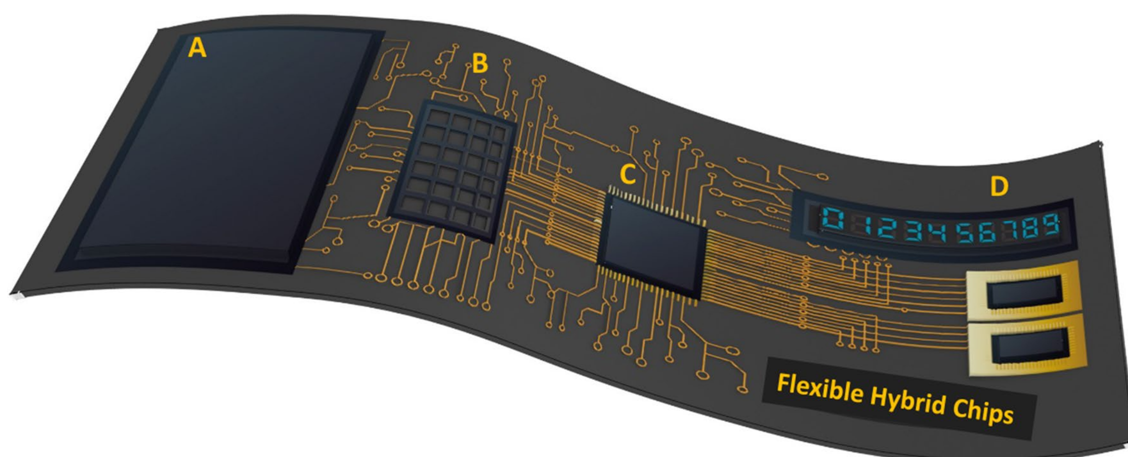


**Fig. 2** A schematic of a sophisticated flexible or semi-flexible package constituting a system of various SiPs. Part A: Targeting self-powered (autonomous) wireless devices, various types of 'ambient' energy supply from energy harvesting sources (solar, mechanical, RF, water, etc.) and associated energy storage units (supercapacitors, batteries) should be integrated, while developing micro-power management solutions for miniaturized systems operation. Part B: Multi-chiplet integration is the solution to the yield issues in larger chips, while facilitates splitting the design and implementing sub-systems into separate smaller dies with enhanced customization and lowered costs. Part C: Peripheral circuits to handle data processing enabled by either thinned Si IC including amplifiers, filters analog to digital converters or flexible units. Part D: Printed displays, antennas and sensors contribute to IoT devices communication. Interconnections between the various SiP and chips are realized by printing, vacuum techniques, laser technologies and flexible integration technologies

as a result of enhancing silicon yields while minimizing waste during chip manufacturing. Specifically, by using chiplets, reduced costs can be also achieved by producing high volumes of standardized chiplets and then combining them in various configurations, while an enhanced performance and extended functionality can be also enabled by this customization potential. There are at least two chiplet designs, namely chip partition and integration (driven by cost and technology optimization) and chip split and integration (driven by cost and yield) [3]. To make multi-chiplet designs viable, significant progress has been made in interconnect technologies, including development of inter-chiplet communication protocols, high-bandwidth interconnects, and efficient packaging techniques.

Heterogeneous integration is a critical step toward SiP implementation paving the way for high-performance chips that combine complementary components with distinct functions (such as data processing and I/O). This approach

can be expanded also to systems that include units manufactured using different manufacturing processes including printed electronics and silicon technology [i.e., hybrid chips category (b)], or even systems developed initially on different substrates and heterogeneously integrated onto the same package. The heterogeneous integration approach can be extended to the board level, allowing many SiPs to be integrated on the same printed circuit board (PCB) in 2D, 2.5D, or 3D dimensions [2, 4]. Specifically, 2.5D packaging has become popular, in which chips are placed side-by-side on an interposer. This allows for high-density interconnects between chips avoiding complexities of 3D stacking. To this end, new materials like graphene, carbon nanotubes, and advanced polymers in packaging are required to improve electrical performance and heat dissipation in hybrid chips [5].

Hybrid chips that combine flexible electronics and silicon ICs, thus category (b) of hybrid circuits, are termed as semi-flexible hybrid chips (Fig. 2). These electronics have gained attention recently towards applications that require chips with large-area form factors, high-speed connectivity, low data latency, enhanced functionality, conformability, and low-cost fabrication. This is a very powerful and adaptable technology compatible with a wide range of applications in IoT technology [6–9]. Specifically, printed units provide the flexibility and scalability necessary for sensing and actuating, whereas semi-rigid silicon ICs are employed for implementing complex functions such as intense data processing and communication. Thinned Si IC can be mounted on flexible substrates using conventional manufacturing and assembly procedures such as pick-and-place technique, or even be integrated utilizing direct transfer printing [9]. It is expected that this novel hybrid chips approach will redefine how products are conceptualized, built, and manufactured overcoming technological challenges opening the path for new market opportunities across the whole value chain of the semiconductor ecosystem.

The third type of hybrid chips, namely category (c), addresses flexible hybrid chips in which all components are inherently flexible, being either printed or evaporated (Figs. 1 and 2). The best examples of this type of hybrid chips have been demonstrated by Pragmati IC company in collaboration with ARM industry. The team used Pragmatic's innovative commercial manufacturing approach, known as 'fab-in-a-box', along with its associated FlexLogIC foundry services. This approach has the potential for the development of flexible processing engines addressing IoT edge computing that do not rely on semi-rigid silicon-based components [10]. Such flexible hybrid chips could overcome key hurdles on developing energy efficient IoT devices with reduced cost while increasing sustainability since they rely on manufacturing at low temperatures with minimum wastes of resources [11, 12].

In this perspective, we firstly address in Sect. 2 the need to provide power for billions of IoT devices operation and address the energy demands for this big data processing. Moreover, we argue that the high temperature manufacturing of conventional silicon-based chips together with their limited recyclability and reconfigurability results in e-wastes, which have significant negative environmental impact. A technological transition from single SoC towards hybrid multi-chiplet based architectures is required to overcome the aforementioned issues (Sect. 3.1) implementing a heterogeneous integration and novel packaging of different SiP sub-systems (Sect. 3.2). Future opportunities and required steps towards enhancing the functionality and performance offered by hybrid chips are given toward novel applications including wearables and edge computing (Sect. 4). Challenges that should be addressed are discussed (Sect. 5) suggesting ways to overcome technical difficulties on materials and processes development level, heterogeneous integration, standardization, and reliability testing, in line with sustainability and circular economy plans. Emphasis is given to the economic implications for the required technology transition to hybrid chips discussing manufacturing costs, economic feasibility and market readiness (Sect. 5.4). Recent literature advancements are analyzed covering rigid hybrid chips enabled by heterogeneous integration and packaging technologies, demonstrations based on semi-flexible hybrid chips and finally recent highlights on novel flexible hybrid chips including commercial products (Sect. 6). The innovation potential and the market perspective of hybrid chips is described in Sect 7, pointing out that there is a need for developing European research infrastructures offering both rigid and flexible manufacturing facilities in a single place, while special focus should be given on hybrid integration and packaging technologies of hybrid chips (either rigid or flexible).

## 2 Addressing the manufacturing environmental impact and the power demands of internet of things technology

The world is facing multiple challenges related to climate change, as a result of the extended use of electronic gadgets and growing dependence on non-recyclable critical raw materials (CRM). The ever-increasing consumer demand for electronic devices is contributing to the world's fastest-growing waste stream, known as e-waste [13]. The ever-shortening lifespan of smart devices has created a "tsunami of e-waste," as the UN has characterized it, with 53.6 million tons

accumulated each year, only 20% of which undergo formal e-recycling [14]. The global e-waste monitoring for 2020 shows that we are producing e-waste in the range of 7.3 kg per capita, which is expected to double every 5 years if no measures are taken. This should be reversed by adopting a "green technology" mindset, driving our prosperity for sustainability without sacrificing our digital growth. In addition to developing strategies to manage such e-waste, further challenges should be identified concerning the capability of manufacturing electronics within a holistic eco-design strategy [15]. The focus should be on low power consumption during product manufacturing and operation, while significantly lowering material usage compared to conventional processes. A sustainable approach should be adopted using components and processes based on abundant, recyclable materials with a much smaller environmental footprint towards a circular economy, as for example suggested within "Green Deal for Europe" initiative [16], positively impacting environmental decarbonization.

A novel technology of «responsible electronics» is required considering the Safe and Sustainable by Design (SSbD) framework and eco-design principles, towards producing systems able to be reused, recovered, and recycled thus going beyond silicon chips. This approach should be based on energy efficient manufacturing processes, requiring less CRM than conventional techniques to achieve the required circularity. These «responsible electronics» can be integrated into IoT applications requiring shorter device's lifespan and long-term usefulness,[17]while they should contain sustainable components with increased versatility to allow lower production cost and almost zero environmental impact. The world dependency on CRM, the high energy demand of semiconductor processing and the predicted massive e-waste force communities to set a new paradigm in the design of electronic products. Holistic approaches such as the SSbD and eco-design for sustainable products are instrumental to overcome these challenges. The combination of these strategies should thoroughly focus on safety (intrinsic hazard, occupational, environmental and consumer's safety) and sustainability aspects across the full product's life cycle stages such as raw materials acquisition, manufacturing, usage, and fate. Overall, sustainability plan for IoT applications should enhance the product's design to maximize safety, minimize the use of resources and energy consumption, reduce carbon footprint and waste, increase durability and recyclability while keeping performance high.

The purpose of the IoT is to support and create an intelligent environment by incorporating a distributed network of wireless sensors connected to the cloud, and humans as well, while providing decision-making functions to these objects. As data volume of IoT systems expands exponentially [18], the need to address power consumption during operation and big data processing becomes a severe issue urging for development of novel systems with high flexibility, efficiency and speed to enable a long-term viability of such systems. Technologies implementing autonomous smart devices into an IoT network will lead to 79.4 zettabytes of data in 2025.[19]IoT edge devices[18]are usually not capable of data processing and rely on energy-consuming and high-latency cloud communication. Furthermore, the inherent bottlenecks of Si-based CMOS processors due to their energy inefficient von Neumann's computation architecture [20], lead thus to unsustainable energy cost [21]. Most Si-based IoT devices depend on a battery as their power source, therefore, fail to meet the design goals of lifetime power supply, low-cost, and reliable sensing, demanding radically new device and computing principles. The parallel energy harvesting and edge computing features [22] in the same chip would enable battery-less IoT edge devices with decentralized data processing implemented directly on the edge device leading to a positive environmental, societal, and economic impact. Hence, the deployment of IoT technology will rely on a sustainable, low-cost chip manufacturing while developing self-powered systems.

The development of new innovative technologies based on IoT devices require therefore the cooperation of many complementary disciplines and research fields (Fig. 3). Novel IoT chips should demonstrate efficient on-chip data processing and multiple sensing functions, promising thus the implementation of IoT-edge devices with ultra-low power consumption. Hybrid chips are a potential candidate to drive this sustainable development offering several opportunities for expanding the available chips functionalities across a plethora of applications. Hybrid chips integrate dissimilar materials and technologies that would otherwise be difficult to be interconnected without developing specific heterogeneous integration approaches. 3D deployment and integration methods for the chip [23], module, and system level can contribute significantly to lowering further the manufacturing costs of components and systems. This emerging path leads to more versatile and efficient systems due to the ability to combine multiple manufacturing processes on a common sustainable substrate providing a clear route for low manufacturing costs and reduced $CO_2$ emissions during device manufacturing and operation phase. Another advantage is their potential for up-scalable fabrication using manufacturing techniques such as additive manufacturing technologies (mainly semi-flexible and flexible hybrid chips). This technology transition would make a huge impact, particularly in reshaping the infrastructure and data transmission of the telecommunications sector and especially at radio-frequency (RF) front-ends, where millimeter-wave frequencies are crucial for the next generation of telecommunications beyond 5G [24].

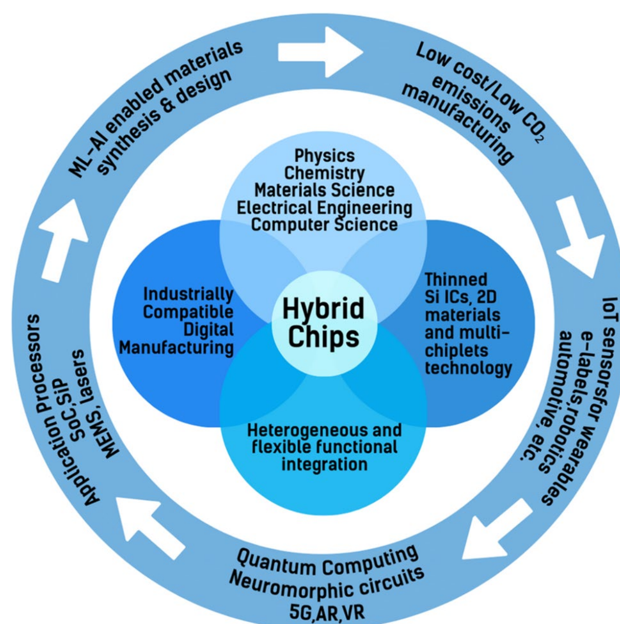


**Fig. 3** Multi/interdisciplinary breakthroughs are needed for hybrid chips deployment. Research and industry collaboration should be established covering physics, chemistry, materials science, electrical engineering, advanced manufacturing technologies, and high-performance modeling to develop cutting-edge rigid, semi-flexible or flexible hybrid chips, for multiple applications

Printing technologies cut costs dramatically and reduce the maximum processing temperature with a huge positive impact on sustainability. Flexible electronics, an important unit of sustainable hybrid chips, are highly relevant for the challenges of the future as is evident by their huge market's potential: IDTechEx predicted that the total market for flexible electronics, which was > 23Bn Euros in 2016, will grow and reach ~ 62Bn Euros in 10 years [25]. The number of possibilities offered by flexible or printed electronics technology is huge addressing various market domains. A novel holistic approach is therefore needed for hybrid chips to achieve the required sustainability, focusing on novel materials [26], advanced manufacturing and packaging enabling hybrid chips functional integration, and developing novel systems architecture.

## 3 Hybrid chips: architecture, integration and packaging

### 3.1 Paradigm transition from a system-on-a-chip to a system-in-a-package architecture

The SoC approach was one of the first examples of hybrid chips that combines multiple ICs in a single application processor chip, each one having different functionalities, such as a central processing unit (CPU), a graphics processing unit (GPU), and memory. This architecture has played a crucial role enabling more efficient and complicated functions toward improved data processing and memory units. Unfortunately, scaling down further SoC features is becoming increasingly complex and expensive. An industrial shift toward multi-chiplet design could be part of the solution to these challenges [27]. Multi-chiplet system designs can facilitate large-scale deployment of AI/ML, and enhance silicon yields, while decreasing material wastes during chip production. In a standard SoC, one chiplet performs computation-intensive tasks, while the other implements the I/O interface and a third one executes memory functions. This is especially significant for the automotive sector in terms of power management in autonomous driving. The Kraken SoC, for example, merges numerous acceleration engines and a set of peripherals from various types of sensors into a SiP. Using a heterogeneous architecture to handle difficult visual tasks, Kraken was shown to enable useful applications for unmanned aerial vehicles (UAVs) [28].

Nowadays, multi-chiplet SiP designs are replacing SoC approach [27]. Chiplet technology has become a popular technique that combines additional functions and capabilities enabling the improvement of system-level performance and power economy. As a solution to yield concerns in larger chips, chiplet integration permits separating the design and implementing sub-systems into separate smaller dies (like processors, memory, RF modules). A large-scale application-specific integrated circuit (ASIC) can be divided into several dies that are connected through chiplet integration forming a heterogeneous SoC. To facilitate efficient communication between the various chiplets, many dies prepared from different processing technologies can be combined utilizing dense parallel package interconnects. Recent advancements

have seen the incorporation of even more diverse components, including analog, digital, and even optical components, leading to highly versatile chip solutions. SiP designs include advanced connectivity features, integrating components like 5G modems and Wi-Fi chips, vital for the IoT and smart device markets.

It has been shown that the SiP approach enables customization, high degrees of flexibility, and low costs when compared to alternative packaging options. The SiP architecture as a novel, advanced integration and packaging technology allows better performance in terms of density, power, and scaling down [29]. Within multi-die architecture, there are three different levels of integration. Figure 4 depicts that the smaller integration level is that of SoC. Multiple SoC can be coupled together toward more complex functions constituting the SiP integration level. Lastly, multiple SiP units can be integrated on the same PCB. Despite the numerous benefits of chiplets, multi-die systems have yet to gain general adoption—there are still advancements to be implemented. Integration technologies, power restrictions, and dedicated testing provide specific issues. The physical size of components, connectivity, layer transitions, and package size all restrict the ability to increase the bandwidth of the interface between chiplets. The 3D stacking capabilities of chiplets, on the other hand, may lead to a system with high-bandwidth interconnects between the chips while preserving a relatively small form factor and offering a solution to the heat dissipation issue when chips are packed together. Another barrier to multi-die systems further deployment is the lack of industrial standards. To this end, the Universal Chiplet Interconnect Express (UCIe) [30], which was launched in 2022, is a major component in enabling chiplet further innovation. More details on potential barriers for hybrid chips technology deployment can be found in Sect. 5.

### 3.2 Heterogeneous integration and packaging technologies in rigid hybrid chips

Next-generation computing architectures require the ability to monolithically incorporate specialized accelerators to meet the demands of various applications [4]. A prerequisite for this is to develop monolithic interconnects that provide ultra-high bandwidth at very low power and extended capacity. 3D integration involves stacking multiple semiconductor layers or dies on top of each other. By stacking chips, data can travel shorter distances, reducing latency and improving overall chip performance. This is particularly beneficial for applications like high-performance computing and AI. Key metrics to monitor system's operation are performance per Watt and performance per unit cost. Equally important is also how the system responds to thermal and power integrity issues associated with Moore's law and the ever-increasing integration density. Heterogeneous integration in standard rigid SiP hybrid chips is implemented using current generation 3D designs such as silicon interposers and omni-directional interconnect (ODI), while hybrid bonding and flip chip method provide powerful tools to address several of the above difficulties [31]. The flip chip is an improvement over wire bonding in terms of signal integrity, power integrity, flexibility, and downsizing. However, in the majority of the available heterogeneous integration approaches, materials and processes that are vastly different compared to standard packaging and silicon procedures are

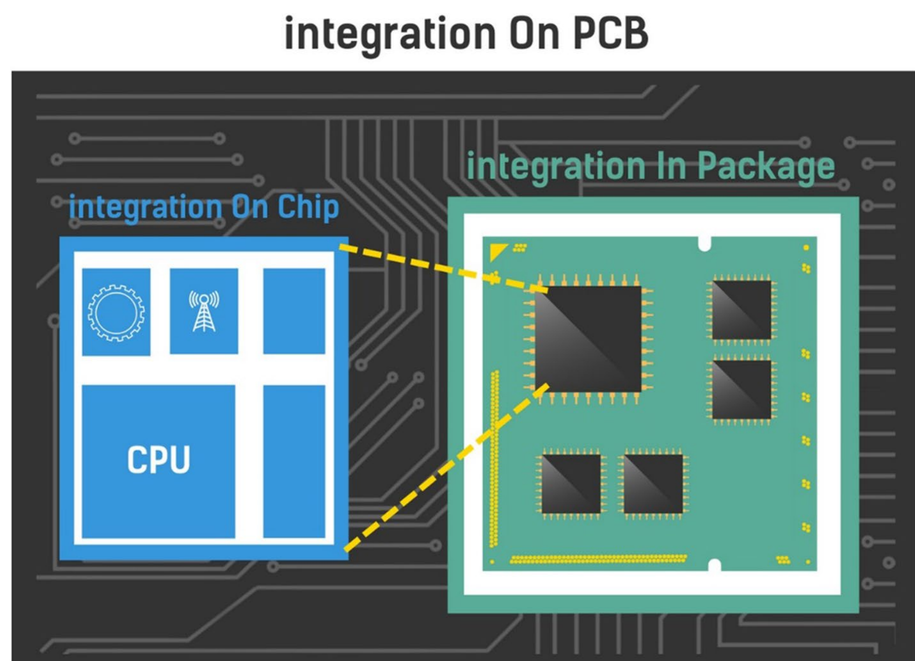


**Fig. 4** Different heterogeneous integration levels implemented in modern hybrid chips. The lowest integration level addresses the SoC approach, while a higher level is related to SiP implementation through multiple SoC integration. In complex hybrid chips, a third level of multiple SiP integration is implemented on PCB level

used, placing considerable constraints on the types and densities of integration that can be attained. Recent progress in techniques like Through-Silicon Vias (TSVs) and wafer bonding has improved the feasibility and reliability of heterogeneously integrated stacks.

Sophisticated packaging methods are used for SiPs such as fan-out wafer-level package (FOWLP), chip-on-wafer-on-substrate (CoWoS), Embedded Wafer-Level Ball Grid Array (eWLB) [32], Embedded Multi-Chip Interconnect Bridge (EMIB) [33] and others [2]. FOWLP provide a very high overall system density, which overcomes the issue of insufficient implant balls created by too many chip pins in typical wafer-level packages. The eWLB has evolved from FOWLP, and this style of packaging not only increases interconnects density but also decreases package size offering a significant amount of board space. Integrated 2.5D and 3D eWLB solutions are available compatible with improved heat dissipation and processing performance for 5G and AI applications. Finally, Intel has invested much R&D in EMIB packaging approach that is based on an organic-board-type package with outstanding electrical properties, offering enhanced shielding structure, as well as minimal crosstalk and losses.

### 3.3 Novel heterogeneous integration approaches in semi-flexible hybrid chips

Thinned silicon ICs are an essential component of semi-flexible hybrid chips. In a usual assembly process of semi-flexible hybrid chips, printed devices and circuits are firstly manufactured, while semi-rigid silicon components are fabricated in a later step. Thinned silicon ICs are particularly appealing for hybrid chips development on flexible substrates because they can be twisted or stretched up to a specific mechanical strain limit. To this end, a great amount of effort has been paid on developing ultrathin silicon ICs with thickness down to few µm that can be bent to a radius of curvature of 5 mm [34]. Various materials and methods have been used in recent years to transfer and mount Si ICs and flexible electronic components together onto flexible substrates [35] and stretchable substrates [36]. As a typical technique for connecting the circuits together, ultrathin ICs are embedded in a film toward a full system fabrication-in-a-foil approach [37]. Specifically, to connect Si ICs with printed sensors and circuits, an interposer is required that transmits the signal to a pitch spacing (> 100 µm); a processing compatible with printing technologies [8].

Semi-flexible hybrid chips also require passive components such as resistors, capacitors, and inductors in addition to silicon ICs. These surface mounted devices (SMDs) are commonly incorporated into flexible hybrid chips to provide circuit functionality. Silicon ICs and SMD passive components are connected using soldering or dispensing Isotropic conductive adhesives (ICAs) between the chip and the substrate. To align various chips, a flip-chip pick-and-place tool can be utilized. In a typical process, the substrate is first drilled to create the via holes that connect top circuitry to the bottom circuitry. Chip pad alignment to printed traces must be precise—alignment accuracies of tens of µm are needed for bonding tools [8]. NextFlex's first-generation printed Arduino is a product fabricated using this process flow [8].

The printed units of semi-flexible hybrid chips can be fabricated by using various large-scale manufacturing technologies such as transfer printing (TP), contact printing (CP), in-tandem contact-transfer printing, and other advanced printing processes. These industrially compatible techniques can enable the accurate integration of devices of various dimensions onto planar or 3D layouts [36, 38]. These printing processes offer a low-cost approach to implement heterogeneous integration of microchips with other functional components, allowing to obtain high transfer yields of nano [9] or micro [39] chip size structures. For example, TP has been investigated for high transfer yield pick and place of microchips (100 µm) onto flexible substrates. [40] Although the pick-and-place method using elastomeric stamps works well for printing large microchips, it is difficult to be used for ultrasmall chips with size ≤ 100 µm and/or nanoscale materials with high transfer yield. This is because at these dimensions, adhesion forces such as electrostatic and Van Der Waals on the chip surface may prevail over gravity forces, introducing complications [31]. Furthermore, due to their ultra small size, thinned chips are more prone to fail during transfer than thicker chips [36]. These issues might be overcome by using the "direct roll transfer printing" technology, which has been proven to integrate laterally aligned nanoscale and microscale components with a 95% transfer yield [39]. However, the range of functional materials that may be printed using this method is restricted by the available wafers. Alternative nanostructure assembly methods, like CP [36], which use bottom-up grown nanomaterials to produce nanoscale electrical layers on diverse substrates, might circumvent such restrictions (Fig. 5).

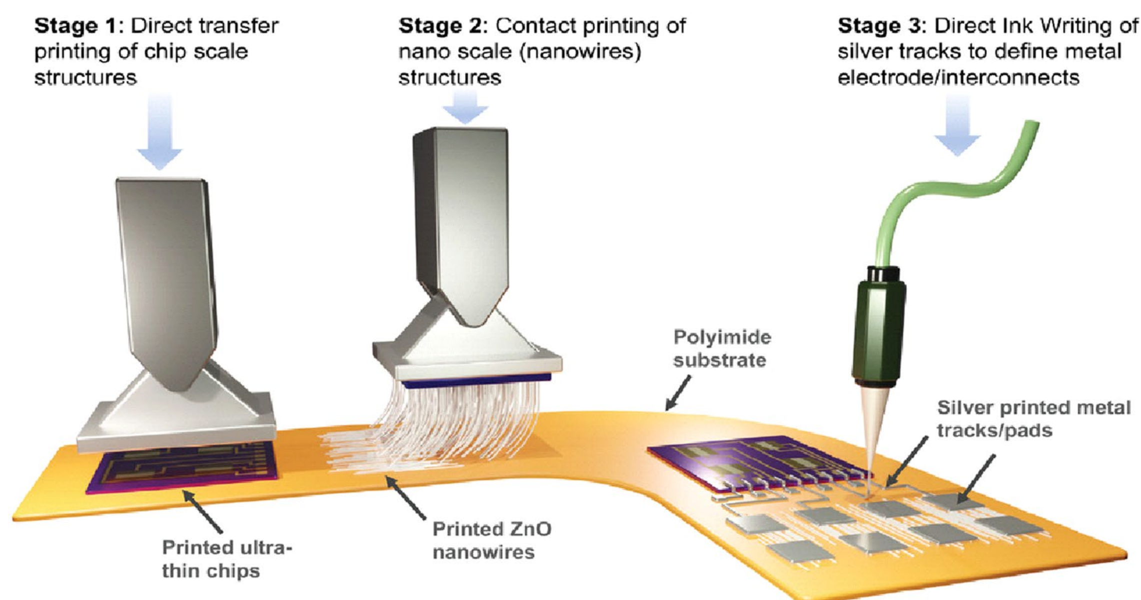


**Fig. 5** A novel manufacturing approach for semi-flexible hybrid chips combining thinned Si ICs with printed units and interconnections on flexible substrate [28]. Stage 1: direct transfer printing of the ultrathin chips; Stage 2: contact printing of nanoscale electronic layers; and Stage 3: direct ink writing of the miniaturized metal tracks defining the device electrodes and interconnects. Copy rights belong to reference [28] that is an open access article distributed under the terms of the Creative Commons CC BY license

## 4 Opportunities

### 4.1 Hybrid chips for healthcare and wellbeing applications

With the development of ML and AI, new chips may now be created to support technologies such as wearable IoT incorporating neural networks and deep learning processes [41]. Wearable devices [42] and human–machine interfaces (HMI) are important components of IoT technological transformation, with applications in digital healthcare, automotive sector, autonomous robots [43], virtual reality (VR), and augmented reality (AR). The quality of the interactive experience with the real and virtual worlds is determined by the natural two-way interfaces allowed by wearables and HMI, as well as the real-time touch-based information they supply and receive. Digital healthcare requires wearable devices that can perform data processing through brain-computer [44]. Haptic technology advances [45, 46] coupled to these technologies are also expected to enhance the overall safety and users comfort in various fields.

Many essential IoT device challenges, including energy efficiency, flexibility [47], and processing speed, may be addressed by hybrid chip solutions, resulting in devices with longer lifespan and a better user experience. Hybrid chips combined with an AI-enabled materials synthesis and design methodology can even aid humans in overcoming difficulties that were previously unsolvable, i.e., enable the development of flexible, biocompatible wearable devices [48]. This can be achieved using material innovation enabled by hybrid organic and inorganic semiconductors opening the path for wearable devices [49] application in various domains and facilitating many different end-user needs. This includes healthcare applications such as brain-computer interfaces for self-management and screening, diagnostics, and treating neurological and mental disorders [50]. This kind of e-neuropatches and stimulation devices can improve the overall patient experience and bring solutions to them that were unattainable with conventional chips technology. A notable example of integrating haptic technology [50] into a wearable device is the potential to aid individuals with sensory impairments such as deafblind, improving their communication and accessibility capabilities and enhancing their quality of life. This haptic technology [51] can also be implemented in the automotive sector to simulate complex manufacturing processes and create touchable and interactive surfaces in vehicle interiors [52, 52] to improve the overall safety and comfort of the passengers. Furthermore, flexible hybrid chips could enable two-way tactile [53] communication for users in AR/VR applications. This would provide a more immersive and interactive experience for the end users within the tactile internet concept as in the case of the metaverse [54].

Hybrid chips can also offer remarkable advantages in the photonics packaging field [55] by improving the integration and functionality, which can lead to contributions in a plethora of applications such as data communications, sensors, and imaging.

By bringing together scientists from many disciplines, while merging multiple manufacturing techniques within a SiP approach, considerable advancement in wearables [18, 56] and IoT technologies is envisaged enabled by hybrid chips adaptability and enhanced functionality.

### 4.2 Hybrid chips for adaptive edge computing and robotics

Adaptive edge computing can greatly benefit from hybrid chips by enabling systems with significantly lower energy consumption and enhanced data processing energy efficiency. By leveraging hybrid chips' adaptive edge capabilities [57], IoT devices can also perform [58] data processing locally without relying on cloud communication. This architecture therefore effectively reduces the power and time needs improving the latency of such devices as well as security since all the data analysis will be done locally. This ensures that the IoT [59] systems remain functional even under challenging conditions. These emerging capabilities will also assist the sustainable growth of IoT [60] networks that are expected to reach soon billions of interconnected devices.

The compatibility of memristive technology with the CMOS process, makes the use of hybrid chips highly relevant in the context of energy-efficient, neuromorphic edge computing devices [58, 61]. This allows for unconventional circuit design and adaptation in ML algorithms taking advantage of the memristive device properties. Neuromorphic systems constitute a great opportunity for the future of electronics since they are scalable [62] and can combine both analog and digital synaptic functions compatible with large-scale integration circuits. This overcomes traditional limitations while offering the advantages of neuromorphic computing [41] revealing the beneficial role of hybrid chips as recently demonstrated in robotics [63]. Specifically, an autonomous standalone robot that uses integrated organic neuromorphic (organic electrochemical transistors and organic MEMS) was shown to learn through sensorimotor integration. Coupling neuromorphics with hybrid chips leads to robotic systems with low energy consumption and easy-to-tune architecture. These adaptable and decentralized autonomous robotic devices certainly pave the way toward more complex behaviors. Neuromorphic sensory systems can also be integrated on stretchable substrates. Combining various technologies and materials such as quantum dot light-emitting diodes, capacitive pressure sensors, resistive RAM synapses, neural network processing, as well as intrinsically stretchable materials (i.e., PDMS polymer), a highly versatile neuro synaptic system can be created. This hybrid system can adapt to different mechanical deformations, making it suitable for wearable electronics as well as HMI.

Distributed energy systems are an inseparable unit in the next-generation wearables and robotic systems. This novel architecture offers features such as high flexibility, availability, and eco-friendliness, while enables devices that are safe, have high efficiency, and are self-sustainable. Bioinspired distributed energy could enable novel technologies where energy sources are critically needed for autonomous robots to work in unstructured environments for extended periods [64]. Inspired by nature, multifunctionality integrates energy storage, actuation, and sensing in a combined unit within the device by using electroactive polymers and batteries, allowing this way to reducing the weight of the robots and perform more complex tasks. Specifically, distributed energy harvesting, and storage can benefit wearable systems and even a swarm of micro-/ nanorobots. This decentralized power structure constitutes an efficient solution for robotic applications while having the potential for universal application. All those benefits will contribute in making our everyday life smarter with applications in Big Data, AI analytics, IoT, autonomous robots [64], digital twin simulations, and neurotechnology.

## 5 Challenges

### 5.1 Steps for addressing the current challenges

The first step towards developing semi-flexible hybrid chips is to adapt and structurally integrate conventional semi-rigid circuits onto substrates that are commonly used in flexible electronics [50] (Fig. 6). This is an important path to develop (semi-) flexible hybrid chips exhibiting foldable and stretchable functions compatible with new generation of electronics that are required within IoT. The second step is to transfer and adopt the multi-chiplets approach [65] already developed in rigid hybrid chips technology, to (semi-) flexible hybrid chips (step 2 in Fig. 6). Integrating multiple components, such as sensors, energy generation and storage units and communication interfaces in a single platform or structure has been

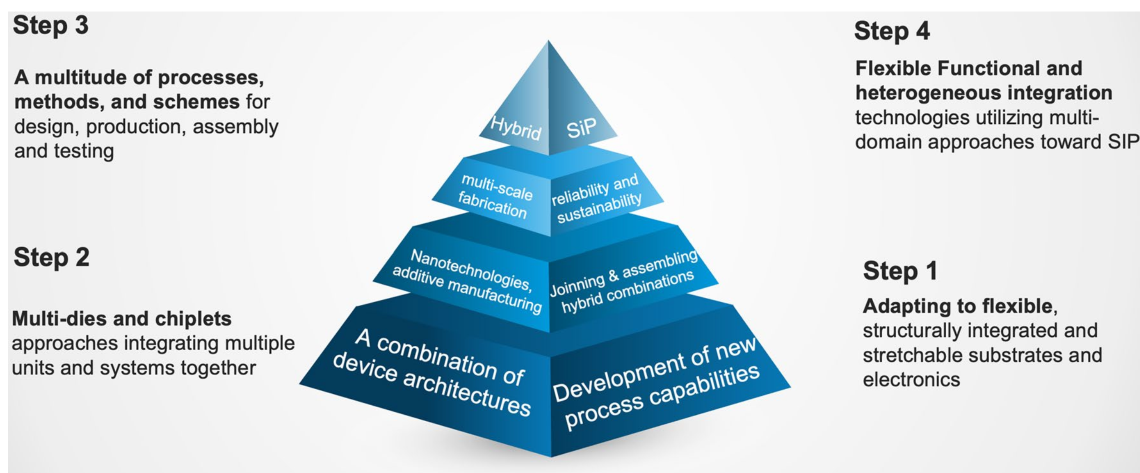


**Fig. 6** Hybrid Chips for developing heterogeneous SiP and multi-chiplets, bringing together conventional semiconductor technologies with flexible electronics towards a new generation of electronic components and systems for a sustainable future

already demonstrated as a promising path in rigid hybrid chips technology. This approach allows for the heterogeneous integration of various materials and components into platforms targeting emerging applications with a key focus on low power consumption during manufacturing stages while producing components with energy-efficient operation. As a third set, a multitude of efficient manufacturing processes, methods, and testing schemes should be developed providing a comprehensive framework for the design, production, assembly as well as testing of the various components and systems (step 3). This will ensure sustainability and reliability during production, development, and evaluation.

Novel hybrid chips development require multi-disciplinary and multi-domain approaches that will enable seamless interconnections between different devices and modules. A flexible functional and heterogeneous integration [66] of technologies on the component, module and system level should be demonstrated (step 4). Overall, hybrid chips (rigid or flexible) approach allows fostering of innovation and sustainability in the semiconductors industry accelerating IoT's mission. Below, we analyze the main challenges towards hybrid chips' further development, namely achieving reliable heterogeneous integration while developing suitable materials and processes towards sustainability in line with the electronic components and systems roadmap [67](Fig. 6).

## 5.2 Materials and Processes Development

Identifying the right materials and manufacturing processes to be developed is a crucial step and a significant challenge in the progression of hybrid chips. Specifically, (semi-) flexible hybrid chips require a multitude of processes, as well hybrid combinations, and novel additive manufacturing techniques, to ensure sustainable and cost-efficient manufacturing (Fig. 7). The transition to non-silicon and non-silicon compatible materials, or at least thinned Si ICs, requires substantial research to identify suitable substrates, active compounds, and packaging materials. These materials need to have properties that are either complementary or better than silicon [42, 68, 69] and offer new functionalities that expand the range of hybrid chip applications. Towards SiP implementation, power autonomy and power efficient computational resources are required that is achievable through a physical and functional integration. An extension of semiconductors coverage beyond silicon is required including advanced materials that are abundant, recyclable and non-toxic, as well as biocompatible / biodegradable substrates.

Layered 2D materials (LM) possess a great potential [68–70] thanks to their exceptional properties while at the same time offering easy integration processes with silicon CMOS technology making them the perfect candidate in order to expand conventional silicon chips functionalities. Unique properties such as high surface-to-volume ratio, tunable electronic properties as well as incredible mechanical and optoelectronic capabilities enable these materials to be applied in a number of applications from gas, chemical, and biosensing to events MEMS/NEMS, optoelectronics, photonics, neuromorphics and even quantum computing [68–70] 2D materials are particularly interesting because of their hybrid integration compatibility with conventional CMOS circuits such as transistors [72]. LM are usually grown on rigid substrates and then are transferred to flexible substrates, requiring the need of complex transferring process that could affect the quality and electrical properties of LM [73, 74].

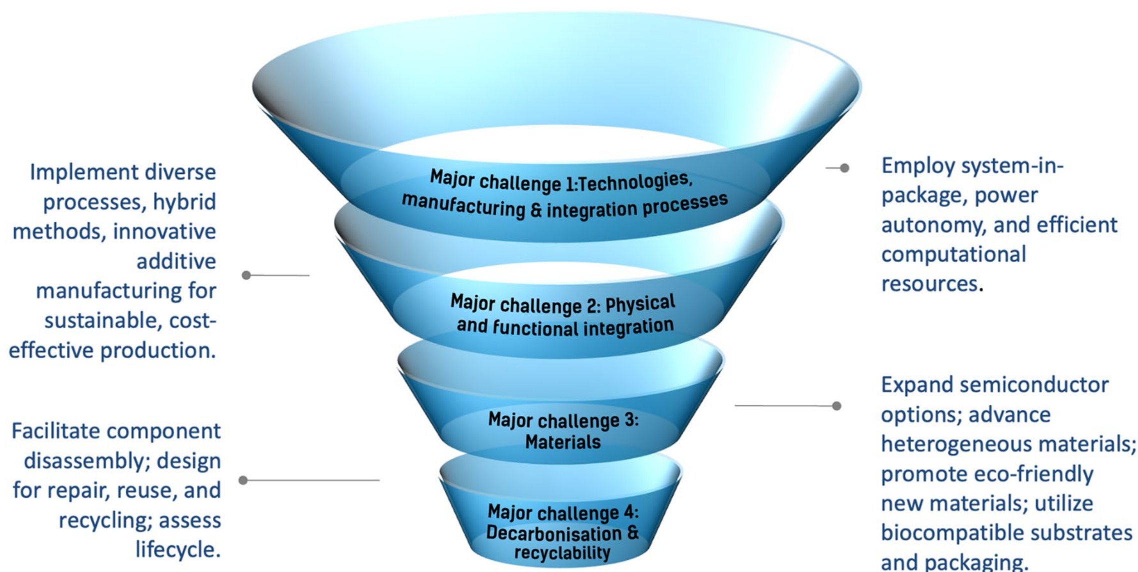


**Fig. 7** Main challenges towards hybrid chips' further development in line with the ECS roadmap

Although LM possess promising properties for advancing chips technology, their limited manufacturing at scale, while adhering to industry standards, is still under progress. High processing temperatures are required for producing LM with high quality, while controlling the contact interfaces present difficulties. The performance of devices utilizing these materials is still limited and only demonstrated in lab scale, originating in low quality interfaces and contacts. Precise etching or layered 2D material removal poses another challenge. Meanwhile, the objective of the European Experimental Pilot Line for layered LM [71] is to overcome these manufacturing bottlenecks. Despite these challenges, LM are excellent candidates for various applications such as integrated circuits, neuromorphic computing, and quantum technologies. They could also be ideal for sensing applications requiring high sensitivity, photonic and optoelectronic applications due to their unique properties like low surface carrier scattering and direct band gap. Nevertheless, the successful integration of these materials on industrial level depends on whether the above mentioned technical challenges can be overcome [70].

Another factor to consider is the availability of these materials at large quantities as well as their sustainability (Fig. 7). These newly implemented materials and processes must be more environmentally friendly than their previous counterparts and need to be recyclable to minimize their environmental impact. The whole initiative should support circular economy while avoiding the e-waste issues of silicon-based technology [75]. The efficient recycling and reuse at the end of the life of new materials is also crucial, and it can substantially contribute to the overall sustainability of electronics and technology in general. At the same time, those materials and processes must maintain safety conditions both for the end user as well as for the people involved in the development process. There is a need, therefore, for non-toxic precursors and solvents to ensure that their use and disposal after usage do not negatively affect the environment. All the above need to be ensured while retaining high levels of performance and reliability for the intended use case scenario. This smooth technological process transition for hybrid chips is required to fulfill the prerequisites of chips industry and therefore ensure its success. Revolutionizing the materials used in chip applications has the potential to revolutionize the semiconductor sector and help advance beyond Moore's Law.

### 5.3 Heterogeneous Integration, Scalability, Standardization, and Reliability Testing

Achieving heterogeneous integration and demonstrating scalability potential are key prerequisites for the successful deployment of hybrid chips, either being developed on rigid or flexible substrates. This development involves tackling issues of material compatibility as well as scalable manufacturing processes, system integration, standardization, testing, and reliability. Despite the many advantages of chiplets, multi-die systems have not yet seen widespread adoption—there are still many necessary innovations to be implemented related to rigid hybrid chips. Developing effective strategies for integrating various materials and technologies in hybrid chips requires addressing the complexity of heterogeneous integration [76]. All targeted sub-units of hybrid chips must be compatible with existing hardware and software

infrastructures. Integrating different materials and technologies requires the consideration of material compatibility since different materials can have distinct electrical, mechanical, and thermal properties. This includes physical dimensions, power requirements, interface mismatch issues, and many more. Incompatibility therefore can significantly hinder adoption of emerging technologies. The physical size of components, interconnections, layer transitions, as well as the interface quality between chiplets and the size of the package could limit the bandwidth of targeted systems.

Semi-flexible hybrid chips require combining the manufacturing processes of silicon CMOS chips and flexible electronic components into a seamless, cost-effective manufacturing line. This is a complex activity since new equipment or significant modifications are required placing a barrier to fast adoption of this emerging technology. Existing electronic design automation tools optimized for rigid, planar substrates should be adjusted increasing complexity and cost, while new tools and design methodologies should be developed to address specifications of flexible hybrid chips. Ensuring compatibility between flexible hybrid systems and existing CMOS-based systems in terms of thermal and mechanical properties, required voltage levels, communication protocols, and power requirements is also essential. Flexible substrates typically have poorer thermal conductivity than silicon, posing challenges in heat management for high-power applications, while operate at different voltage and power levels. Notably to mention, differences in thermal expansion coefficients between silicon chips and flexible substrates can cause reliability issues, thus stress at the interface can lead to device failure.

Thinned silicon ICs, featuring tiny touch pads, are fragile, while standard assembling tools can damage the final hybrid chip as a result of enhanced heat conduction. There is also a need to design strategies for flexible interconnections to ensure efficient communication between subsystems, at required operation frequency and minimum signal noise. Developing interconnects that can withstand multiple bending and sending cycles, while maintaining high electrical conductivity is challenging. Conventional metallic interconnects may not be suitable to operate under these conditions, urging for the development of stretchable conductive materials, i.e., based on LM or other novel material. Demonstrating interconnections that allow transmission of low noise signals across hybrid systems can be demanding due to the different electrical performance of flexible materials especially at high frequencies.

Identified processes should allow scalability for larger use case scenarios [77] avoiding units failure considering relevant mechanical and thermal stress during fabrication (Fig. 5).This is a crucial step to ensure smooth system heterogeneous integration. The demonstration of large-scale hybrid chips is a major challenge. Scaling up manufacturing should be compatible with increased volume, while maintaining the same chips quality and yield. This is a demanding task for hybrid chips due to their inherent complexity and the required heterogeneous integration of multiple technologies on the same package. Maintaining the same performance across all chips at scaled up production becomes challenging, since slight variations in one sub-unit of the system can significantly impact the overall chip performance. One of the advantages of hybrid chips is their customization features rendering them applicable to various applications such as consumer electronics, automotive, or medical devices. At the same time, however, this induces a barrier for the upscaling of hybrid chip technology because each application field has specific requirements that all should be taken in account to meet these diverse needs. Managing heat dissipation and power becomes more challenging for upscaled demonstrations. This is crucial in applications like data centers or high-performance computing, where the density of computing power (and hence heat generation) is very high.

The scalability of hybrid chip technologies is also dependent on the availability and current cost of precursor materials, especially if CRM are part of the hybrid chip, making large-scale production financially or logistically challenging. The upscaling of semi-flexible hybrid chips depends on the availability and cost-effectiveness of flexible substrate materials like polyimide, parylene, or other polymers. Scaling up their production involves adapting existing fabrication techniques (like lithography) for flexible substrates or developing new methods that can reliably be used to print flexible chips on these materials. Moreover, in semi-flexible chips peripheral units like batteries, antennas, and sensors (not all necessarily flexible), should be integrated with flexible units. The integration of flexible units with conventional CMOS electronics, and hybrid chips into existing systems in general, requires the development of standardized methodologies whereas a specific focus should be given on interconnect and communication standards. Hybrid chips should effectively communicate with other components thus enabling their seamless integration and their wider adaptability. UCIe will likely be a critical part of enabling chiplet innovation in rigid hybrid chips.

Another important ingredient for hybrid chips' further deployment is the development of reliability testing protocols to verify whether a product can operate consistently over the duration of a given life cycle. Developing strategies for efficient testing methods to ensure their performance and reliability could also give feedback to standardization methodologies. When it comes to package reliability study, possible difficulties include warpage, chip cracking, delamination, toughness fracture, plastic deformation, and many more. The system can fail in a variety of ways, including stress fracture,

high-temperature deformation and degradation, open circuit, short circuit, line impedance mismatch, electromagnetic interference, and many others. Maintaining consistent performance and reliability as (semi-)flexible hybrid chips production scales is challenging due to potential variability in flexible substrates and the sensitivity of organic materials used in some flexible electronics. In particular, ensuring compatibility and reliable electrical connections as production scales is crucial- a demanding task that requires extensive testing at various conditions. Accelerated lifespan testing, which is often employed in conventional silicon devices, may also be applied to hybrid chip's reliability testing. Mechanical tests encompass the investigation of bonding processes, materials, and their tensile strength during bending, stretching, and twisting. The interfaces between rigid components and printed circuit lines should be tested using repetitive bending at a defined radius or shear force testing. This development of strategies for efficient testing [3], failure analysis, and fault tolerance will be critical to maintain the high standards required by semiconductors industry. Three factors—thermal management, mechanical stress, and electrical properties—can be investigated in specific use cases in order to detect and improve package reliability. The lack of standardized processes and materials for flexible electronics compared to the well-established standards in silicon-based manufacturing can be a limiting factor for scaling production.

Though the transition to (semi-) flexible hybrid chips adopting a multi-chiplet approach provides certain challenges, it opens the path for a variety of emerging applications. To address these challenges and effectively scale and integrate flexible hybrid chip technologies, ongoing R&I is crucial. Collaborations between academia, industry, and material science experts are essential to advance materials, manufacturing processes, and design tools. Additionally, developing universal standards and protocols for flexible chips will play a critical role in enabling their wider adoption and integration in existing products. This paradigm transition is expected to be a slow process, requiring incremental advancements in technology, manufacturing, and design methodologies. However, the potential applications of these lightweight, and versatile electronic devices are significant, securing already a lot of investments. Lastly, the integration of hybrid chips into consumer products requires society's adaptation in new technologies, while the benefits of these new chips should communicated to potential users allowing their successful integration into the market. Overcoming those obstacles will bring us one step closer to realizing market products based on efficient hybrid chips.

### 5.4 Economic implications for the technology transition to hybrid chips: manufacturing costs, economic feasibility and market readiness

A significant investment is required in R&D of hybrid chips, as described in previous sections, including addressing the cost of developing new materials, processes, and heterogeneous integration methods. While manufacturing costs of chiplet-based designs are in principle lower than standard CMOS (better yield due to smaller area), overall costs of rigid hybrid chips are still less clear. This is due to the complexity of integrating different technologies, the need for specialized equipment, and potentially lower yields in the manufacturing process at least during the initial production phase. Although the initial costs of developing and manufacturing hybrid chips are high, they may offer long-term savings in terms of energy efficiency, performance, and miniaturization benefits. More R&D is required on design, architecture, verification, and testing in order for this technology to offer systems with lower cost. In the near future, rigid hybrid chips may use materials that are less common or more expensive than those used in conventional silicon chips, however the economy of scale can reverse this situation in a longer term. After establishing the required infrastructures and technological tools for these emerging chips, production pace can ramp up leading to optimized processes reducing thus corresponding manufacturing costs.

The paradigm shift to flexible hybrid chips manufacturing is even more ambitious compared to rigid hybrid chips since this transition is a costly and time-consuming process that requires new manufacturing facilities, equipment, and specialized skill sets, leading to significant investment and training costs. Establishing a reliable supply chain for novel materials and components used in flexible hybrid chips is crucial and can be a severe limiting factor. Compatibility with current technologies and standards is crucial. As with any emerging technology, there is a risk associated with the uncertainty of market acceptance. The market readiness of semi-flexible or flexible hybrid chips is even less established compared to rigid hybrid chips. Although there have been significant advancements, it is still an emerging field compared to conventional silicon-based technology and rigid hybrid chips. Integrating flexible chips into existing product lines may require important redesigning effort, impacting their readiness for market exploitation, depending on how easily they can be integrated into existing systems and infrastructures. The market adoption also depends on consumer awareness and on what benefits flexible chips can offer to their lives. In specific applications like wearable technology, the long-term benefits due to the durability and versatility of flexible chips may justify the higher initial costs. Furthermore, there is strong potential to create new product concepts such as foldable smartphones and smart textiles, establishing

significant market opportunities, which can be an important factor in the cost–benefit analysis. The application of hybrid chips is foreseen in smartphones and laptops, while the challenge is to integrate them without significantly increasing the cost or affecting device form factors. Another targeted domain is the automotive sector (electric and autonomous vehicles) that can benefit from the advanced capabilities of hybrid chips.

The market is more likely to adopt hybrid chips if they offer significant performance benefits over conventional chips. This includes factors like increased performance, higher speed and efficiency, or extended functionality. This path requires reliability and safety standards. While hybrid chips can significantly improve performance and energy efficiency, integrating them into existing data center infrastructures requires careful management of power and cooling systems. In medical applications, the challenge is not just technical integration but also compliance with healthcare regulations and ensuring reliability. Hybrid chips could revolutionize this sector, but integration requires robustness in harsh environments and seamless communication with control systems. Hybrid chips might open new market opportunities in fields like AI, quantum computing, AR/VR features, or IoT, where conventional chips might not be competitive. This potential for establishing new markets can justify the initial high costs or the high risk that companies should take aiming at gaining a significant competitive advantage. Hybrid chips might offer environmental benefits, like reduced energy consumption, low manufacturing temperatures, extended flexibility, and emerging functions that can be a significant factor in their overall cost–benefit analysis, especially in a market increasingly concerned with sustainability.

Semiconductor chips in general have a very high market value and have a very high compound annual growth rate (CAGR). A study from custom market insights (Fig. 8) showed that they could reach a market of 1.12 trillion by 2023 [78]. The GAGR for this study was approximately at 7.1% but in 2023 according to Gartner a decline of the market was reported by 10.9%, but it is expected to reach back on target at 2024 with a rise of 17% [79]. On the other hand, the growth for hybrid chips is multiple times higher, signifying their projected use case scenarios (Fig. 8). According to Veracious Statistics Research, the market value for hybrid chips at 2020 was 21.14 billion with an CAGR of 41.2% that based on our estimations (Fig. 8) could reach a staggering 236.56 billion market size in 2027 almost half of the current semiconductor market [80]. Flexible hybrid chips also exhibit approximately double growth rates in comparison to conventional semiconductor chips. The market value at 2021 was approximately 125 million with a projected growth of 16% reaching close to 411 million in 2029 and approximately 306 million in 2027 according to a statistical research by maximize market research [81]. This market analysis for each technology with the projected market growth indicates the projections of the market for hybrid chips is highly favorable.

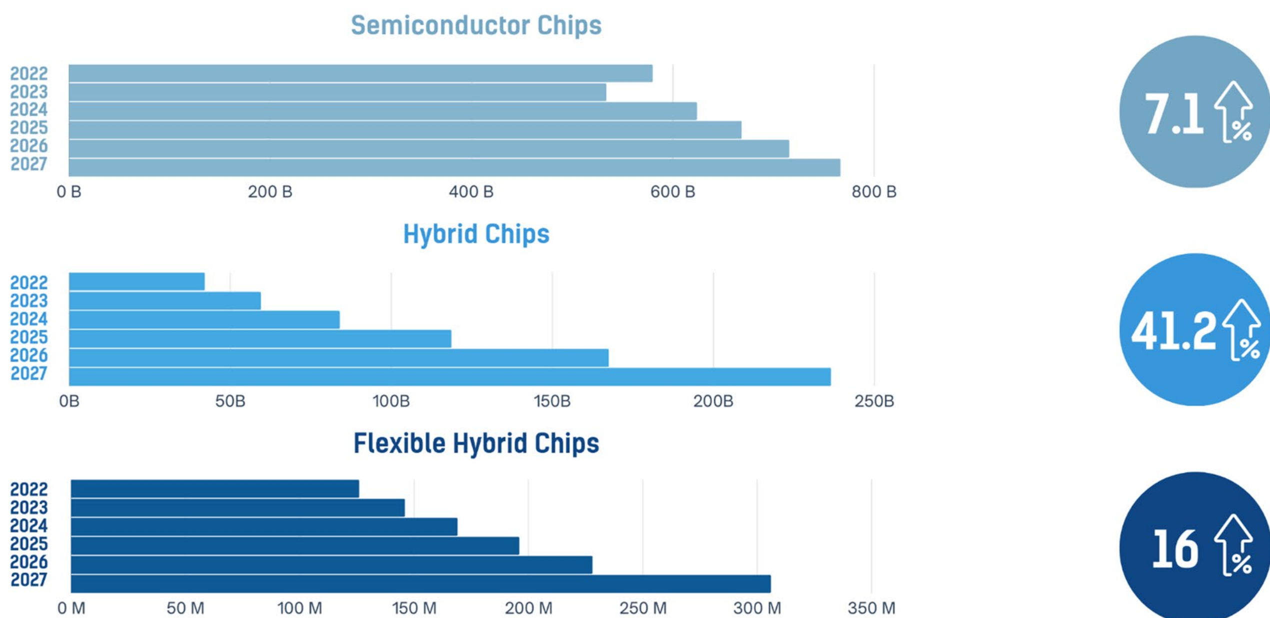


**Fig. 8** Approximate predictions of market sizes for semiconductor devices, hybrid chips and flexible hybrid chips in the period of 2022–2027

In summary, while the transition to hybrid chip technologies presents significant economic challenges, including high initial costs and market adoption barriers, it also offers potential long-term benefits like performance improvements, new market opportunities, and environmental advantages. Balancing the high initial costs and market readiness issues against the potential long-term benefits and opportunities is crucial in assessing the feasibility of transitioning from conventional silicon chip technologies to rigid or (semi-)flexible hybrid chips. The decision to invest in hybrid chips technology should be based on a careful consideration of these factors, alongside the constantly evolving landscape of consumer demands and technological advancements.

### 5.5 Sustainability and Circular Economy

The sustainability aspect of minimizing environmental impact that spans across various categories such as greenhouse gas emissions, human and ecological toxicity as well as the depletion of natural resources, is pivotal for the successful and sustainable development of Hybrid Chips. As a notably example, market estimates indicate that ~ 40 billion passive RFID tags are produced annually, with ~ 24 billion used in retail tagging [82]. Considering only the greenhouse gas emissions associated with tag production, (~ 20–120 g $CO_2$ eq.) [83], this corresponds to 1 – 5 million tons of greenhouse gas (GHG) emissions, with additional environmental impacts arising from contamination of paper or recycling waste streams. Therefore, design for energy efficiency and durability, repairability, upgradability, maintenance, reuse and recycling will be an essential part of IoT device development. This would bring IoT devices in line with regulations, e.g., EU Eco-design directives, which are currently in place for large electronics items [15], and are foreseen for consumer electronics devices, including phones, tablets and chargers.

In order to promote sustainable practices, it is important to consider the repairability and reusability of hybrid chips during the design phase [84]. This could work by including the standardization of the process steps in order to accommodate these practices, such as designing modular components or employing standardized connections and individual parts without the need to discard the whole device. This is also crucial to ensure that hybrid chips can be easily disassembled and sorted through the recycling process. In that way, valuable resources can be conserved, limiting the environmental impact [13, 16] of hybrid chips. Biodegradable materials are another sustainable approach allowing them to be naturally disassembled at the end of their use and their lifecycle. To address this, we need to take into account the expected lifetime period [85] of the hybrid chips and provide an assessment that can lead to overall improvements in the chips designing process and reduce the environmental footprint as well as prolong their life duration leading to better-performing devices with high durability. It's therefore important that hybrid chips are designed by considering circular economy and promoting sustainable practices.

## 6 Recent advancements in hybrid chips' prototypes and products

In previous sections, we have introduced three main categories of hybrid chips, namely rigid hybrid chips, semi-flexible and flexible hybrid chips. Besides, basic elements of the various hybrid chips' architecture, integration and packaging technologies were presented, revealing that concepts from one chip category can be applied to others. For instance, the multi-chiplet approach of rigid hybrid chips could be applied also in flexible hybrid chips upon required modifications. Moreover, all the above centralized SiP advanced packaging solutions, implemented either on rigid or flexible substrates, have their own characteristics and advantages aiming at increasing the power density, reduce size and enhance system performance for targeted applications. Specific modifications are applied depending on the application such as developing consumer electronics, healthcare devices, wireless communication units, power modules, processors, MEMS based sensors, lasers, circuits for industrial automation, automotive, and data centers, just to name a few examples. In the following section, we summarize recent advancements across the various hybrid chips categories.

### 6.1 Advances in rigid hybrid chips

Progress in advanced packaging technologies such as SiP, 3D integration, and multi-chiplet designs enabled enhanced performance, functionality, reduced manufacturing costs and enhanced reusability through reconfiguration process [86] for application-specific developments. Sophisticated packaging technologies are being tailored for AI and ML applications where high-bandwidth memory integration and energy-efficient designs are important. Multi-SiP technology has been implemented in various rigid hybrid chips such as wireless communication systems, power supply units, CPUs, lasers,

and MEMS-based sensors. Specifically, multi-SiP technology has been reported as one of the best pathways in developing MEMS-based sensors offering scaled down systems with light-weight [87, 88]. Photonic silicon-based sensors can be used to improve the performance of medical diagnostics by speeding up processes like antimicrobial susceptibility testing. Specifically, it was shown that the use of sensors in 3D printed microfluidic devices reduces the time required for a diagnosis [89]. Besides, there is an important advancement of using SiP technology in laser packaging. Following this approach, a miniature laser or other optical components are attached to the chip to form a complete system, which is then soldered onto a PCB and connected to an electrical pin [90].

A next-level heterogeneous integration architecture has been recently released by Intel, termed as quasi-monolithic chips (QMC) approach, implemented in Intel Processors [23] constituting a groundbreaking advancement in rigid hybrid chips. QMC enables combinations of silicon processes and packaging techniques to create 3D architectures with ultra-high interconnections density to fit future computing and AI needs [23]. It uses inorganic materials like silicon dioxide while maintaining the chips cleanliness in the integration process as well as improving the thermomechanical stability of the structure. This arrangement allows for adjustable interconnections while being highly scalable. To achieve near-monolithic interconnections, the development of a modular QMC is implemented using the UCIe standard. This hybrid interconnection approach enables chipset interoperability with a power consumption of ten times less in terms of performance than regular die-to-die interconnects. QMC uses advanced hybrid bonding instead of soldered connections between the chips, while it uses a fine-pitch hybrid bonding layer as well as an ultra-thick oxide deposition. Overall, QMC is making advances in heterogeneous integration, interconnections density as well as modularity and combines elements from silicon processing and advanced packaging techniques, making it a serious candidate for the progression of hybrid chips, especially in comparison to conventional architectures**.** In order to maximize its benefits, modular chiplet interfaces should be developed to enable mix and match of chiplets between different chiplets, e.g., through chiplet interconnect standards [30]. These advances in rigid hybrid chips are reshaping the semiconductor industry, enabling more powerful, efficient, and compact electronic devices. As these technologies continue to evolve, they will play a critical role in the development of next-generation electronics across various sectors.

### 6.2 Advances in semi-flexible hybrid chips

The motivation of developing semi-flexible hybrid chips is to combine the advantages of both silicon ICs and printed/flexible electronics toward meeting the requirements of emerging application domains. This hybrid approach overcomes the limited performance of flexible electronics in intensive tasks such as data processing or communication by replacing them with silicon chips, while the final hybrid chip retains sufficient mechanical flexibility and stretchability enabled by the flexible units overcoming limits of rigid silicon chips in a clever manner. As an example, printing circuits currently demonstrate low-speed communication in the frequency range relevant for IoT applications such as e-label sensors, e-skin, bioelectronics, HMI, and mobile device technologies [8, 9]. On the other hand, flexible units can be embedded in real-world objects and on human bodies offering distributed monitoring and recording of a wide range of chemical, physical, and biological information. They can bend, fold, and stretch, which is essential for applications in wearable electronics, medical devices, and flexible displays. Printed sensors are used in semi-flexible hybrid chips to convert physical and chemical variables such as temperature, light, pressure, and chemical concentrations, to electrical signals, while energy harvesters provide the necessary operational power. Inputs from these electrical signals are usually processed with silicon chips that include analogue and digital circuitry to receive and process sensory input, execute signal processing, and transmit data to an external host through printed antennas or show information on a printed display. It is therefore important that conventional silicon-based CMOS techniques to be merged with other technologies, particularly printed electronics, to complement the promise of low-cost flexible chips.

Semi-flexible hybrid chips enabled by printed electronic components offer unique advantages such as manufacturing on soft substrates at large areas with high throughput and scalability, while these emerging device concepts with free-of-form structure could have a vast number of sensing applications. These include developments in skin-like electronics that can monitor health parameters and flexible sensors that can be integrated into textiles, in wearables and robotics, as well as in industrial, environmental, and agricultural sensing [91]. Radio-frequency identification (RFID) labels printed on IoT edge objects have been fabricated for logistics/tracking of fragile, sensitive, or costly goods. Such tags typically include a silicon IC, a printed antenna, and printed sensors. Printed electronics, on the other hand, suffer from batch-to-batch and device-to-device process variability, which should be reduced to ensure proper circuit performance. Because of the limited variability and performance of printed units at large area, only small modular circuits have been demonstrated as the first semi-flexible hybrid chips, while silicon ICs provided the demanding functionality. The number of contact pads

grows according to the number of I/O required to interact with all the subunits of an ASIC chip. The number of required pads in modern ASIC chips has been increased, while their assembly method limits chip designs resulting in costly manufacturing. In complex chips, the pads should cover most of the silicon-chip surface, making the technology too costly for many of the targeted e-label applications. Ersman et al. recently demonstrated that printed electronic components based on organic electrochemical transistors can be produced and integrated with silicon ASIC toward semi-flexible hybrid chips implementation reducing the required number of pads while cutting production costs dramatically [92].

Christou et al. recently showed the sequential application of direct TP and CP to demonstrate the integration of nano- to chip-scale structures on flexible substrates, offering a novel printing platform for semi-flexible hybrid chips. [9] The team demonstrated that an initially 520 µm -thick Si chip was thinned down to 35 µm utilizing a backside lapping approach aided by a poly(methyl methacrylate) (PMMA) sacrificial layer. The thinned chips were then carefully integrated onto flexible substrates via direct TP. The applied contact force was an important parameter in determining the transfer yield of direct TP. It was reported that an applied force of 5 N was adequate to remove the ultra-thin chips off the stage without causing any cracks or defects. A novel printing platform was then developed to merge conventionally made and in-house thinned chips with sophisticated nanoscale electronic layers of nanowires. The researchers used direct ink write (DIW) printing to define the metal electrodes or interconnections for the semi-flexible hybrid system on a flexible substrate (Fig. 3). Specifically, direct TP method was employed to place MOSFETs based on ultrathin silicon chips at selected location, while photodetectors were built using ZnO nanowires (formed by DIW technique) connected to the ultrathin chips using a custom made semi-automated contact printing system.

A high transistor density integration was recently demonstrated utilizing LM of hexagonal boron nitride. These devices were fabricated using a 180 nm CMOS platform achieving high endurances > 5 million cycles for a 5by5 memristive transistor crossbar [72]. Another example of hybrid chips integrating LM was demonstrated using molybdenum disulfide ($MoS_2$). Films of $MoS_2$ have been synthesized at very low temperatures of about 150 °C, while their unique optoelectronic functionalities are paving the way for many novel applications of flexible hybrid electronics [73]. A wafer scale synthesis of $MoS_2$ at temperatures below 300 °C compatible to industrial scale production was recently reported, while direct integration with CMOS circuits was show cased indicating that the integration of LM with conventional CMOS silicon electronics is possible and efficient [74]. All the above showcase the added functionalities of LM integration with silicon chips that can lead to enhanced performance.

Research has also been focusing on how these flexible devices can be self-powered. Studies include the integration of thin-film batteries, energy harvesting techniques (like piezoelectric or solar), and low-power electronic design optimized for flexible substrates [22, 61, 93–95]. There's a growing interest in using flexible hybrid electronics for healthcare applications, smart implants, smart bandages for wound monitoring, and flexible sensors for real-time health monitoring [96, 97]. Research has led to the development of skin-like electronic patches that can monitor various health parameters and even deliver drugs. These devices often integrate flexible sensors for monitoring vital signs (like heart rate, temperature, and blood pressure) or assist in healing processes with thinned CMOS circuits for data processing, offering a new level of convenience and functionality in medical diagnostics and treatment [98]. They can be embedded in flexible materials conforming to the human body, like smartwatches, and even smart textiles [99].

Semi-flexible hybrid chips can be also used in in-vitro environments. This includes applications in drug testing, toxicology examination, and even to monitor the function of the intestinal barrier, preventing harmful substances such as toxins and pathogens and allow the normal flow of nutrients and electrolytes. Other in vitro applications include nutrients absorption monitoring and even personalized medicine development and modeling of gastrointestinal diseases [100]. This type of semi-flexible hybrid chips combines technologies from both gut-on-a-chip and transwell insert culture systems while integrating advanced materials and fabrication methods for biomimetic purposes. The goal of this is to model and study cellular interactions and behaviors under controlled conditions by using a biomimetic chip model of a lifelike intestinal barrier. For these semi-flexible hybrid chips, a lithography was implemented using polydimethylsiloxane (PDMS) that is a biocompatible elastomer. It enables the formation of a better intestinal barrier by including the transwell insert that is essential for the abovementioned use cases while being versatile, scalable, and adaptable to those applications. This is a novel approach paving the way for the future of hybrid chips in the pharmaceutical sector [101].

These novel hybrid chip fabrication routes will open new avenues in semi-flexible hybrid chips field to meet the high-performance and sustainability requirements of a wide range of applications such as integrating flexible MEMS components with silicon-based circuits. Silicon based chips will enable scaling down thus better performance that is critical for IoT devices, while flexible MEMS can offer a solution to protect delicate components like pressure sensors and microphones during the manufacturing process [102]. While these examples highlight the diverse applications of flexible hybrid chips, they also highlight challenges in manufacturing, durability, and integration with existing technologies. Each

application requires a tailored approach to material selection, circuit design, and manufacturing processes. Despite these challenges, the successful implementation in these case studies demonstrates a growing trend towards more ubiquitous and versatile electronics in various aspects of everyday life.

### 6.3 Advances in flexible hybrid chips

As described in Sect. 2, flexible hybrid chips are the most promising technology as a path going beyond silicon chips to address the sustainability issues related to e-wastes and environmental impact in general. This should be the case at least for some targeted applications such as responsible and transient electronics, where low manufacturing cost and zero environmental impact are priorities [17].

Flexible hybrid chips offer versatility of flexible substrates allowing a very low processing temperature while avoiding complex heterogeneous integration approaches. They often integrate various electronic components – such as organic semiconductors, sensors, and conductive interconnects – onto a flexible material like plastic or polymers (Polyethylene terephthalate, PET, or Polyimide, PI). This technology offers several advantages, such as it can bend, fold, and stretch, which is essential for applications in wearable electronics, medical devices, and flexible displays [50, 103]. Being inherently thin and light, these chips are ideal for integration into clothing, flexible screens, and portable electronics without adding bulk or weight. Flexible hybrid chips are less prone to breakage compared to rigid or semi-flexible hybrid chips, making them suitable for applications where chips might fail due to mechanical stress [104] Certain flexible materials are biocompatible, allowing these chips to be used in medical implants and sensors that directly interface with the human body [105]. They enable new applications in areas like smart textiles, foldable electronics, implantable medical devices, and more, which are not feasible with rigid or semi-flexible hybrid chips [106]. Similar implantable devices with flexible sensors for health monitoring [107] are able to measure blood pressure, blood oxygen saturation or even monitor the progression of cardiovascular diseases.

There have been many advancements recently towards demonstrating flexible hybrid chips without requiring thinned silicon ICs, supporting the fact that are a substantial part of the future market of sustainable electronics. The collaboration between Arm and Pragmatic has led to groundbreaking advancements in flexible hybrids chips [10, 108]. Specifically, the team have initially demonstrated the fabrication a flexible hardwired processing engine based on integrating flexible metal-oxide thin-film transistors (TFTs) enabled by indium-gallium-zinc oxide (IGZO) with organic sensors, for usage in odor recognition application [108]. This study showcased a flexible, efficient chip with low power consumption that incorporates both nanoscale field programmable gate arrays as well as metal-oxide-based TFTs. The low power consumption of this device as well as the efficient implementation of ML algorithms, i.e., algorithm UB-FVC, renders the system more efficient and compact offering high gate density per area. This work demonstrated that flexible chips allow more complex designs to be implemented in less space, with improved overall performance and enhanced sustainability.

Besides, the teams recently presented a flexible 32-bit microprocessor fabricated using a 0.8 μm metal oxide TFT technology, [10] compatible with existing Arm Cortex-M class toolchains that completely simplifies the adoption process and makes it easier to develop it further, enabling new opportunities and applications. Arm and Pragmatic's vision towards flexible circuits integrates several different technologies, such as TFTs being built on a flexible substrate such as polyimide, avoiding the use of silicon wafers and conventional silicon-based manufacturing technology. This innovation enables the creation of flexible low cost and ultra-thin processors that can be implemented in everyday devices creating a new generation of IoT devices manufactured at low temperatures with minimum material waste. Another great feature of this technology is its ability for application-specific innovation. This technology is tailored-made specifically for emerging applications such as fast-moving consumer goods, mass market healthcare, and smart packaging domains that all require devices prepared by low cost and are only needed for a short amount of time at high production volumes (addressing responsible and transient electronics).

### 6.4 Commercial products enabled by hybrid chips

Several demonstrations of real-life applications of hybrid chips have been released. Those expand across various fields and industrial sectors, highlighting the high adaptability and versality of these technologies. In this section, a summary of recent commercial products enabled by hybrid chips is presented. Intel's Foveros technology represents a significant advancement in chip design [109]. It's a 3D stacking technology that allows logic chips developed across 3D, enabling more powerful, yet energy-efficient processors. Foveros has been used in Intel's Lakefield processors that are integrated in certain lightweight, high-performance laptops. Lakefield processors combine high performance

with energy efficiency thanks to their hybrid configurations that vertically stack processing cores. These devices have been tested in several consumer products such as Microsoft's surface and Lenovo's laptops. This is proof that hybrid chip technologies can deliver consumer electronics with high performance and efficiency.

Another advancement of hybrid chips was recently released by AMD related to Ryzen processors [110]. Specifically, AMD's Ryzen series of processors use a hybrid chip based on chiplet design. Instead of a single, large monolithic die, AMD uses multiple smaller chiplets. This allows for more efficient manufacturing and better yields. The chiplets in these processors are connected using AMD's Infinity Fabric, which allows for high-speed communication between them. This design is used across various products in the Ryzen line, including desktop and server processors. AMD's approach has allowed them to compete with Intel in terms of performance and price, demonstrating that hybrid chip technology can be a successful strategy in the highly competitive CPU market. Apple's M1 chip is a SoC that integrates several components, including the CPU, GPU, and Neural Engine, onto a single chip [111]. This integration is a form of hybrid technology, combining different functionalities and architectures. The M1 chip powers a range of Apple devices, including the MacBook Air, MacBook Pro, Mac Mini, and iPad Pro. Its implementation shows a significant performance and power efficiency improvement over previous Intel-based models. The M1 chip has been known for its performance gains and energy efficiency, proving the viability of highly integrated SoC designs in consumer products.

Google's Tensor Processing Units (TPUs) are custom-designed chips aiming at accelerating ML workloads [112]. They represent a hybrid approach by being specifically tailored for a particular type of computation, in this case, tensor operations which are fundamental to ML algorithms. TPUs are deployed in Google's data centers and are a critical part of their AI services. They power products like Google Search, Google Photos, and are also available to third-party developers through Google Cloud services [113]. Google's TPUs have shown significant performance improvements in ML tasks compared to standard CPUs and GPUs, showcasing the benefits of application-specific hybrid chip design in large-scale data center applications. Nvidia's Hopper architecture is another example, [114] designed for AI workloads but integrating both GPU and DPU (Data Processing Unit) functionalities. The aforementioned hybrid architecture is designed to as an AI accelerator, by providing versatility in different computational tasks in order to make significant impact on complex tasks such as deep learning.

Samsung and other smartphone manufacturers have explored flexible display technologies that incorporate flexible hybrid chips. Samsung's Galaxy Fold series is a prominent example [115]. These smartphones use flexible OLED displays and associated flexible circuitry to enable a foldable screen. The flexible hybrid chips inside allow the phone to maintain functionality even when bent or folded. The successful launch and adoption of foldable phones have demonstrated the viability of flexible hybrid chips in consumer electronics, offering new form factors and user experiences. Companies like Levi's and Google have collaborated on projects like the Jacquard smart jacket [116]. This wearable technology integrates flexible hybrid chips into the fabric of clothing. The integration of touch-sensitive fabrics and flexible circuitry allows users to control their mobile devices through simple gestures on their clothing. Such smart textiles have showcased how flexible hybrid chips can be embedded into everyday objects, turning them into interactive surfaces. E-paper display technology typically used by e-readers also typically implements flexible hybrid chip technologies. At the same time flexible e-readers depend on flexible hybrid chips for their integration [117]. This progress allows the creation of a device that is lightweight, durable and at the same time energy-efficient. This display technology is also implemented on public transportation signs, grocery store price tags offering clear visibility and adaptability in the context with minimal power consumption.

Many companies have developed wearable devices that use flexible hybrid chips [118]. In the case of MC10, the BioStamp Research Connect System, is in a form of a temporary tattoo that monitors the vital signs and similar medical data. Those devices include sensors and circuits integrated onto the skin and body of the users without being invasive and at the same time being comfortable for the user without interfering with everyday activities. These devices have also been successfully used in clinical trials and research studies for the monitoring of many parameters, showcasing the potential of hybrid chips in the biomedical sector. Specifically, research institutions and companies in the biomedical sector have developed bio-implantable electrodes that can monitor brain activity. These electrodes can also stimulate the neuronal system in order to achieve rehabilitation of neurological disorders such as Parkinson or traumatic brain injury or even stroke [119–121]. In these applications, these electrodes need to conform to the brain's surface and provide accurate measurements and stimulation. At the same time, they need to ensure biocompatibility in order to minimize rejection from the body. Early trials have shown promising results towards understanding neurological disorders and even rehabilitating process, highlighting the significance of flexible hybrid chips in the bioelectronics sector for advanced medical treatments.

Flexible hybrid chips have also been used in energy systems specifically for the integration of flexible solar cells, piezoelectric materials or even CMOS circuits for power management of thermoelectric generators. They can be utilized in wearables providing self-powered operation by harvesting ambient light energy. The integration of this technology with CMOS has led to further opportunities especially in consumer electronics [122–124]. One example is smart phones with foldable or even rollable displays by using thinned CMOS ICs with flexible Organic LED panels [125]. There has been significant interest in using hybrid flexible electronics for aerospace applications. This includes embedding sensors in aircraft or spacecraft structures for real-time monitoring of stress, temperature, or strain, providing valuable data for maintenance and safety [126]. Deploying flexible sensor networks combined with CMOS technology for environmental monitoring offers new opportunities in tracking pollution, climate conditions, or agricultural parameters [127]. These sensors can be distributed over a wide area, providing real-time data with high spatial resolution. In ophthalmology, smart contact lenses have been demonstrated that monitor ocular health parameters (like intraocular pressure) [128]. These lenses use flexible sensors and antennas combined with miniaturized CMOS circuits for continuous monitoring and wireless data transmission.

All the abovementioned real word use cases of flexible or rigid hybrid chips support the potential and versatility of this technology across various fields, spanning from wearables, to bioelectronic implants, e-paper displays and even flexible displays for smartphones. Each real world application demonstrates the practical benefits of this technology in terms of efficiency, performance and customization that hybrid chips offer.

## 7 Perspectives

In February 2022, the European Commission (EC) announced the European Chips Act initiative, a comprehensive set of measures worth of €45bn for strengthening semiconductor ecosystem in Europe [129]. Meanwhile, in January 2023, the Industry and Energy Committee of the European parliament has adopted two drafts on the EU Chips Act and its R&D companion termed as 'Chips Joint Undertaking' (Chips JU) [130]. In February 2023, the Members of the European parliament endorsed the text adopted by the Industry Committee and voted to adopt the Chips JU proposal [130]. The proposals target among others: investment in next-generation technologies, access across Europe to design tools and pilot lines for the prototyping, testing and experimentation of cutting-edge chips, and fostering skills, talent and innovation in microelectronics. All these provisions are indispensable as the most important step to become a globally competitive player in the development of semiconductor technologies will be to structure R&D and training activities in this direction.

More R&D funding and private investments are needed to shorten the translation path from the lab to the fab by enabling researchers to unlock the R&I capacity for next-generation and future sustainable hybrid chips through access to state-of-the-art infrastructure and platform technologies, leading expertise and training supports. Joint infrastructures and research facilities offering access both to conventional silicon ICs and emerging printed/flexible electronics will lower the barriers for academic and industrial researchers in the field. These joint infrastructures will offer access to technology blocks and key enabling capabilities for the sustainable semiconductor products based on hybrid chips. Specifically, bringing together actors of the two communities will facilitate the mutual transfer of knowledge and technologies towards an integrated, distributed research infrastructure. Providing such a comprehensive range of capabilities, these new joint facilities will become the equivalent of a 'breadboard' supporting accelerated innovation pathfinding in sustainable technologies. Investments are needed to provide the additional infrastructure necessary to sustain the semiconductor innovation pipeline at the early to medium readiness levels.

This requirement for new joint infrastructures has been well-supported since several innovative institutions have already stepped up to meet these demands and support the development of these hybrid chips. As notably examples, Fraunhofer EMFT, the Georgia Tech 3D systems packaging research centre, IMEC and the TNO Holst Centre, among others, are organisations that are prepared for the next generation of hybrid chips. The Fraunhofer EMFTs features roll-to-roll lithography and other advanced techniques that would enable flexible-thin chip designs with broad applications. Component miniaturisation will be achieved by hetero-integration of silicon and foils [131]. The Georgia Tech 3D systems packaging research centre is implementing ML strategies for flexible efficient electronics manufacturing by creating an open-source-process design tool that shortens design cycles and reduces costs [132]. TNO at Holst Centre is also a pioneer in the field, working on non-intrusive medical monitoring devices, multisensory foils, 3D-printed electronics, photonic soldering, and even laser mass transfer technologies for silicon on flexible substrates [133]. These institutions, among others, are pioneers in the field paving the way for future of hybrid chip technologies by investing in the proper infrastructure. This deployment is crucial in redefining the next generation of hybrid chips for digital and IoT applications.

Technology advances on hybrid chips enabled by integration of new materials, components, modules and systems will open the path for:

- **Embedded intelligence** with higher functionality, less or tunable requirements for HMI, improved interoperability, haptic interfaces, and lower demand for power resources. Design, development and production of heterogeneous autonomous systems that are able to sense and compute at the same node with ultra-low operation and standby power consumption.
- **Energy efficiency** through smart and intelligent battery/supercapacitor management, combination of functions and/or digital interfacing with sensors, transceivers, and microcontrollers to minimize system-level power consumption, multi-source energy harvesting and high-density, low-leakage storage devices to avoid battery replacement, and integration of new power-saving techniques (e.g. GaN-based switching) in combination with resource-efficient packaging technologies.
- **Enhanced features** such as reliability, security, safety, self-monitoring, error-correction and trustability that will become more crucial in near future. Physical and functional integration technologies can greatly support these features. New energy-efficient information processing paradigms such as in-memory-computing, neuromorphic computing and semiconductor quantum computation.
- **Paradigm shifts** related to the design, architecture and processing of new functional SiP, e.g., energy source in Package (eSiP), which are presently built using heterogeneous/hybrid integration on conformable or stretchable substrates for wearables and beyond.

Hybrid chips have the potential to reshape semiconductors industry and associated IoT deployment. This transition is supported by smart components, modules and systems that will enable the deployment of edge computing, while reducing the communication bandwidth requirements and the devices power consumption. Even though challenges in heterogeneous integration and material development need to be resolved, their wide applications range including robotics, wearable devices, IoT networks, etc., pushes forward the necessary R&D. The key recommendation for their success would be the continued investment in facilities to improve further integration and upscaling processes while developing novel sustainable materials and processes compatible with CMOS infrastructure. Furthermore, considering the significant sustainability impact of these technologies, it is crucial to adopt eco-friendly manufacturing processes that minimize environmental impact and support recycling and reuse after their end of life. For a successful market penetration of hybrid chips, collaborations between academic research and industry should be planned to facilitate knowledge transfer that will allow the quick development of required techniques and systems. As these efforts progress, the realization of hybrid chips will be achieved offering revolutionary solutions promising to transform the future of our communities. Hybrid chips hold not only the promise to reshape the whole electronics industry but also contribute significantly to global sustainability goals. Sustainable manufacturing processes for the development of energy-efficient and environmentally friendly solutions across many industries are in line with the multiple initiatives such as the New Green Deal, Chips Act and Circular economy plan**.**

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**Data Availability** Data (i.e., related to Fig. 8)available on request from the authors.

## Declarations

**Competing interests** The authors declare no competing interests.

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## References


1. Waly MM, Mickovski SB, Thomson C. Application of circular economy in oil and gas produced water treatment. Sustainability. 2023;15:2132. https://doi.org/10.3390/su15032132.
2. Lau JH. Recent advances and trends in advanced packaging. IEEE Trans Compon Packag Manuf Technol. 2022;12:228–52. https://doi.org/10.1109/TCPMT.2022.3144461.
3. Appello D, Bernardi P, Grosso M, Reorda MS. System-in-package testing: problems and solutions. IEEE Des Test Comput. 2006;23:203–11. https://doi.org/10.1109/MDT.2006.79.
4. Heterogeneous Integration Roadmap. IEEE Electronics Packaging Society. https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html. Accessed 27 Apr 2023.
5. Zhang S, Xu X, Lin T, He P. Recent advances in nano-materials for packaging of electronic devices. J Mater Sci Mater Electron. 2019;30:13855–68. https://doi.org/10.1007/s10854-019-01790-3.
6. Berggren M, Simon DT, Nilsson D, Dyreklev P, Norberg P, Nordlinder S, Ersman PA, Gustafsson G, Wikner JJ, Hederén J, Hentzell H. Browsing the real world using organic electronics, Si-chips, and a human touch. Adv Mater. 2016;28:1911–6. https://doi.org/10.1002/adma.201504301.
7. Ma S, Kumaresan Y, Dahiya AS, Dahiya R. Ultra-thin chips with printed interconnects on flexible foils. Adv Electron Mater. 2022;8:2101029. https://doi.org/10.1002/aelm.202101029.
8. Khan Y, Thielens A, Muin S, Ting J, Baumbauer C, Arias AC. A new frontier of printed electronics: flexible hybrid electronics. Adv Mater. 2020;32:1905279. https://doi.org/10.1002/adma.201905279.
9. Christou A, Ma S, Zumeit A, Dahiya AS, Dahiya R. Printing of nano-to chip-scale structures for flexible hybrid electronics. Adv Electron Mater. 2022. https://doi.org/10.1002/aelm.202201116.
10. Biggs J, Myers J, Kufel J, Ozer E, Craske S, Sou A, Ramsdale C, Williamson K, Price R, White S. A natively flexible 32-bit Arm microprocessor. Nature. 2021;595:532–6. https://doi.org/10.1038/s41586-021-03625-w.
11. Life Cycle Analysis Whitepaper. In: Pragmatic Semicond. https://www.pragmaticsemi.com/life-cycle-analysis/white-paper. Accessed 29 Jan 2024.
12. Sustainable Manufacturing. In: Pragmatic Semicond. https://www.pragmaticsemi.com/sustainable-manufacturing. Accessed 29 Jan 2024.
13. Awasthi AK, Zeng X. Li J (2016) Environmental pollution of electronic waste recycling in India: A critical review. Environ Pollut Barking Essex. 1987;211:259–70. https://doi.org/10.1016/j.envpol.2015.11.027.
14. World Economic Forum Annual Meeting. In: World Econ. Forum. 2019. https://www.weforum.org/events/world-economic-forum-annual-meeting-2019/. Accessed 29 Jan 2024.
15. Ecodesign and Energy Labelling Working Plan 2022–2024. https://energy.ec.europa.eu/publications/ecodesign-and-energy-labelling-working-plan-2022-2024_en. Accessed 7 Nov 2023.
16. A European Green Deal. 2021. https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/european-green-deal_en. Accessed 5 May 2023.
17. Kang S-K, Yin L, Bettinger C. The emergence of transient electronic devices. MRS Bull. 2020;45:87–95. https://doi.org/10.1557/mrs.2020.19.
18. Yasuura H, Kyung CM, Liu Y, Lin YL. Smart sensors at the IoT frontier. Berlin: Springer; 2017.
19. Wang Y, Li Y, Wang T, Liu G. Towards an energy-efficient Data Center Network based on deep reinforcement learning. Comput Netw. 2022;210: 108939. https://doi.org/10.1016/j.comnet.2022.108939.
20. WmA W, McKee SA. Hitting the memory wall: implications of the obvious. ACM SIGARCH Comput Archit News. 1995;23:20–4. https://doi.org/10.1145/216585.216588.
21. Zidan MA, Strachan JP, Lu WD. The future of electronics based on memristive systems. Nat Electron. 2018;1:22–9. https://doi.org/10.1038/s41928-017-0006-8.
22. Rogdakis K, Loizos M, Viskadouros G, Kymakis E. Memristive perovskite solar cells towards parallel solar energy harvesting and processing-in-memory computing. Mater Adv. 2022;3:7002–14. https://doi.org/10.1039/D2MA00402J.
23. Elsherbini A, Jun K, Liff S, Talukdar T, Bielefeld J, Li W, Vreeland R, Niazi H, Rawlings B, Ajayi T, Tsunoda N, Hoff T, Woods C, Pasdast G, Tiagaraj S, Kabir E, Shi Y, Brezinski W, Jordan R, Ng J, Brun X, Krisnatreya B, Liu P, Zhang B, Qian Z, Goel M, Swan J, Yin G, Pelto C, Torres J, Fischer P. Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process. In: 2022 International Electron Devices Meeting (IEDM).2022; 27.3.1–27.3.4
24. Wang Z, Du Y, Wei K, Han K, Xu X, Wei G, Tong W, Zhu P, Ma J, Wang J, Wang G, Yan X, Xiang J, Huang H, Li R, Wang X, Wang Y, Sun S, Suo S, Gao Q, Su X. Vision, application scenarios, and key technology trends for 6G mobile communications. Sci China Inf Sci. 2022;65: 151301. https://doi.org/10.1007/s11432-021-3351-5.
25. Das R, He X. Printed, Organic & Flexible Electronics Forecasts. 2016. Players & Opportunities 2017–2027. Markert Report
26. innoLAE. 2020. In: InnoLAE—Innov. Large Area Electron. https://innolae.org/Innolae2020. Accessed 29 Jan 2024.
27. Tian W, Li B, Li Z, Cui H, Shi J, Wang Y, Zhao J. Using Chiplet Encapsulation Technology to Achieve Processing-in-Memory Functions. Micromachines. 2022;13:1790. https://doi.org/10.3390/mi13101790.
28. Di Mauro A, Scherer M, Rossi D, Benini L. Kraken: A Direct Event/Frame-Based Multi-sensor Fusion SoC for Ultra-Efficient Visual Processing in Nano-UAVs. In: 2022 IEEE Hot Chips 34 Symposium (HCS). 2022; 1–19.
29. Santagata F, Sun J, Iervolino E, Yu H, Wang F, Zhang G, Sarro PM, Zhang G. System in package (SiP) technology: fundamentals, design and applications. Microelectron Int. 2018;35:231–43. https://doi.org/10.1108/MI-09-2017-0045.
30. Das Sharma D, Pasdast G, Qian Z, Aygun K. Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level. IEEE Trans Compon Packag Manuf Technol. 2022;12:1423–31. https://doi.org/10.1109/TCPMT.2022.3207195.

31. Elsherbini A, Jun K, Vreeland R, Brezinski W, Niazi HK, Shi Y, Yu Q, Qian Z, Xu J, Liff S, Swan J, Yao J, Liu P, Pelto C, Rami S, Balankutty A, Fischer P, Turkot B. Enabling Hybrid Bonding on Intel Process. In: 2021 IEEE International Electron Devices Meeting (IEDM). 2021; 34.3.1–34.3.4. https://doi.org/10.1109/IEDM19574.2021.9720586
32. Ali M, Nabavi M, Hassan A, Honarparvar M, Savaria Y, Sawan M. A Versatile SoC/SiP Sensor Interface for Industrial Applications: Design Considerations. IEEE Access, 2022;10:24540. https://doi.org/10.1109/ACCESS.2022.3152379.
33. Mahajan R, Sankman R, Patel N, Kim D-W, Aygun K, Qian Z, Mekonnen Y, Salama I, Sharan S, Iyengar D, Mallik D. Embedded Multi-die Interconnect Bridge (EMIB)—A High Density, High Bandwidth Packaging Interconnect. 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), IEEE Xplore. 2016; 557–565. https://doi.org/10.1109/ECTC.2016.201.
34. Gupta S, Navaraj WT, Lorenzelli L, Dahiya R. Ultra-thin chips for high-performance flexible electronics. Npj Flex Electron. 2018;2:1–17. https://doi.org/10.1038/s41528-018-0021-5.
35. Soman VV, Khan Y, Zabran M, Schadt M, Hart P, Shay M, Egitto FD, Papathomas KI, Yamamoto NAD, Han D, Arias AC, Ghose K, Poliks MD, Turner JN. Reliability challenges in fabrication of flexible hybrid electronics for human performance monitors: a system-level study. IEEE Trans Compon Packag Manuf Technol. 2019;9:1872–87. https://doi.org/10.1109/TCPMT.2019.2919866.
36. Wu T, Chen X, Wen S, Liu F, Li S. Coupled excitation strategy for crack initiation at the adhesive interface of large-sized ultra-thin chips. Processes. 2023;11:1637. https://doi.org/10.3390/pr11061637.
37. Harendt C, Kostelnik J, Kugler A, Lorenz E, Saller S, Schreivogel A, Yu Z, Burghartz JN. Hybrid Systems in Foil (HySiF) exploiting ultra-thin flexible chips. Solid-State Electron. 2015;113:101–8. https://doi.org/10.1016/j.sse.2015.05.023.
38. Dahiya AS, Christou A, Neto J, Zumeit A, Shakthivel D, Dahiya R. In tandem contact-transfer printing for high-performance transient electronics. Adv Electron Mater. 2022;8:2200170. https://doi.org/10.1002/aelm.202200170.
39. Zumeit A, Dahiya AS, Christou A, Mukherjee R, Dahiya R. Printed GaAs microstructures-based flexible high-performance broadband photodetectors. Adv Mater Technol. 2022. https://doi.org/10.1002/admt.202200772.
40. Guo C, Pan Z, Li C, Zou S, Pang C, Wang J, Hu J, Gong Z. Large-scale programmable assembly of functional micro-components for advanced electronics via light-regulated adhesion and polymer growth. Npj Flex Electron. 2022;6:1–13. https://doi.org/10.1038/s41528-022-00180-w.
41. Christensen DV, Dittmann R, Linares-Barranco B, Sebastian A, Gallo ML, Redaelli A, Slesazeck S, Mikolajick T, Spiga S, Menzel S, Valov I, Milano G, Ricciardi C, Liang S-J, Miao F, Lanza M, Quill TJ, Keene ST, Salleo A, Grollier J, Marković D, Mizrahi A, Yao P, Yang JJ, Indiveri G, Strachan JP, Datta S, Vianello E, Valentian A, Feldmann J, Li X, Pernice WHP, Bhaskaran H, Furber S, Neftci E, Scherr F, Maass W, Ramaswamy S, Tapson J, Panda P, Kim Y, Tanaka G, Thorpe S, Bartolozzi C, Cleland TA, Posch C, Liu S-C, Panuccio G, Mahmud M, Mazumder AN, Hosseini M, Mohsenin T, Donati E, Tolu S, Galeazzi R, Christensen ME, Holm S, Ielmini D, Pryds N. 2022 roadmap on neuromorphic computing and engineering. Neuromorphic Comput Eng. 2022;2: 022501. https://doi.org/10.1088/2634-4386/ac4a83.
42. Rogdakis K, Karakostas N, Kymakis E. Up-scalable emerging energy conversion technologies enabled by 2D materials: from miniature power harvesters towards grid-connected energy systems. Energy Environ Sci. 2021;14:3352–92. https://doi.org/10.1039/D0EE04013D.
43. Stroobants S, Dupeyroux J, de Croon GCHE. Neuromorphic computing for attitude estimation onboard quadrotors. Neuromorphic Comput Eng. 2022;2: 034005. https://doi.org/10.1088/2634-4386/ac7ee0.
44. Tang X, Shen H, Zhao S, Li N, Liu J. Flexible brain–computer interfaces. Nat Electron. 2023;6:109–18. https://doi.org/10.1038/s41928-022-00913-9.
45. Yin J, Hinchet R, Shea H, Majidi C. Wearable soft technologies for haptic sensing and feedback. Adv Funct Mater. 2021;31:2007428. https://doi.org/10.1002/adfm.202007428.
46. van Wegen M, Herder JL, Adelsberger R, Pastore-Wapp M, van Wegen EEH, Bohlhalter S, Nef T, Krack P, Vanbellingen T. An overview of wearable haptic technologies and their performance in virtual object exploration. Sensors. 2023;23:1563. https://doi.org/10.3390/s23031563.
47. Fuchs A, Passarella A, Conti M. Compensating for sensing failures via delegation in Human–AI hybrid systems. Sensors. 2023;23:3409. https://doi.org/10.3390/s23073409.
48. Liu Y, Pharr M, Salvatore GA. A lab-on-skin: a review of flexible and stretchable electronics for wearable health monitoring. ACS Nano. 2017. https://doi.org/10.1021/acsnano.7b04898.
49. Papakonstantinopoulos C, Bousoulas P, Aslanidis E, Skotadis E, Tsigkourakos M, Tsoukalas D. Highly sensitive stretchable sensor combined with low-power memristor for demonstration of artificial mechanoreceptor properties. Flex Print Electron. 2022;7: 035024. https://doi.org/10.1088/2058-8585/ac88e1.
50. Wu H, Huang Y, Yin Z. Flexible hybrid electronics: Enabling integration techniques and applications. Sci China Technol Sci. 2022;65:1995–2006. https://doi.org/10.1007/s11431-022-2074-8.
51. Breitschaft SJ, Clarke S, Carbon CC. A theoretical framework of haptic processing in automotive user interfaces and its implications on design and engineering. Front Psychol. 2019. https://doi.org/10.3389/fpsyg.2019.01470.
52. Murali PK, Kaboli M, Dahiya R. Intelligent in-vehicle interaction technologies. Adv Intell Syst. 2022;4:2100122. https://doi.org/10.1002/aisy.202100122.
53. Zhang J, Yao H, Mo J, Chen S, Xie Y, Ma S, Chen R, Luo T, Ling W, Qin L, Wang Z, Zhou W. Finger-inspired rigid-soft hybrid tactile sensor with superior sensitivity at high frequency. Nat Commun. 2022;13:5076. https://doi.org/10.1038/s41467-022-32827-7.
54. Mystakidis S. Metaverse. Encyclopedia. 2022;2:486–97. https://doi.org/10.3390/encyclopedia2010031.
55. Ranno L, Gupta P, Gradkowski K, Bernson R, Weninger D, Serna S, Agarwal AM, Kimerling LC, HuOBrien JP. Integrated photonics packaging: challenges and opportunities. ACS Photonics. 2022;9:3467–85. https://doi.org/10.1021/acsphotonics.2c00891.
56. Zhang S, Li Y, Zhang S, Shahabi F, Xia S, Deng Y, Alshurafa N. Deep learning in human activity recognition with wearable sensors: a review on advances. Sensors. 2022;22:1476. https://doi.org/10.3390/s22041476.
57. Covi E, Donati E, Liang X, Kappel D, Heidari H, Payvand M, Wang W. Adaptive extreme edge computing for wearable devices. Front Neurosci. 2021;15:61130.
58. Kim SH, Baek GW, Yoon J, Seo S, Park J, Hahm D, Chang JH, Seong D, Seo H, Oh S, Kim K, Jung H, Oh Y, Baac HW, Alimkhanuly B, Bae WK, Lee S, Lee M, Kwak J, Park J-H, Son D. A bioinspired stretchable sensory-neuromorphic system. Adv Mater. 2021;33:2104690. https://doi.org/10.1002/adma.202104690.

59. Xavier MC, do Nascimento IT, Nogueira EC de F, Oliveira FDVR, Gomes JGRC, Santos GN. Neuromorphic Hardware Applied in the Development of Low-Power IoTs *. In: 2022 Symposium on Internet of Things (SIoT). IEEE Xplore, 2022; 1–4. https://doi.org/10.1109/SIoT56383.2022.10070266.
60. Polyzoidis C, Rogdakis K, Kymakis E. Indoor perovskite photovoltaics for the internet of things—challenges and opportunities toward market uptake. Adv Energy Mater. 2021;11:2101854. https://doi.org/10.1002/aenm.202101854.
61. Loizos M, Rogdakis K, Kymakis E. An electronic synaptic memory device based on four-cation mixed halide perovskite. Discov Mater. 2022;2:11. https://doi.org/10.1007/s43939-022-00032-4.
62. Kimura M, Shibayama Y, Nakashima Y. Neuromorphic chip integrated with a large-scale integration circuit and amorphous-metal-oxide semiconductor thin-film synapse devices. Sci Rep. 2022;12:5359. https://doi.org/10.1038/s41598-022-09443-y.
63. Krauhausen I, Koutsouras DA, Melianas A, Keene ST, Lieberth K, Ledanseur H, Sheelamanthula R, Giovannitti A, Torricelli F, Mcculloch I, Blom PWM, Salleo A, Van De Burgt Y, Gkoupidenis P. Organic neuromorphic electronics for sensorimotor integration and learning in robotics. Sci Adv. 2021;7:eabl5068. https://doi.org/10.1126/sciadv.abl5068.
64. Aubin CA, Gorissen B, Milana E, Buskohl PR, Lazarus N, Slipher GA, Keplinger C, Bongard J, Iida F, Lewis JA, Shepherd RF. Towards enduring autonomous robots via embodied energy. Nature. 2022;602:393–402. https://doi.org/10.1038/s41586-021-04138-2.
65. Kim M, Shin Y, Jo W, Shon T. Digital forensic analysis of intelligent and smart IoT devices. J Supercomput. 2023;79:973–97. https://doi.org/10.1007/s11227-022-04639-5.
66. Kumar A, Chang N, Geb D, He H, Pan S, Wen J, Asgari S, Abarham M, Ortiz C. ML-based Fast On-Chip Transient Thermal Simulation for Heterogeneous 2.5D/3D IC Designs. In: 2022 International Symposium on VLSI Design, Automation and Test (VLSI-DAT). 2022; 1–8.
67. ECS-SRIA. 2021. EPoSS. https://www.smart-systems-integration.org/publication/ecs-sria-2021. Accessed 30 Jan 2024.
68. Ma J, Liu H, Yang N, Zou J, Lin S, Zhang Y, Zhang X, Guo J, Wang H. Circuit-Level Memory Technologies and Applications based on 2D Materials. Adv Mater. 2022;34:2202371. https://doi.org/10.1002/adma.202202371.
69. Pescetelli S, Agresti A, Viskadouros G, Razza S, Rogdakis K, Kalogerakis I, Spiliarotis E, Leonardi E, Mariani P, Sorbello L, Pierro M, Cornaro C, Bellani S, Najafi L, Martín-García B, Del Rio Castillo AE, Oropesa-Nuñez R, Prato M, Maranghi S, Parisi ML, Sinicropi A, Basosi R, Bonaccorso F, Kymakis E, Di Carlo A. Integration of two-dimensional materials-based perovskite solar panels into a stand-alone solar farm. Nat Energy. 2022;7:597–607. https://doi.org/10.1038/s41560-022-01035-4.
70. Lemme MC, Akinwande D, Huyghebaert C, Stampfer C. 2D materials for future heterogeneous electronics. Nat Commun. 2022;13:1392. https://doi.org/10.1038/s41467-022-29001-4.
71. Parhizkar S, Prechtl M, Giesecke AL, Suckow S, Wahl S, Lukas S, Hartwig O, Negm N, Quellmalz A, Gylfason K, Schall D. Two-dimensional platinum diselenide waveguide-integrated infrared photodetectors. ACS Photonics. 2022;9(3):859–67. https://doi.org/10.1021/acsphotonics.1c01517.
72. Zhu K, Pazos S, Aguirre F, Shen Y, Yuan Y, Zheng W, Alharbi O, Villena MA, Fang B, Li X, Milozzi A, Farronato M, Muñoz-Rojo M, Wang T, Li R, Fariborzi H, Roldan JB, Benstetter G, Zhang X, Alshareef HN, Grasser T, Wu H, Ielmini D, Lanza M. Hybrid 2D–CMOS microchips for memristive applications. Nature. 2023;618:57–62. https://doi.org/10.1038/s41586-023-05973-1.
73. Hoang AT, Hu L, Kim BJ, Van TTN, Park KD, Jeong Y, Lee K, Ji S, Hong J, Katiyar AK, Shong B, Kim K, Im S, Chung WJ, Ahn J-H. Low-temperature growth of MoS2 on polymer and thin glass substrates for flexible electronics. Nat Nanotechnol. 2023;18:1439–47. https://doi.org/10.1038/s41565-023-01460-w.
74. Zhu J, Park J-H, Vitale SA, Ge W, Jung GS, Wang J, Mohamed M, Zhang T, Ashok M, Xue M, Zheng X, Wang Z, Hansryd J, Chandrakasan AP, Kong J, Palacios T. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. Nat Nanotechnol. 2023;18:456–63. https://doi.org/10.1038/s41565-023-01375-6.
75. Naik S, Satya Eswari J. Electrical waste management: Recent advances challenges and future outlook. Total Environ Res Themes. 2022;1–2: 100002. https://doi.org/10.1016/j.totert.2022.100002.
76. Xiang C, Jin W, Huang D, Tran MA, Guo J, Wan Y, Xie W, Kurczveil G, Netherton AM, Liang D, Rong H, Bowers JE. High-performance silicon photonics using heterogeneous integration. IEEE J Sel Top Quantum Electron. 2022;28:1–15. https://doi.org/10.1109/JSTQE.2021.3126124.
77. Taguchi K, Uemura T, Namba N, Petritz A, Araki T, Sugiyama M, Stadlober B, Sekitani T. Heterogeneous functional dielectric patterns for charge-carrier modulation in ultraflexible organic integrated circuits. Adv Mater. 2021;33:2104446. https://doi.org/10.1002/adma.202104446.
78. Global Semiconductor Chip Market 2023–2032. Markert Report. 2023. https://www.custommarketinsights.com/report/semiconductor-chip-market/. Accessed 29 Jan 2024
79. Gartner Forecasts Worldwide Semiconductor Revenue to Grow 17% in 2024. Market report. 2023. https://www.gartner.com/en/newsroom/press-releases/2023-12-04-gartner-forecasts-worldwide-semiconductor-revenue-to-grow-17-percent-in-2024. Accessed 29 Jan 2024
80. Hybrid Chip Market Size, Share, Growth, Industry, Statistic Report 2020-2027. Market report. 2020. https://www.veraciousstatisticsresearch.com/research-study/hybrid-chip-market/. Accessed 29 Jan 2024
81. Flexible Hybrid Electronics (FHE) Market - Global Industry Analysis and Forecast (2022-2029). Market Report. MAXIMIZE Mark. Res. 2023. https://www.maximizemarketresearch.com/market-report/global-flexible-hybrid-electronics-fhe-market-industry-analysis-and-forecast-2020-2026-by-type-application-and-region/99907/. Accessed 29 Jan 2024
82. Chang H. and Das R. RFID Forecasts, Players and Opportunities 2023-2033. Market report. https://www.idtechex.com/en/research-report/rfid-forecasts-players-and-opportunities-2023-2033/927.
83. https://cordis.europa.eu/project/id/720897. Accessed 7 Nov 2023
84. Välimäki MK, Sokka LI, Peltola HB, Ihme SS, Rokkonen TMJ, Kurkela TJ, Ollila JT, Korhonen AT, Hast JT. Printed and hybrid integrated electronics using bio-based andrecycled materials—increasing sustainability with greener materials andtechnologies. Int J Adv Manuf Technol. 2020;111:325–39. https://doi.org/10.1007/s00170-020-06029-8.
85. Sinha S, Modak NM. A systematic review in recycling/reusing/re-manufacturing supply chain research: a tertiary study. Int J Sustain Eng. 2021;14:1411–32. https://doi.org/10.1080/19397038.2021.1986594.

86. Zhuang Z, Yu B, Chao K-Y, Ho T-Y. Multi-package co-design for chiplet integration. In: Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design. New York: Association for Computing Machinery; 2022. p. 1–9.
87. Guo X, Xun Q, Li Z, Du S. Silicon carbide converters and MEMS devices for high-temperature power electronics: a critical review. Micromachines. 2019;10:406. https://doi.org/10.3390/mi10060406.
88. Wang Z. Microsystems using three-dimensional integration and TSV technologies: fundamentals and applications. Microelectron Eng. 2019;210:35–64. https://doi.org/10.1016/j.mee.2019.03.009.
89. Heuer C, Preuss J-A, Buttkewitz M, Scheper T, Segal E, Bahnemann J. A 3D-printed microfluidic gradient generator with integrated photonic silicon sensors for rapid antimicrobial susceptibility testing. Lab Chip. 2022;22:4950–61. https://doi.org/10.1039/D2LC00640E.
90. Xue J, Razdan S, Dobbelaere PD, Miele A, Prasad A, Wang T, Patel V, Chadha G. Trends and challenges in advanced packaging development for silicon photonics beyond 400Gbps in hyperscale data center networking applications. 2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM). IEEE Xplore, 2022; 148–150. https://doi.org/10.1109/EDTM53872.2022.9798331.
91. Lim H-R, Kim HS, Qazi R, Kwon Y-T, Jeong J-W, Yeo W-H. Advanced soft materials, sensor integrations, and applications of wearable flexible hybrid electronics in healthcare, energy, and environment. Adv Mater. 2020;32:1901924.
92. Andersson Ersman P, Lassnig R, Strandberg J, Tu D, Keshmiri V, Forchheimer R, Fabiano S, Gustafsson G, Berggren M. All-printed large-scale integrated circuits based on organic electrochemical transistors. Nat Commun. 2019;10:5053. https://doi.org/10.1038/s41467-019-13079-4.
93. Polyzoidis C, Rogdakis K, Veisakis G, Tsikritzis D, Hashemi P, Yang H, Sofer Z, Shaygan Nia A, Feng X, Kymakis E. Piezo-phototronic In2Se3 nanosheets as a material platform for printable electronics toward multifunctional sensing applications. Adv Mater Technol. 2023;8:2300203. https://doi.org/10.1002/admt.202300203.
94. Rogdakis K, Chatzimanolis K, Psaltakis G, Tzoganakis N, Tsikritzis D, Anthopoulos TD, Kymakis E. Mixed-halide perovskite memristors with gate-tunable functions operating at low-switching electric fields. Adv Electron Mater. 2023;9:2300424. https://doi.org/10.1002/aelm.202300424.
95. Jebali F, Majumdar A, Turck C, Harabi K-E, Faye M-C, Muhr E, Walder J-P, Bilousov O, Michaud A, Vianello E, Hirtzlin T, Andrieu F, Bocquet M, Collin S, Querlioz D, Portal J-M. Powering AI at the edge: a robust, memristor-based binarized neural network with near-memory computing and miniaturized solar cell. Nat Commun. 2024;15:741. https://doi.org/10.1038/s41467-024-44766-6.
96. Khan Y, Garg M, Gui Q, Schadt M, Gaikwad A, Han D, Yamamoto NAD, Hart P, Welte R, Wilson W, Czarnecki S, Poliks M, Jin Z, Ghose K, Egitto F, Turner J, Arias AC. Flexible hybrid electronics: direct interfacing of soft and hard electronics for wearable health monitoring. Adv Funct Mater. 2016;26:8764–75. https://doi.org/10.1002/adfm.201603763.
97. Ma Y, Zhang Y, Cai S, Han Z, Liu X, Wang F, Cao Y, Wang Z, Li H, Chen Y, Feng X. Flexible hybrid electronics for digital healthcare. Adv Mater. 2020;32:1902062. https://doi.org/10.1002/adma.201902062.
98. Gao Y, Yu L, Yeo JC, Lim CT. Flexible hybrid sensors for health monitoring: materials and mechanisms to render wearability. Adv Mater. 2020;32:1902133. https://doi.org/10.1002/adma.201902133.
99. Wang H, Zhang Y, Liang X, Zhang Y. Smart fibers and textiles for personal health management. ACS Nano. 2021;15:12497–508. https://doi.org/10.1021/acsnano.1c06230.
100. Shin W, Kim HJ. 3D in vitro morphogenesis of human intestinal epithelium in a gut-on-a-chip or a hybrid chip with a cell culture insert. Nat Protoc. 2022;17:910–39. https://doi.org/10.1038/s41596-021-00674-3.
101. Covi E, Lancaster S, Slesazeck S, Deshpande V, Mikolajick T, Dubourdieu C. Challenges and perspectives for energy-efficient brain-inspired edge computing applications (Invited Paper). In: 2022 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS), IEEE Xplore. 2022; 1–4. https://doi.org/10.1109/FLEPS53764.2022.9781597.
102. Braun T, Dreissigacker M, Wöhrmann M, Becker K-F, Schneider-Ramelow M. A novel hybrid method to integrate delicate MEMS components into a FOWLP. IMAPSource Proc. 2023;2022:000056–61. https://doi.org/10.4071/001c.74606.
103. Liu J-M, Lee TM, Wen C-H, Leu C-M. High-performance organic-inorganic hybrid plastic substrate for flexible displays and electronics. J Soc Inf Disp. 2011;19:63–9. https://doi.org/10.1889/JSID19.1.63.
104. Gao H, Bhat G, Ogras UY, Ozev S. Optimized Stress Testing for Flexible Hybrid Electronics Designs. In: 2019 IEEE 37th VLSI Test Symposium (VTS), Xplore. 2019; 1–6. https://doi.org/10.1109/VTS.2019.8758661.
105. Someya T, Bao Z, Malliaras GG. The rise of plastic bioelectronics. Nature. 2016;540:379–85. https://doi.org/10.1038/nature21004.
106. Kassanos P, Anastasova S, Chen CM, Yang G-Z. Sensor embodiment and flexible electronics. In: Yang G-Z, editor. Implantable sensors and systems: from theory to practice. Cham: Springer; 2018. p. 197–279.
107. Chen S, Qi J, Fan S, Qiao Z, Yeo JC, Lim CT. Flexible wearable sensors for cardiovascular health monitoring. Adv Healthc Mater. 2021;10:2100116. https://doi.org/10.1002/adhm.202100116.
108. Ozer E, Kufel J, Myers J, Biggs J, Brown G, Rana A, Sou A, Ramsdale C, White S. A hardwired machine learning processing engine fabricated with submicron metal-oxide thin-film transistors on a flexible substrate. Nat Electron. 2020;3:419–25. https://doi.org/10.1038/s41928-020-0437-5.
109. Basu S, Lazar D, Pothineni R. Design Techniques of High Speed PHY using Highly compact FOVEROS Through Silicon Via. In: 2022 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE Xplore, 2022; 2542–2546. https://doi.org/10.1109/ISCAS48785.2022.9937221.
110. Naffziger S, Beck N, Burd T, Lepak K, Loh GH, Subramony M, White S. Pioneering chiplet technology and design for the AMD EPYCTM and RyzenTM processor families: industrial product. Symp Int Comput Archit. 2021. https://doi.org/10.1109/ISCA52012.2021.00014.
111. Zhang Z. Analysis of the advantages of the M1 CPU and its impact on the future development of Apple. Int Conf Big Data Artif Intell Softw Eng. 2021. https://doi.org/10.1109/ICBASE53849.2021.00143.
112. Norrie T, Patil N, Yoon DH, Kurian G, Li S, Laudon J, Young C, Jouppi N, Patterson D. The design process for google's training chips: TPUv2 and TPUv3. IEEE Micro. 2021;41:56–63. https://doi.org/10.1109/MM.2021.3058217.
113. Shrestha R, Bajracharya R, Mishra A, Kim S. AI accelerators for cloud and server applications. In: Mishra A, Cha J, Park H, Kim S, editors. Artificial intelligence and hardware accelerators. Cham: Springer International Publishing; 2023. p. 95–125.
114. Elster AC, Haugdahl TA. Nvidia Hopper GPU and grace CPU highlights. Comput Sci Eng. 2022;24:95–100. https://doi.org/10.1109/MCSE.2022.3163817.

115. Zhou H, Lee T-W. Display that bend and stretch: Some smartphones can now fold like a wallet. In a few years, you may wear one on your skin. IEEE Spectr. 2020;57:24–9. https://doi.org/10.1109/MSPEC.2020.9262146.
116. McCann J. 14 - Preparation for smart clothing production. In: McCann J, Bryson D, editors. Smart clothes and wearable technology. 2nd ed. Sawston: Woodhead Publishing; 2023. p. 371–404.
117. Bairaktaris G, Borgne BL, Turkani V, Corrigan-Kavanagh E, Frohlich DM, Sporea RA. Augmented books: hybrid electronics bring paper to life. IEEE Pervasive Comput. 2022;21:88–95. https://doi.org/10.1109/MPRV.2022.3181440.
118. Ammann KR, Ahamed T, Sweedo AL, Ghaffari R, Weiner YE, Slepian RC, Jo H, Slepian MJ. Human motion component and envelope characterization via wireless wearable sensors. BMC Biomed Eng. 2020;2:3. https://doi.org/10.1186/s42490-020-0038-4.
119. Oldroyd P, Malliaras GG. Achieving long-term stability of thin-film electrodes for neurostimulation. Acta Biomater. 2022;139:65–81. https://doi.org/10.1016/j.actbio.2021.05.004.
120. Khodagholy D, Gelinas JN, Thesen T, Doyle W, Devinsky O, Malliaras GG, Buzsáki G. NeuroGrid: recording action potentials from the surface of the brain. Nat Neurosci. 2015;18:310–5. https://doi.org/10.1038/nn.3905.
121. Woodington BJ, Curto VF, Yu YL, Martínez-Domínguez H, Coles L, Malliaras GG, Proctor CM, Barone DG. Electronics with shape actuation for minimally invasive spinal cord stimulation. Sci Adv. 2021;7:eabg7833. https://doi.org/10.1126/sciadv.abg7833.
122. Choi HW, Shin D-W, Yang J, Lee S, Figueiredo C, Sinopoli S, Ullrich K, Jovančić P, Marrani A, Momentè R, Gomes J, Branquinho R, Emanuele U, Lee H, Bang SY, Jung S-M, Han SD, Zhan S, Harden-Chaters W, Suh Y-H, Fan X-B, Lee TH, Chowdhury M, Choi Y, Nicotera S, Torchia A, Moncunill FM, Candel VG, Durães N, Chang K, Cho S, Kim C-H, Lucassen M, Nejim A, Jiménez D, Springer M, Lee Y-W, Cha S, Sohn JI, Igreja R, Song K, Barquinha P, Martins R, Amaratunga GAJ, Occhipinti LG, Chhowalla M, Kim JM. Smart textile lighting/display system with multifunctional fibre devices for large scale smart home and IoT applications. Nat Commun. 2022;13:814. https://doi.org/10.1038/s41467-022-28459-6.
123. Chung S, Lee T. Towards flexible CMOS circuits. Nat Nanotechnol. 2020;15:11–2. https://doi.org/10.1038/s41565-019-0596-6.
124. Takeda Y, Hayasaka K, Shiwaku R, Yokosawa K, Shiba T, Mamada M, Kumaki D, Fukuda K, Tokito S. Fabrication of ultra-thin printed organic TFT CMOS logic circuits optimized for low-voltage wearable sensor applications. Sci Rep. 2016;6:25714. https://doi.org/10.1038/srep25714.
125. Han SH, Shin JH, Choi SS. Analytical investigation of multi-layered rollable displays considering nonlinear elastic adhesive interfaces. Sci Rep. 2023;13:5697. https://doi.org/10.1038/s41598-023-31936-7.
126. Baumbauer CL, Anderson MG, Ting J, Sreekumar A, Rabaey JM, Arias AC, Thielens A. Printed, flexible, compact UHF-RFID sensor tags enabled by hybrid electronics. Sci Rep. 2020;10:16543. https://doi.org/10.1038/s41598-020-73471-9.
127. Kim MY, Lee KH. Electrochemical sensors for sustainable precision agriculture—a review. Front Chem. 2022;10:848320. https://doi.org/10.3389/fchem.2022.848320.
128. Zhang J, Kim K, Kim HJ, Meyer D, Park W, Lee SA, Dai Y, Kim B, Moon H, Shah JV, Harris KE, Collar B, Liu K, Irazoqui P, Lee H, Park SA, Kollbaum PS, Boudouris BW, Lee CH. Smart soft contact lenses for continuous 24-hour monitoring of intraocular pressure in glaucoma care. Nat Commun. 2022;13:5518. https://doi.org/10.1038/s41467-022-33254-4.
129. European Chips Act. https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en. Accessed 30 Jun 2023.
130. Semiconductors: MEPs ready to start talks on new law to boost EU chips industry. News. European Parliament. 2023. https://www.europarl.europa.eu/news/en/press-room/20230210IPR74801/semiconductors-meps-ready-to-start-talks-on-new-law-to-boost-eu-chips-industry. Accessed 30 Jun 2023.
131. Flexible Hybrid Electronics. In: Fraunhofer Inst. Electron. Microsyst. Solid State Technol. EMFT. https://www.emft.fraunhofer.de/en/research-development/microtechnologies-nanotechnologies/flexible-hybrid-electronics.html. Accessed 10 Jul 2023.
132. Flexible Hybrid Electronics (FHE). 3D systems packaging research center. https://sites.gatech.edu/ien-prc/flexible-hybrid-electronics-fhe/. Accessed 10 Jul 2023.
133. Hybrid printed electronics. TNO. https://www.tno.nl/en/healthy/flexibele-en-vrije-vorm-producten/hybrid-printed-electronics/. Accessed 10 Jul 2023.

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