A Low Noise Offset Cancellation Method for Improving Sensitivity of CMOS Hall Sensor

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Received: 30 April 2018 / Revised: 7 September 2018 / Accepted: 15 November 2018 / Published online: 3 January 2019
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Abstract

A low-noise offset-cancellation method is proposed to increase the sensitivity of CMOS Hall sensors. Conventional CMOS Hall sensors have low sensitivity because of high offset, flicker ($1/f$) noise, and chopper switching noise. To improve the sensitivity of Hall sensors, we need to reduce the noise generation and separate the Hall signal from the noise. Therefore, in this study, switching noise and harmonics are reduced by applying a low-noise offset-cancellation method using a reduced number of choppers. In addition, because the Hall signal does transform back to DC, it is not affected by the offset noise of the read-out circuits. A Hall sensor system that includes a CMOS Hall plate is designed and tested. When the Hall signal processed by the proposed method is compared with the existing system under the same conditions, we confirm that the signal-to-noise ratio (SNR) improves by 18.36 dB and the spurious free dynamic range (SFDR) improves by 9.02 dB.

Keywords CMOS Hall sensor · Chopper stabilization technique · Magnetic sensor · Offset cancellation · Spinning current technique

1 Introduction

Recently, as technology development and demand for future vehicles such as electric cars and autonomous vehicles have increased, the utilization of Hall sensors has also significantly increased. In addition, Hall sensors are extensively used in the medical, white-goods, aerospace, and defense fields [1]. Because the application fields of Hall sensors are diverse, various research works on the geometry, materials, noise elimination, and driving circuits have been carried out to improve the accuracy of Hall sensors [2–6].

To manufacture Hall sensors at low cost and high integration for mass production, they must be fabricated using the CMOS process. Thus, in recent years, market applications for proximity switching, positioning, speed detection, and current sensing have emerged that use integrated Hall

sensors fabricated using low-cost CMOS technologies [5]. However, Hall sensors manufactured by using the CMOS process are not evenly doped. Therefore, the offset is larger than that of the other processes, and the flicker ($1/f$) noise is also large. In addition, because the Hall plate manufactured using the CMOS process outputs a low Hall voltage of several tens of millivolts, the noise may be sufficiently large to cover the Hall voltage. Because of low sensitivity and high noise, the minimum value of the magnetic field that can be measured, as well as the accuracy of the measurement, is limited [6]. Figure 1 shows the most commonly used Hall sensor noise-cancellation technique and the Hall voltage in the frequency domain. The conventional Hall sensor consists of a Hall plate, a spinning-current circuit, more than one pair of choppers, amplifier, and a low-pass filter (LPF). When a magnetic field is applied to the Hall plate and an output voltage is generated, the direction of the bias current switches between the spinning-current circuit and the chopper. Because the polarity of the offset changes according to the direction of the bias current, the Hall voltage shifts to the spinning-current frequency, and the offset and flicker noise shift to the low-frequency band. Thereafter, the amplifier sufficiently amplifies the low Hall signal. After passing through the chopper, the Hall voltage shifts to the low-frequency band, the noise component shifts to f_{sp} , and the noise

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Fig. 1 Noise-cancellation technique of the conventional Hall sensor

is removed by the LPF. This method requires at least five system blocks and a higher order LPF, thereby increasing the size and complexity of the system. In addition, the Hall voltage is affected by the offset and flicker noise generated after transforming the Hall voltage to DC. Often, several pairs of choppers are used to completely separate the Hall voltage from the offset and flicker noise. However, in this case, because the chopper includes many switches, according to [7], a switching circuit designed to remove noise may cause switching noise and harmonic that affect the Hall voltage.

Therefore, the present paper proposes a novel low-noise offset-cancellation method with a simpler structure than the existing Hall sensors and has superior noise-canceling performance. In Sect. 2, the proposed low-noise offset-cancellation method is described in detail, and we explain the design of the low-noise offset-cancellation circuit in Sect. 3. In Sect. 4, we present the construction of the measurement environment to verify and analyze the performance test results of the proposed method.

2 Proposed Low-Noise Offset-Cancellation Method

To overcome the limitations of the noise-reduction technology of the existing CMOS Hall sensor, a low-noise offset-cancellation method is proposed. Figure 2 shows the block diagram of the proposed method and the Hall signals in the frequency domain. This system consists of a Hall plate, a spinning-current circuit, one chopper, BPF, and an amplifier. Similar to the existing system, the direction of the bias current is switched by the spinning-current circuit and the chopper to separate the Hall voltage into f_{sp} and the offset and

flicker noise into the low-frequency band. Then, the noise is removed by the BPF, and the amplifier sufficiently amplifies the Hall voltage. This method uses only one chopper; thus, the switching noise and harmonics can be reduced. Further, because the Hall voltage does not transform back to the DC band, it is not affected by the offset noise of the read-out circuit generated after the offset of the Hall plate is removed.

3 Design of the Offset-Cancellation Circuit of the CMOS Hall Sensor System

The Hall sensor system proposed in this paper consists of a Hall plate, spinning-current circuit chopper, BPF, and amplifier. The design and simulation of each block are described.

3.1 Cross-Shaped Horizontal Hall Plate

To manufacture Hall sensors at low cost and high integration for mass production, fabricating them using the CMOS process is preferable. In this work, we fabricate and test a CMOS Hall plate using the Tower Jazz BCD 180 nm process. The plate is made of a cross-shaped vertical Hall plate, among the various geometries, which is easy to manufacture and has a relatively large Hall voltage. The N-well is weakly doped into the active area of a p-substrate in a cross-shaped Hall plate, and the four terminals are highly doped with N+ to reduce the terminal resistance. The larger the width (W) of the Hall plate is, the better is the flicker noise. The larger the length (L) is, the better is the sensitivity [8]. However, because the size cannot be indefinitely increased, W is set to 100 μm and L is set to 12 μm to obtain high sensitivity within a limited area. The geometry of the Hall plate

Fig. 2 Proposed experimental environment **Fig. 3** Hall plate fabricated using the CMOS technology

is shown in Fig. 3. The measured Hall voltage according to the magnetic field is shown in Fig. 4. As the magnetic field generated by the Helmholtz coil increases, the Hall voltage linearly increases, and the sensitivity of the manufactured Hall plate is 77 mV/T.

3.2 Spinning-Current Circuit and Chopper

The spinning-current circuit and chopper are constructed as shown in Fig. 5. When CLK is high, M1 and M4 are turned on, current flows from C1 to C2 in the Hall plate, and a Hall signal is output to C3 and C4. Conversely, when CLK is low, M2 and M3 are turned on, current flows from C4 to C3 in the Hall plate, and a Hall signal is

Fig. 4 Graph of the Hall voltage according to the magnetic field

Fig. 5 Spinning-current circuit and chopper

output to C1 and C2. The offset and Hall voltage according to CLK in the time domain are shown on the right side of Fig. 5. In the frequency domain, the Hall voltage is separated into f_{sp} , and the offset and flicker noise separate into the low-frequency band. In the proposed system, the bias current is set to 5 mA, and f_{sp} is set to 100 kHz.

3.3 BPF and Amplifier

The BPF is designed as shown in Fig. 6 to remove noise from the Hall signal. A fifth-order Chebyshev filter with a center frequency of 100 kHz and a 3-dB bandwidth of 40 kHz is designed. In addition, the amplifier uses ADA4528 with an ultra-low offset of 2.5 μ V and is designed to have a gain of 32 dB to sufficiently amplify the Hall signal.

3.4 Verifications

Figure 7 shows the test board of the Hall sensor system using the proposed noise-canceling technique. The Hall plate is designed with a protruding shape to be installed at the center of the Helmholtz coil. A spinning-current circuit and a chopper are installed to allow current to flow into the Hall plate and to separate the Hall voltage from the flicker noise and offset. The circuit also includes a fifth-order Chebyshev BPF designed with passive elements and an amplifier with a 32-dB gain. Figure 8 shows the experimental environment. The clock generator provides the clock for the spinning current, and the power supply applies power to all the devices for the Hall sensor system experiment. The Helmholtz coil generates a uniform magnetic field among the coils [9].

The Helmholtz coil generates a constant magnetic field of 26 mT, and the chopper output is measured. Figure 9 shows the measurement results in the frequency domain. Because the signal passes through the spinning current and chopper,

Fig. 6 Fifth-order Chebyshev BPF

Fig. 7 Test board of the proposed Hall sensor system **Fig. 8** Experimental environment

flicker noise and offset occur under the following conditions: DC, Hall voltage of 100 kHz, and harmonics of 200 kHz.

Next, the BPF output is measured and shown in Fig. 10. Because the center frequency of the BPF is 100 kHz, the offset flicker noise located at DC and the harmonics located at 200 kHz are filtered.

Finally, the amplifier output and the output of the proposed Hall sensor system are measured and shown in Fig. 11. The Hall voltage at 100 kHz is amplified by 30.61 dB from 56.58 to 25.97 dBV.

Table 1 lists the summary of the output of the Hall sensor system using the proposed low-noise offset-cancellation method under a magnetic field of 26 mT. From the proposed

method, we can observe that the Hall signal and the offset increase and the flicker noise and harmonic components decrease. The total sensitivity of the proposed Hall sensor system is 1925 mV/T.

The read-out circuits of the conventional (Fig. 1) and proposed (Fig. 2) Hall sensors are designed with the same Hall plate. The Hall signals are also compared under the same conditions of a bias current of 5 mA and spinning frequency of 100 kHz. Figure 12 shows that the signal-to-noise ratio (SNR) improves by 18.36 dB. The spurious free dynamic range (SFDR) is defined as the difference between the largest noise and Hall voltage. We confirm that it is 9.02 dB higher than that of the conventional Hall sensor. The proposed Hall

Fig. 9 Output voltage after passing through the spinning-current circuit and chopper

Fig. 11 Output voltage after passing through the amplifier

Fig. 10 Output voltage after passing through the BPF

sensor is simplified by removing one chopper compared with the conventional Hall sensor, and the Hall voltage does not transform back to the DC band. Therefore, performance can be improved because of the lesser influence on the offset, flicker noise, switching noise, and harmonics.

4 Conclusion

This paper has proposed a low-noise offset-cancellation method to increase the sensitivity of Hall sensors. Because the CMOS Hall sensor process has higher noise and lower Hall voltage than the other processes, it can reduce the switching noise and harmonic components by applying the

Table 1 Measurement results of proposed Hall sensor system

Frequency	Spinning-current circuit and chopper (dBV)	BPF (dBV)	Amplifier (dBV)
DC	− 28.07	− 98.15	− 76.59
100 kHz	− 53.93	− 56.58	− 25.97
200 kHz	− 41.9	− 80.9	− 58.62

Fig. 12 Comparison of the SNR of the conventional and proposed Hall sensors

proposed low-noise offset-cancellation circuit that reduces the number of choppers. In addition, because the Hall signal does not transform back to the DC band, it is not affected by the offset noise of the read-out circuit. Table 2 lists the specifications of the proposed Hall sensor system.

Table 2 Specification of the proposed Hall sensor system

Hall plate	
Process	Tower Jazz BCD 180 nm
Size	W = 100 μm L = 12 μm
Sensitivity	77 mV/T
Magnetic field in the experiment	26 mT
Spinning-current circuit and chopper	
Bias current	5 mA
Spinning frequency	100 kHz
BPF	
Center frequency	100 kHz
3-dB bandwidth	40 kHz
Amplifier	
Gain	32 dB
Whole system	
Sensitivity	1925 mV/T

In this work, only the Hall plate is implemented in the CMOS process to verify the proposed method. Future validation of fully integrated CMOS Hall sensors, including ADC and digital signal processing, is needed. Furthermore, if additional research is conducted for high-voltage application, we expect that it can be applied to various applications that require high Hall sensor sensitivity, such as in the automotive, medical, and other fields.

Acknowledgements This work was supported by the BK21 plus program through the National Research Foundation (NRF) funded by the Ministry of Education of Korea.

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