Research

Investigation of graded channel effect on analog/linearity parameter analysis of junctionless surrounded gate graded channel MOSFET

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Abstract
Linearity analysis of nanoscale devices is a vital issue as nonlinearity behavior is exhibited by them when employed in circuits for microwave and RF applications. In this work, a junctionless surrounded gate-graded channel MOSFET (JLSGGC MOSFET) is investigated thoroughly to analyze its linearity performance with the help of ATLAS tool of technology computer-aided design. The proposed device is compared systematically with the conventional junstionless surrounded gate MOSFET(JLSG MOSFET) to investigate their linearity. To evaluate the linearity, the figure of merits such as higher-order transconductance (G_{m1}, G_{m2}), intercept points(VIP_2, VIP_3, IIP_3), IMD_3 and 1 dB—compression point(P1 dB) are considered. The linearity of our proposed device improves by 35.5% in view of the compression point in comparison to JLSG MOSFET before the threshold voltage region of operation. The simulation results reveal a substantial enhancement in the linearity performance of the JLSGGC MOSFET. The improved linearity behavior of JLSGGC MOSFET makes it suitable for wireless RF and system-on-chip applications.Analog/RF performance is studied in terms of intrinsic gain (G_m/G_{ds}), cut-off frequency (f_T),maximum frequency of oscillation (f_{max}).Improved analog/RF performances of JLSGGC MOSFET suggests its applications in high frequency operating range.

Article Highlights

- Linearity is an important issue that need to be resolved before employing the nano MOSFETs for high frequency radio applications.It is assessed through certain key factors which determine the level of distortion present in the said device. The key factor quantifies what should be the maximum input with in which the device should operate without reducing its gain by 1 decibel unit
- The impact of graded channel architechure on the linearity of the proposed device is explored by comparing the key performance factors between graded and ungraded structures of junctionless surrounded gate MOSFETs
- Systematic Comparison of gain , unity current gain frequency(f_T) ,unity power gain frequency (f_{max}) are performed to find the suitability for anlog/RF applications of the JLSGGC MOSFET.

Keywords Higher order transconductance (G_{m1},G_{m2}) · VIP_2,VIP_3 · IIP_3 · IMD_3,P1dB,intrinsic gain,f_T · f_{max}

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1 Introduction

The downscaled nano MOSFETs find their suitability for wireless and microwave applications. Short channel effects (SCE_s) are the major hindrances in the path of further downscaling. Advanced MOS devices are proposed in the literature that minimizes SCEs up to a certain extent but still can't be neglected. SOI $MOSFET_s$ [1], multi-gate $MOSFET_s$ [2], nanowires [3], and nanotube $MOSFET_s$ [4] are investigated to reduce SCEs and these structures are proved to be potential candidates for VLSI applications. SiGe Double gate MOSFET TFET with low doped drain region enhances the scaling capabilities and exhibits reduced susceptibility in comparison to conventional Si DG MOSFET [5]. The neural network-based hybrid approach is proposed to model graphene nanoribbon field-effect transistors (GNRFETs) which relaxes the computational burden substantially [6]. The requirement of steep S/D junction and parasitic resistance set obstacles in further downscaling which are overcome with the introduction of Junctionless MOSFETs [7, 8]. JL MOSFET is a uniformly doped gated resistor with a doping concentration of $1 \times 10^{19}\ cm^{-3}$ or more than that. The advantageous features of junctionless devices, such as easy fabrication, channel homogeneity, and improved electrical characteristics, make them a promising option for enhancing the immunity performances of nano-scaled CMOS-based devices [9]. Device reliability and performance optimizations are two major concerns for the designing of advanced nano-scaled MOSFETs. The reduction in DIBL is more prominent due to the presence of a hot carrier in DG MOSFET as the channel length enters into the nanometer regime [10]. The immunity of JL DG MOSFET against hot carrier degradation is better than DG MOSFET [11]. By leveraging the benefits of junctionless DG MOSFETs, nanoelectronics digital applications can benefit from improved device immunity and reliability [11]. The mole fraction of Ge is explored in $Si_{1-x}G_x$/Ge/Si heterojunction (HJ) DG JL TFET to bring an improvement in sub-threshold characteristics and reduction in ambipolar conduction [12]. The investigation of the drain and source extension design in gate-all-around junctionless MOSFETs offers valuable insights into their electrical behavior for high-performance RF and analog applications [13]. The use of higher doping concentration in JL MOSFET results in mobility degradation and reduction of transconductance [14]. Lowering of transconductance restricts the use of JL MOSFET in analog/RF applications due to a reduction in cut-off frequency in comparison to traditional $MOSFET_s$ [15, 16]. As a matter of solution to improve RF performance, asymmetrical channel engineering has been proposed in past literature [17, 18]. The nanoscale graded channel gate stack double-gate (GCGS DG) MOSFET structure offers a promising solution for suppressing short-channel effects and improving subthreshold performance in MOSFETs for nanoelectronics applications [17]. The multi-objective optimization approach yields optimal subthreshold parameters for GCGSDG MOSFETs [18]. By iteratively evaluating and adjusting the subthreshold parameters using the genetic algorithm, significant improvements in threshold voltage, DIBL, subthreshold swing, and OFF-current are achieved [18]. Leakage current is reduced by the confinement of the electric field using gate engineering in the surrounding gate structure [19].To the best of our knowledge, improvement in analog and RF characteristics of DG JL MOSFET is put forward by Chen et al., implement asymmetric channel doping or nonuniform channel doping profile [20]. The results reveal the supremacy of graded channel DG JL MOSFET over traditional double gate JL MOSFET. Combining the advantage of surrounded gate architecture from gate engineering and graded channel architecture from channel engineering, here we put forward the proposal junctionless surrounded gate graded channel MOSFET (JLSGGC MOSFET).

Transistors have inherent nonlinearity within themselves. Nonlinearity in power amplifiers, continuous time alias filters, and LNAs leads to system performance degradation. The radio frequency performance of a system under investigation depends upon its linearity which in turn minimizes the inter-modulation terms and higher-order harmonics [21]. A higher level of linearity can be achieved in RF systems by designing sophisticated circuits which in turn reduces the nonlinearity from MOS devices up to a certain extent. However, linearization at the circuit level requires a larger IC area, more power consumption, and becomes costly. Linearity improvement is more appropriate at the device- level rather than at the system level as complex hardware circuitry is needed in system-level linearization [22, 23]. Hence linearity needs to be analysed precisely and comprehensively using physics-based device simulators. Many reports are available in the literature, focussing on the analog/RF analysis of graded channel (asymmetric channel) MOSFETs [24–26]. Linearity has not got much attention for surrounded gate JL MOSFET with asymmetric or graded channel architecture which is a potential candidate for VLSI applications and there still lies a gap. In this paper, we have investigated the linearity performance of surrounded gate junctionless MOSFET with graded channel architecture. Linearity performance is studied on a comparison basis with respect to the figure of merits (FOMs)such as higher-order transconductance (G_{m2}, G_{m3}), second and third-order intercept point (VIP_2 and VIP_3), third-order intermodal dispersion (IMD_3), 1dBcompression point.

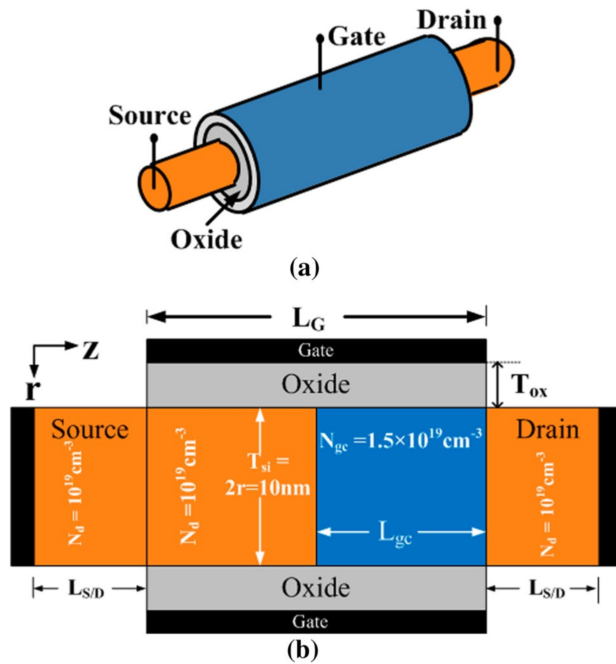


Fig. 1 **a** A 3-D view of JLSGGC MOSFET. **b**: A 2-Dimensional view of JLSGGC MOSFET

.The organization of the paper is mentioned as: Sect. 1 represents the reports from the literature concerning the state of the art. Section 2 describes the structural parameters of the device and the physical model used during simulation along with the model validation. Sections 3 and 4 illustrate the simulated results for linearity analysis between JLSGGC MOSFET and the conventional SGJL MOSFET. Finally, conclusion is drawn in Sect. 5.

2 Device structure and simulation setup

The conventional junctionless surrounded gate MOSFET is uniformly doped having an impurity concentration of 10^{19} cm^{-3}. The doping concentration of JLSGGC MOSFET is the same as that of JLSG MOSFET. The channel of JLSGGC MOSFET is graded laterally along the direction of z. The device parameters and supply sources are selected for simulation according to ITRS [27]. Figures 1a and b depict the views of JLSGGC MOSFET in 3D and 2D. In the proposed device grading is done exactly in half the channel. The length of the channel(L_G) is twice that of the graded channel length(L_{gc}). The radius (r) of the JLSGGC MOSFET is kept at 5 nm, hence the width (T_{si}) is 10 nm. The length of Source/Drain extension ($L_{S/D}$) and channel (L_G) are kept at 20 nm and 30 nm respectively while performing the simulation.

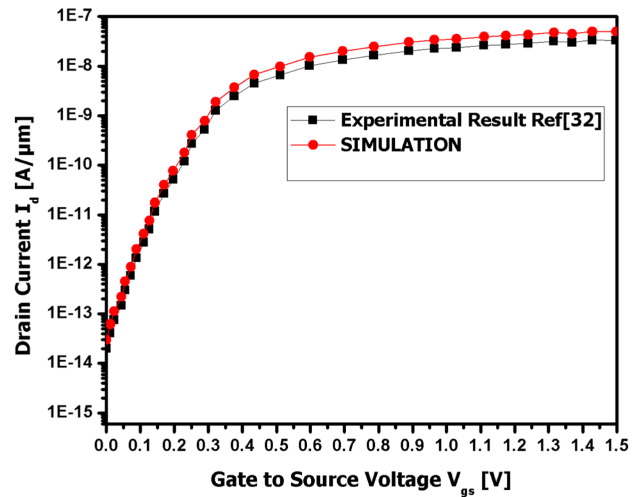


Fig. 2 Model validation used in simulation by calibrating the simulated result against experimental output V_{DS} = 0.05 Volt

In the proposed device the channel is graded exactly at half of its length. The channel length(L_G) is twice that of the graded channel length(L_{gc}). The radius (r) and width (T_{si}) of the nanowire JLGC MOSFET are kept at 5 nm and 10 nm respectively. Half of the region of the channel towards the source end of nanowire JLSGGC MOSFET is doped with 1×10^{19} cm^{-3} (N_d) and the rest of the channel towards the drain end is doped with 1.5×10^{19} cm^{-3} (N_{gc}). In the present work, simulation is carried out with ATLAS TCAD SILVACO three-dimensional device simulator [28]. Drift Diffusion and Boltzmann models are included during the simulation to consider the carrier transportation inside the semiconductor. Lombardi CVT model and FLDMOB models are used to consider carrier mobility. The Shockley Read Hall (SRH) physical model considers carrier lifetime before recombination during simulation. In nanoscaled devices, quantum effects become significant due to the reduced size and confinement of charge carriers, leading to unique quantum phenomena and properties. Moreover, when layer thickness approaches 7 nm or less, the de Broglie wavelength of the layer approaches that of a thermalized electron, and conventional energy–momentum relations for bulk semiconductors are no longer operational [29, 30]. Similarly, ballistic transport refers to the motion of charge carriers, such as electrons, through a material without experiencing scattering or collisions. In this transport, carriers travel freely, following classical physics principles, and their trajectories are not influenced by impurities, defects, or lattice vibrations. Ballistic transport is typically observed in ultra-small devices, where the device dimensions are comparable to the mean free path of the charge carriers [31]. The channel length and thickness of the present device are 30 nm and 10 nm respectively. The quantum

Table 1 Dimensions of the design parameters of JLSGGC and JLSG mosfets

Parameters	JLSG MOSFET	JLSGGC MOSFET
Channel length (L_G)	30 nm	30 nm
Radius of the cylindrical body (r)	5 nm	5 nm
Diameter/thickness of the cylindrical body (T_{si})	10 nm	10 nm
Source/ Drain region Doping concentration	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Channel region doping Concentration of channel	1×10^{19} cm^{-3}	1×10^{19} cm^{-3} for 15 nm from source side
Graded channel length (L_{gc})	Channel is not graded	15 nm from the grading position of the channel
Graded channel doping concentration (N_{gc})	Channel is not graded	1.5×10^{9} cm^{-3} for 15 nm towards drain side
Oxide layer Thickness (T_{OX})	1 nm	1 nm
Work function of polysilicon metal (ϕ_m)	5.0 Ev	5.0 eV

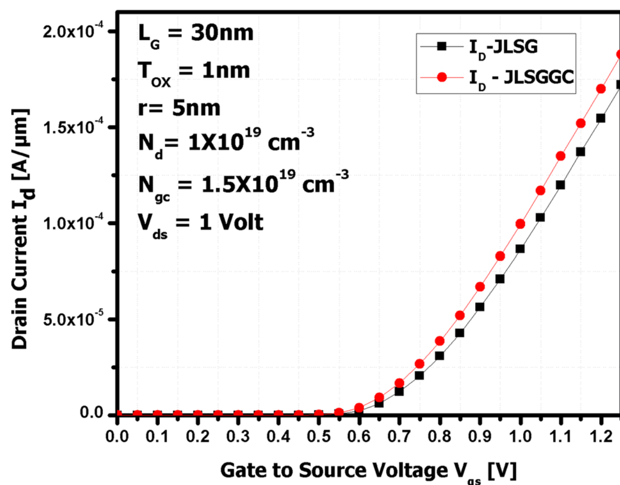


Fig. 3 A plot of I_d V_s V_{gs} for JLSGGC and JLSG MOSFET$_s$ at workfunction (ϕ_{m}), diameter(Tsi) and graded channel length (L_{gc}) is 5.0 eV, 10 nm, 15 nm respectively

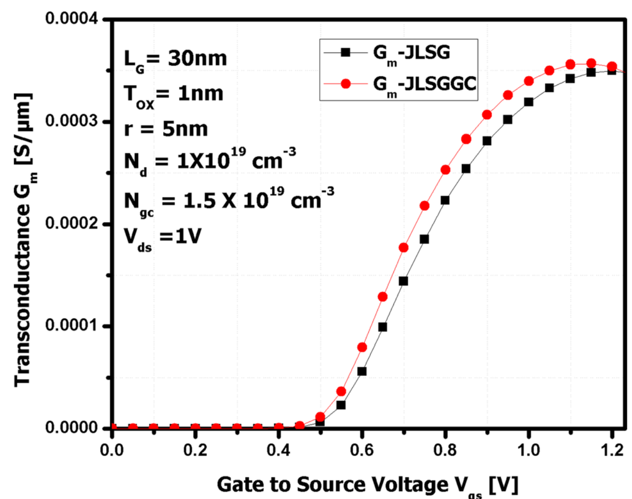


Fig. 4 A Plot of transconductance (G_m) Vs V_{gs} for JLSGGC and JLSG MOSFETs at workfunction (ϕ_{m}), diameter(Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

and ballistic phenomenon come into play if the channel length and body thickness reduce below 20 nm and 7 nm respectively. The present model doesn't include the quantum as well as ballistic transport mechanisms as (i) The size of the devices is more than de-Broglie wavelengths which leads to the beyond the realm of quantum effects [30]. (ii) The computed value of the mean free path ($\lambda = \frac{1}{\pi d^2 N}$) (where d is diameter and N is concentration) is not comparable to the dimensions of the proposed device, which causes the exclusion of the ballistic transport mechanism [31]. Complete depletion of the charge carrier during the off state of such a heavily doped device is ensured by using polysilicon as the gate metal having work function 5.0 eV. Differential equations are solved using the Gummel-Newton numerical method. The chosen models are validated by calibrating the simulated results against the experimental results of n-type junctionless nanowires [32]. The body thickness and channel length of the device are kept at 30 nm and 1 µm respectively which are the same as the experimental data. The simulation is done at $V_{DS}=0.05$ V. Figure 2 illustrates good agreement between the results obtained from simulation and experiment. Hence the chosen models are validated.

The design parameters of JLSGGC MOSFET are summarized in Table 1.

3 Transfer characteristics

The drain current for graded channel and ungraded channel MOSFETs are compared with respect to V_{gs} and illustrated in Fig. 3.

The charge carriers of both devices face different electric fields due to which there is a faster increase in the center potential of JLSGGC MOSFET than the traditional one [33]. A discontinuous electric field is marked

in JLSGGC MOSFET having two peaks [33]. But junctionless surrounded gate MOSFET has one electric field peak. The additional electric field peak, created at the grading channel position, leads to the electric field diminution towards the drain. The reduced electric field accelerates the electrons while crossing the conducting channel. This improved transportation of electrons enhances the drain current in JLSGGC MOSFET.

Transconductance (G_m) is a major factor in considering linearity in the case of MOSFETs. Transconductance (G_m) represents the variation in drain current as per the change in V_{gs}. Figure 4 illustrates G_m as a function of V_{gs} for both of the devices.

The existence of an additional electric field peak due to channel grading redistributes the electric field at the drain. This is the cause of improved G_m in the proposed device.

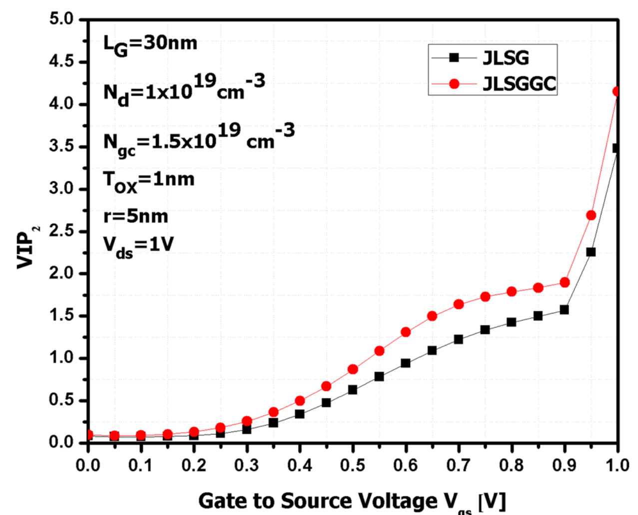


Fig. 6 A Plot of VIP_2 Vs V_{gs} for JLSGGC and JLSG MOSFETs at workfunction (ϕ_{m}), diameter(Tsi) and graded channel length (L_{gc}) is 5.0 eV, 10 nm, 15 nm respectively

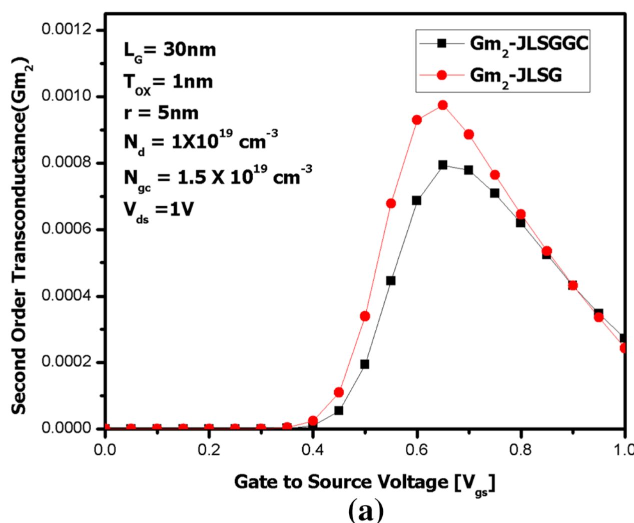
4 Linearity analysis

In this section, a systematic comparison is made between the linearity performance of JLSGGC MOSFET and JLSG MOSFET with the performance indices like second and third-order incept points(VIP_2, VIP_3), intermodal dispersion (IMD_3), input intercept point (IIP_3), 1-dB compression point(P1-dB). Linearity has a direct and inverse relationship with first and higher-order transconductances [34]. A MOSFET is a nonlinear time-variant system that modulates the AC input i,e (V_{gs}) and thereby produces the current I_D. I_D can be represented as a Taylor series expansion and the coefficients of this expansion are given by [35]:

$$I_d = I_0 + G_{m1}V_{gs} + G_{m2}V_{gs}^2 + G_{m3}V_{gs}^3 + \cdots \tag{1}$$

$$G_{m1} = \frac{\delta I_d}{\delta V_{gs}},\ G_{m2} = \frac{\delta^2 I_d}{\delta V_{gs}^2},\ G_{m3} = \frac{\delta^3 I_d}{\delta V_{gs}^3} \tag{2}$$

The 2nd and 3rd order transconductance terms cause nonlinearity in the device. The variable intercept points are interpreted as the extrapolated gate voltage amplitude at which the harmonics of the 2nd and 3rd order will be the same as the fundamental tone in drain current I_D. The values of intercept points should be high to obtain higher



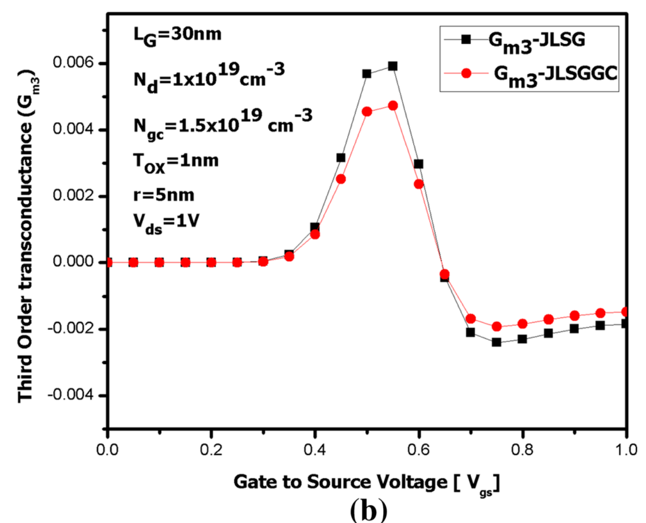


Fig. 5 **a** An illustration of G_{m2} Vs V_{gs} with T_{si} = 10 nm, L_{gc} = 15 nm. **b** An illustration of G_{m3} Vs V_{gs} with T_{si} = 10 nm, L_{gc} = 15 nm

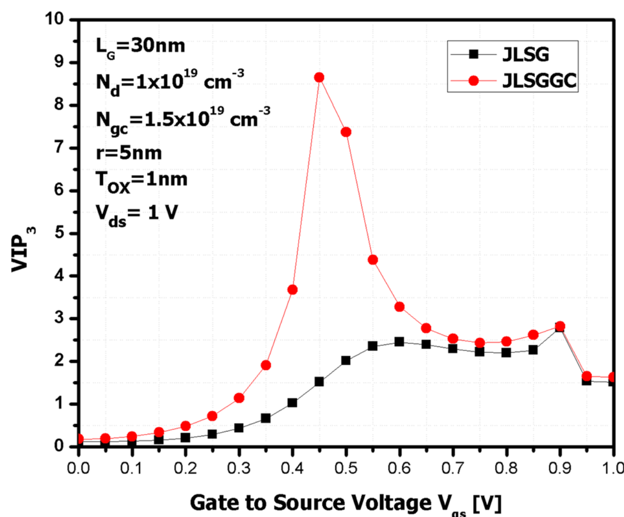


Fig. 7 A plot of third order variable intercept point (VIP_3) Vs V_{gs} for JLSGGC and JLSG MOSFETs at $L_{gc}=15$ nm, work function ($\phi_{m)}=5.0$ eV

linearity and lower distortion. The variable intercept points are formulated as: [36]

$$VIP_2 = \left[4 \times \left(\frac{G_{m1}}{G_{m2}}\right)\right]_{V_{ds}=\text{Constant}} \quad (3)$$

$$VIP_3 = \left[\sqrt{24 \times \left(\frac{G_{m1}}{G_{m3}}\right)}\right]_{V_{ds}=\text{Constant}} \quad (4)$$

The peaks of G_{m2} and G_{m3} for both of the devices are obtained at lower voltages of V_{gs} as demonstrated by Fig. 5a and b. This result shows the utilization of the devices in the circuits operated in moderately inverted regions. Both (a) and (b) of Fig. 5 clarify that JLSGGC MOSFET possesses more linearity in terms of suppressing higher-order inter-modulation terms by achieving lower peaks of G_{m2} and G_{m3}.

It is evident from Figs. 6 and 7 that JLSGGC MOSFET attains higher peaks of VIP_2 and VIP_3 as compared to JLSG MOSFET. The reason for this is the discontinuous electric field that redistributes itself towards the drain side and carriers transport more efficiently.

The distortion due to inter-modulation terms in the output of the RF stage is measured by third-order inter-modulation term i.e. IMD_3. To achieve linearity in the proposed MOSFET, the IMD_3 should be minimal. The expression for IMD_3 is as follows [37]

$$IMD_3 = R_S \times \left\{4.5 \times \left(VIP_3\right)^3 \times G_{m3}\right\}^2 \quad (5)$$

Usually, Rs is 50 Ω for radio frequency applications.. As depicted in Fig. 7 JLSGGC MOSFET is said to have a value of IMD3 ranging from −79 dBm to 0dBm whereas JLSG MOSFET posses IMD3 ranging from −93 dBm to 0dBm from VGS = 0.0 V to VGS = 0.4. The more negative the value of IMD3, the more will be the distortion because distortion is regarded as a loss. Hence JLSGGC MOSFET shows less distortion in comparison to JLSG MOSFET suggesting improved linearity. But from VGS = 0.4 V to VGS = 0.7, JLSGGC MOSFET attains a higher value of IMD3 as compared to JLSG MOSFET

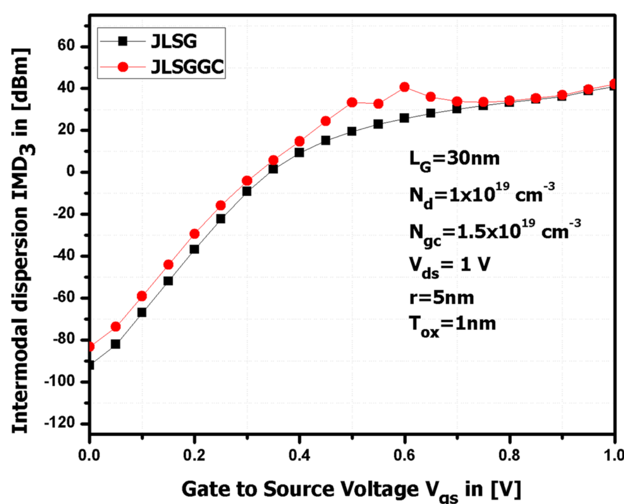


Fig. 8 Plot of IMD_3 Vs V_{gs} for JLSGGC and JLSG MOSFETs at workfunction ($\phi_{m)}$, diameter(Tsi) and graded channel length (L_{gc}) is 5.0 eV, 10 nm, 15 nm respectively

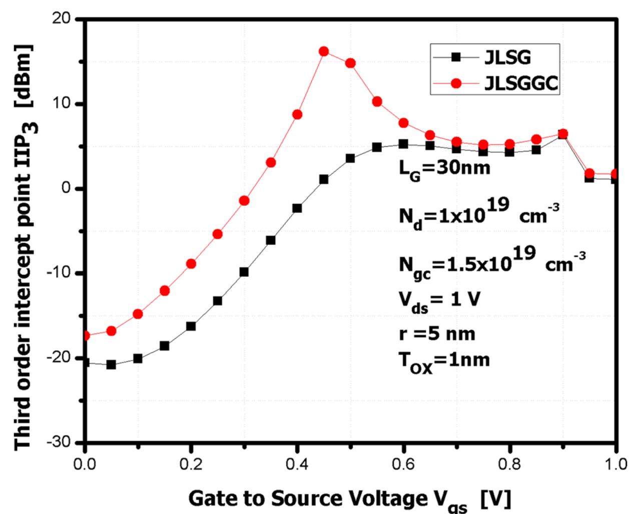


Fig. 9 A Plot of IIP_3 as a function of V_{gs} for JLSGGC and JLSG MOSFETs work function (ϕ_m), diameter(Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

showing degradation in linearity performance. Hence SJLGC MOSFET can be chosen to be a potential candidate for low-power analog applications during the lower value of VGS possessing lower distortion [37, 38]

It is G_{m3} which is mostly responsible for generating inter-modulation terms i.e. amplitude of the main signal is distorted along with the amplitudes of sideband signals. In advanced RF communication systems, 3rd order intermodulation intercept point (IIP_3) is considered a major source for nonlinear systems and devices.

The IIP_3 is expressed as: [38]

$$IIP_3 = \frac{2 \times G_{m1}}{3 \times G_{m3} \times R_S} \tag{6}$$

Figure 9. shows that IIP_3 for the JLSGGC MOSFET is more than the traditional one, suggesting better suppression of intermodulation terms in NWJL MOSFET. The linearity of the device is assessed through higher variable and inter-modulation intercept points [39].

The 1-dB compression point (P1dB) of an RF power amplifier refers to that point where the gain of the amplifier reduces by 1 dB. This point indicates the amount of RF input power needed to ensure a loss of 1 dB. The highest allowable input power to the RF mixer is obtained from this point.

1 dB compression point is expressed as: [38]

$$1 - dB \ \ compression \text{ point} = 0.22\sqrt{\frac{G_{m1}}{G_{m3}}} \tag{7}$$

P1 dB represents the level of output power at which there is a fall in gain by 1 dB from its saturated constant value. It is desirable to operate the amplifiers below the P1dB point. The higher value of 1-dB compression point results in lower distortion and reduced inter-channel interference so that RF and Microwave systems can operate linearly. Our proposed devices possess better linearity than the traditional counterpart as they achieve higher P1dB than JLSG MOSFET as noticeable in Fig. 10. In graded channel architecture there is an increase in carrier

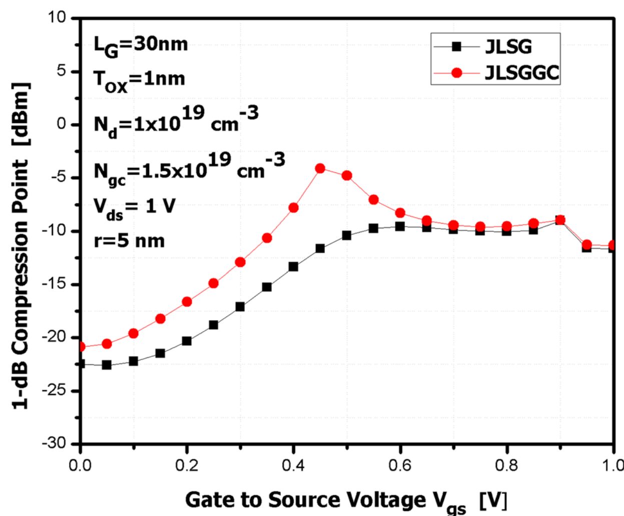


Fig. 10 A plot of P1dB VsV_{GS} for JLSGGC and JLSG MOSFETs at work function (ϕ_m), diameter (Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

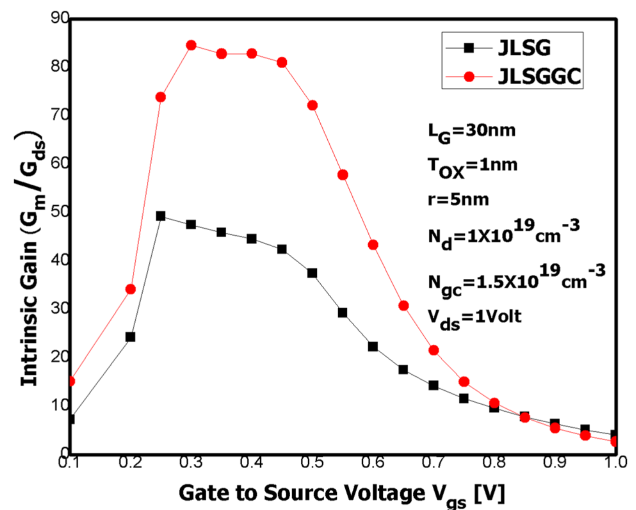


Fig. 11 A plot of intrinsic gain VsV_{gs} for JLSGGC and JLSG MOSFETs at work function (ϕ_m), diameter (Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

Table 2 Comparison of FOMs for linearity analysis

SL.NO	Parameters	JLSGGC	JLSG
1	Transconductance, G_m[S/µm]	0.00009	0.00005
2	Second-order transconductance, G_{m2} [S/ µm]	0.0008	0.0010
3	Third-order transconductance, G_{m2} [S/ µm]	0.002	0.003
4	Second-order variable intercept Point, VIP_2	1.25	0.75
5	Third-order variable intercept Point, VIP_3	3.5	2
6	Third-order intermodal dispersion, IMD_3 [dBm]	40	20
7	Third-order intercept point, IIP_3[dBm]	5	4
8	1-dB compression Point [dBm]	− 10	− 12

transportation towards the drain end due to reduced electric field [33]. Although both of the devices have surrounded gate structures the impact of gate controllability in JLSGGC MOSFET is more in focusing the electrons in the channel towards the drain end owing to their higher transportation efficiency. This results in a higher I_d, hence the transconductance. Higher G_m leads to an improved 1 dB compression point. The results discussed above are summarized in Table 2 for a comparative study.

Apart from linearity analysis, analog/RF performance figure of merits (FOMs) such as intrinsic gain, cut-off frequency, maximum frequency of oscillation are investigated for the proposed device.

Intrinsic gain is the highest possible voltage gain of the transistor amplifier irrespective of the biasing point.It is one of the figure of merits (FOMs) to access the analog circuits. Intrinsic gain is the ratio of the transconductance (G_m) to output conductance (G_{ds}). Figure 11 depicts the comparison of intrinsic gain in between JLSG and JLSGGC MOSFETs.

Our proposed device posses higher gain as compared to the conventional one as evident from Fig. 11. The reason for this is the higher transconductance (G_m) and lower output conductance (G_{ds}) exhibited by JLSGGC MOSFET. The lowering of G_{ds} in the proposed device is due to the discontinuity in electric field along the channel where it is graded. The higher doping region of the channel absorbs additional V_{ds} and doesn't allow the punch through to occure. This is known as screening effect due to which G_{ds} reduces in JLSGGC Mosfet [40].

The cut-off frequency (f_T) is that frequency of an amplifier where short circuit current gain is one.It has significance in evaluating the radio frequency performance of RF amplifier.The analytical formula for f_T is given by: [34, 37, 38]

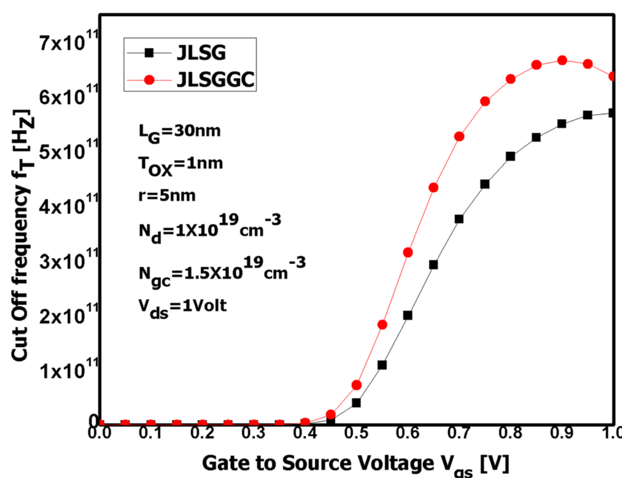


Fig. 12 A plot of f_T VsV_{gs} for JLSGGC and JLSG MOSFETs at work function (ϕ_m), diameter (Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

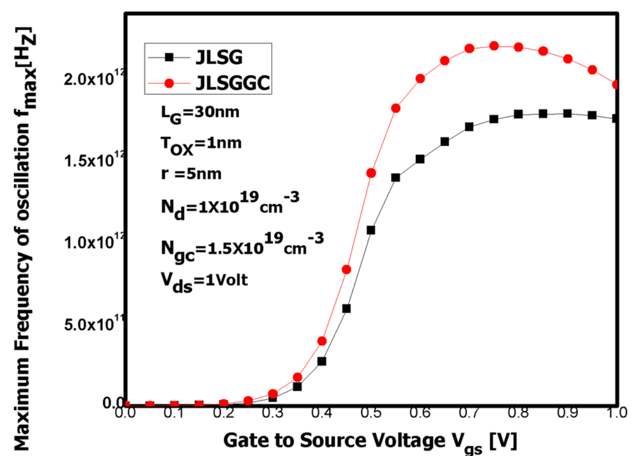


Fig. 13 A plot of f_{max} VsV_{gs} for JLSGGC and JLSG MOSFETs at work function (ϕ_m), diameter (Tsi) and graded channel length (L_{gc}) are 5.0 eV, 10 nm, 15 nm respectively

$$f_T = \frac{G_m}{2\pi C_{gg}} \tag{8}$$

In Eq. (8), C_{gg} is the intrinsic inter electrode gate to gate capacitance. The comparison of f_T is illustrated in Fig. 12. The volume of inversion charges reduces towards the source end due to discontinuous electric field in the graded channel structure. V_{gs} gradually looses its control towards the source end to invert the charges. As a result, JLSGGC MOSFET posses lower C_{gg} than JLSG MOSFET. Cut off frequency is more in JLSGGC MOSFET because of increased G_m and decreased C_{gg} in the device.

The upper limit of frequency for successful operation of RF amplifiers are quantified by f_{max}.It is the frequency at which power gain is unity. The expression for f_{max} is given by:[34, 37, 38]

$$f_{max} = \frac{f_T}{\sqrt{4R_g(G_{ds} + 2\pi f_T C_{gd})}} \tag{9}$$

In Eq. (9), R_g, C_{gd},G_{ds} are the gate resistance, gate to drain capacitance, drain to source conductance respectively. f_{max}

Table 3 Comparisionof analog/RF FOMs

Parameters	L_G = 30 nm,Tsi = 10 nm	
	Proposed work	Ref. [20]
Intrinsic gain	80.21	42.3
F_T (Hz)	617 × 10^9	567X10^9
F_{max} (Hz)	2 × 10^{12}	9 × 10^{11}

varies exactly in the same way as f_T w.r.t V_{gs} as shown in Fig. 13. The maximum frequency of oscillation is more in JLSGGC MOSFET than JLSG MOSFET. This is because the increase in parasitic drain to source capacitance is compensated by decrease in G_{ds} in the proposed device.

Table 3 represents a comparison of performance indexes between the proposed device and one comparable device (laterally graded with double gate junctionless architechture)reported in literature.The surrounded gate structure brings improvement in JLSGGC MOSFET as shown in Table 3.This comparision reveals that our proposed device is a befitting candidate for VLSI and RF applications.

5 Conclusion

The impact of a non-uniformly doped channel (graded channel) on the linearity performance of nanowire junctionless graded channel MOSFET is investigated in this paper. The existence of an additional electric field peak at the location where the channel is graded leads to the enhancement of on-state current. Thus the transportation capability of charge carriers is enhanced 35.53% improvement in the 1- dB compression point for our proposed device, suggesting its more linearity in comparison to comparison to JLSG MOSFET in the subthreshold region. Higher value of intrinsic gain of JLSGGC MOSFET in the sub threshold region is best suitable for its low power switching applications.The proposed device can be a better choice to operate in wide range of RF spectrum because of its higher cut-off frequency and maximum frequency of oscillation. This paper demonstrates that a compromise is required according to the utilization of the novel MOSFET in various areas. The present paper paves the path to new additional inquiries for the proposed device from its application area.

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Declarations

Conflict of interest The authors declared there is no conflict of interest in this work.

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