Design study of gate-all-around vertically stacked nanosheet FETs for sub-7nm nodes

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Abstract

Vertically stacked horizontal nanosheet gate-all-around transistors seem to be one of the viable solutions toward scaling down below sub-7nm technology nodes. In this work, we compare electrical performance, including variability studies of several horizontal nanosheet transistors toward transistor structure optimization. We explore the impacts of nanosheet width and thickness on the electrical performance and outline important design guidelines necessary for vertically stacked nanosheet FETs. An increase in the complexity of the stacked nanosheet structures can lead to significant device variability. Using numerical simulation, we study the characteristics fluctuations induced by the random discrete dopants (RDD) and metal grain granularity (MGG) in nanosheet gate-all-around (GAA) transistors. We use 3-D quantum-mechanically corrected transport models in the simulation. It is observed that the σV_{TH} due to MGG variability is 12% higher than RDD variability while the RDD variability strongly influences the I_{ON} . The statistical simulation results predict that the presence of combined variability due to RDD and MGG strongly influences the threshold voltage variation (σV_{TH}) in nanoscale devices. This approach may be applied to the different types of variability, the geometry of the device, including the vertical and lateral dimensions of the transistor, and biasing conditions.

Keywords Stacked nanosheet FETs · Gate-all-around (GAA) · Random discrete dopants (RDD) · Source/drain extension · Metal gate granularity (MGG) · Variability

1 Introduction

Stacked nanosheet FETs (SNSFETs) have been emerged as new innovative device architecture to replace fin-shaped FETs (FinFETs) due to their high current driving capabilities, excellent electrostatics control, and high-frequency operation [1–3]. SNSFETs provide a higher current per layout footprint because it has a large effective channel width (W_{eff}) per footprint compared to nanowire FETs or even stacked nanowire FETs [2, 4, 5]. The use of technologies below 22 nm leads to a complexity of increased design with more potential sources of variability. However, these miniaturized transistors suffer from the process and

statistical variations, which significantly affect the overall performance of the circuit [6]. The manufacturing variation represents a random deviation from the specifications of typical design, which stimulates circuit degradation, abnormal power consumption, and diverging performance. Furthermore, as transistors scale down, the device to device variation also becomes important.

In SNSFETs, nanosheet width is not limited by fin pitch and fin quantization, giving more degree of freedom to achieve larger effective widths (W_{eff}) for circuit design [7]. W_{eff} significantly affects current drivability, electrostatics, and parasitic components. Advanced technologies are more likely to experience process variations such as line

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edge roughness (LER) and metal gate granularity (MGG). The variability of manufacturing represents a random deviation which changes the structure of the transistor, and therefore, changes the electrical properties of a circuit. For proper design optimization of NSFETs, it is essential to evaluate device design options. The process flow plays an important role in device design and its performance optimization [2]. Process variations of SNSFET have been investigated in terms of metal thickness variation, which includes intersheet spacing and metal thickness to minimize the threshold voltage, V_{TH} variability [8]. Many researchers have investigated the statistical variations of FinFETs and GAA-nanowire FETs and proposed various modeling frameworks for variability-aware design. The most significant statistical variations are random discrete dopants (RDD), metal gate granularity (MGG), and line edge roughness (LER) [9–15]. However, the intrinsic variation LER becomes insignificant due to the larger width of SNSFET compared to fin thickness in FinFETs [2]. According to Mittal et al., fin thickness do not represent the quantum confinement regime in the width direction [16]. Therefore, LER arising due to the lithography and etching process does not result in significant variability.

Although the use of metal as gate material is advantageous for controlling specific challenges, it changes grain orientations by generating different, randomly aligned work functions, which involves higher fluctuations in the work function. MGG of the gate induces work function variation (WfV), which causes V_{TH} variability in high- k /metal gate technology for sub-10 nm-technology nodes [17]. The WfV would also cause dc performance variations of SNSFETs; however, these have not been investigated in detail. The RDD-induced variations have been a dominant source of variability, which is not related to manufacturing technology. As the devices are scaled-down, the impact of the source/drain (S/D) parasitic resistance becomes very significant and dominantly affects the device performance. Consequently, the S/D critical dimension variations of SNSFETs

have also been investigated [18]. In particular, the impacts of the S/D process variations, which include S/D epitaxy shape, depth, S/D length, and S/D doping concentration on the Si-FinFETs, have been addressed in several studies [19–22]. Still, the analysis of RDD-induced variations in the S/D extensions on SNSFETs has not been explored in detail. From a design perspective, these challenges require precise estimates of the circuit behavior, emphasizing the importance of indicating new design guidelines capable of handling these challenges to maintain the technology progress. In this work, the variation in width and thickness of nanosheet has been studied to propose a better design. The metal work function variation, and RDD-induced variations in the S/D extensions in SNSFETs, have also been explored in details. The main focus is to evaluate how the device variability can be accurately predicted in nanosheet GAA FETs and define guidelines that can be used by the device designers.

This manuscript is organized as follows: Section 2 describes the device specifications and simulation parameters. The performance of different device geometries is analyzed in Sect. 3. We address the SNSFET device random fluctuation induced by RDD and MGG via 3-D numerical device simulations. A statistical modeling approach is used to model the observed variability and identify the sources of variations in terms of the sensitivities to each source of variability. We investigate the random fluctuation considering MGG in conjunction with RDD in Sect. 4. The concluding remarks are presented in Sect. 5.

2 Device structure and simulation methodology

The simulated device SNSFET is a three-dimensional structure with 14 nm gate length, as shown in Fig. 1a. The cross-sectional view of three stacked nanosheets and the net doping concentration is shown in Fig. 1b and c,

Fig. 1 **a** Schematic of SNSFETs ($L_g = 14\text{ nm}$), **b** the cross-sectional view of three stacked nanosheets and **c** Net doping concentration of SNSFET is shown

Table 1 Device details of SNSFETs

Device parameters	Values
Nanosheet thickness (H_{NS})	4–6 nm
Nanosheet width (W_{NS})	3–12 nm
Gate length (L_g)	8–14 nm
High-k (HfO_2) thickness	1.5 nm
Oxide thickness (T_{OX})	0.5 nm
Epi-length	14 nm
Epi-top-width	8 nm
Epi-middle-width	25 nm
Epi-bottom-width	14 nm
Spacer length (L_{SP})	7 nm
Channel-doping (N_{CH})	10^{16} cm^{-3}
S/D-doping	10^{20} cm^{-3}

Fig. 2 Comparison of the simulated transfer characteristics with reported experimental data [from reference 2] in linear and log scale

respectively. All the critical device geometry parameters are defined in Table 1. The width (W_{NS}) of SNSFET is ranging from 3 to 12 nm and thickness (H_{NS}) ranging from 4 to 6 nm. The channel is n-doped (N_D) with a doping concentration of 10^{16} cm^{-3} , and the source/drain (S/D) extension regions are heavily p-doped (N_A) with a doping concentration of 10^{20} cm^{-3} . The gate oxide consists of SiO_2 and HfO_2 of thickness is 0.5 nm and 1.5 nm, respectively, titanium nitride (TiN) is used as the gate material. Considering the diverse requirements in device simulation, it is natural to ask for the level of confidence at which device simulation tools are useful for device development. To gain confidence in simulations of SNSFETs, we first simulate the reported experimental electrical characteristics of SNSFETs [2]. The structure used for 2D numerical simulation is shown in the inset of Fig. 2, and it is designed to match with actual SNSFETs used in this study. Figure 2 shows the calibration of the drain current of a three-stack

SNSFET reported in reference [2] for $V_D = 0.05 \text{ V}$ and 0.7 V in log scale and linear scale. For calibration, L_g and H_{NS} are selected as 12 nm and 5 nm, respectively. The calibration results obtained from our simulations show a good agreement with the reported experimental data. The reproduction of the experimental characteristics of SNSFETs by using the physics-based models described below gives the device designers a high confidence level regarding the effectiveness and feasibility of the models used toward predictive simulations.

The drift–diffusion (DD) model can be used to simulate the transportation inside the channel of the device with several limitations [23, 24]. To include the non-equilibrium transport phenomena, the electrostatic potential has to be calculated from the Poisson equation including quantum corrections combined with the current continuity equation for electrons to calculate the electron current density ($J_n(r)$)

$$J_n(r) = |q|\mu_n(r)n(r)\nabla(\phi_n(r)) \quad (1)$$

$$\text{div}(J_n(r)) = qR(r) \quad (2)$$

where $\mu_n(r)$ is the electron mobility and $R(r)$ is the recombination term.

Density-gradient (DG) quantization model [25] considers the quantum confinement effects of the nanosheet channels were calculated self-consistently with the Poisson, drift–diffusion, and carrier continuity equations. The quantum corrected drift–diffusion carrier transport model is incorporated in MINIMOS-NT [26]. The DG quantum potential for electrons, $V_{DG}(r)$ [27], is obtained as:

$$V_{DG}(r) = \frac{2[b_n]\nabla^2(\sqrt{n(r)})}{\sqrt{n(r)}} = \phi_n(r) - V_{cl}(r) + \frac{k_B T}{q} \ln\left(\frac{n(r)}{n_i(r)}\right) \quad (3)$$

$$\text{where } [b_n] = \frac{\hbar^2}{4qr_n} \begin{pmatrix} 1/m_x & 0 & 0 \\ 0 & 1/m_y & 0 \\ 0 & 0 & 1/m_z \end{pmatrix}.$$

Here, $r = (x, y, z)$ is the spatial coordinate, $\phi_n(r)$ is the electron quasi-Fermi potential, $n_i(r)$ is the intrinsic carrier concentration of electron and holes, $V_{cl}(r)$ is the classical electrostatic potential, k_B , T , and $\hbar$ are the Boltzmann constant, the lattice temperature, and the reduced Planck constant, respectively, r_n is the dimensionless parameter that accounts for statistical effects and m_x , m_y , and m_z are the DG electron effective masses in the x , y , and z directions, respectively. The distributions of electron current density contours for the simulated SNSFET at on-state and off-state are illustrated in Fig. 3. At on-state, due to the presence of V_{GS} , the electric field is generated all around the gate. The strength of net electric field is high in sidewalls

Fig. 3 Electron current density contour at on-state and off-state for NSFET across the channel with $W_{NS} = 12$ nm and $H_{NS} = 5$ nm

compared to top and bottom wall of the gate. This results in such distribution of the carrier and current density as shown in Fig. 3.

The 3D numerical device simulation is analyzed using the quantum corrected drift–diffusion transport model. Shockley–Read–Hall and Auger recombination models are used for minority carrier recombination [28, 29]. Slotboom model for bandgap narrowing is considered [30]. The calibrated mobility models included in our simulation framework are high field saturation, Coulomb scattering, and inversion and accumulation. Lombardi mobility model is used to account for various geometric quantization effects like thickness-fluctuation, phonon, and surface roughness scattering [31].

3 Results and discussion

In this section, we have analyzed different NSFET configurations and the effect of process-induced variabilities RDD, MGG, and their combined impact on the performance of SNSFETs. A technology CAD simulation framework has been used to study the device performance variations.

3.1 Impact of nanosheet width and thickness on the performance of SNSFET

We compared and analyzed each NSFET configuration through threshold voltage (V_{TH}), ON-state drive current (I_{ON}), OFF-state leakage current (I_{OFF}), subthreshold swing (SS), and drain-induced barrier lowering (DIBL). The transfer characteristic ($I_D V_{GS}$) plot is analyzed by varying W_{NS} from 3 to 12 nm with fixed H_{NS} at 5 nm, as shown in Fig. 4a. It is observed that SNSFET provides an improvement in the drive current for higher nanosheet width due to larger effective channel width.

Figure 4b shows I_{ON} as a function of the $V_{TH,sat}$ for SNSFETs with W_{NS} (3–12 nm) at L_g (8–14 nm). By reducing

the gate length to 8 nm, the reduction of V_{TH} results in an increase of I_{ON} . The nanosheet width reduction also induces a higher $V_{TH,sat}$ due to stronger confinement potential. It is also observed that the increase in I_{ON} is due to enhanced effective width. Figure 4c shows I_{OFF} as a function of W_{NS} for different H_{NS} at $V_{DS} = 0.7$ V. I_{OFF} also increases with increasing H_{NS} due to the reduction in potential barrier height, and it can be reduced by using thinner nanosheet. The variations of DIBL as a function of sheet width, which is shown in Fig. 4d, indicate the trade-off between sheet width, which dominates the intrinsic performance of the devices and the immunity to short channel effect (SCE).

Figures 5a and b show the impact of an increase in nanosheet width on SS and DIBL for different gate lengths, respectively. It is observed that the SS degradation at a gate length of 14 nm is marginal. However, an 11 mV/decade SS degradation is observed when the gate length reduces to 8 nm. SNSFETs with thinner width have smaller SS degradation due to enhanced gate control over the channel. Figure 5b shows DIBL has a similar trend with SS, and wider nanosheet provides higher DIBL. The impact of nanosheet width on the I_{OFF} and I_{ON}/I_{OFF} ratio is illustrated in Figs. 5c and d, respectively. It is observed that smaller nanosheet width provides a better I_{ON}/I_{OFF} ratio due to larger overdrive voltage. However, wider nanosheet provides larger I_{ON} and smaller I_{OFF} , so I_{ON}/I_{OFF} ratio gets better due to enhanced effective width. Figure 5d shows I_{OFF} increases with an increase in the nanosheet width, which can be mitigated by using thinner nanosheet. Large I_{OFF} degradation is observed when the gate length reduces from 14 to 8 nm. Finally, optimized SNSFET is presented considering maximum performance improvement with W_{NS} and H_{NS} of 12 nm and 6 nm, respectively. The I_{ON} , DIBL, and SS of presented SNSFET are 73.4 μA , 23.41 mV V^{-1} , and 67 mV/dec, respectively.

3.2 Impact of random dopant fluctuation

The fluctuation of dopants can be used to analyze the impact of RDD in terms of their number and position. Figure 7 shows that the number of dopants follows Poisson distribution, and the location of dopants follows a uniform distribution. Based on the doping concentration, the dopant position is determined randomly. Here the dopant discretization is only executed in the source and drain extension regions [32–34]. Both position and dopant number variations affect the transfer characteristics and other device parameters. The discrete dopants are positioned in the device randomly, and the electrostatics associated with these random dopants are calculated by using the Sano method [35]. The number density of the discrete dopant is given by

Fig. 4 **a** $I_D V_{GS}$ of NSFETs having different W_{NS} at $V_{DS} = 0.7$ V. **b** I_{ON} , as a function of $V_{TH,sat}$ for SNSFETs with $W_{NS} = 3-12$ nm at $L_g = 8-14$ nm. **c** I_{OFF} and **d** DIBL of NSFETs with different W_{NS} and H_{NS}

$$n(r) = N_f \frac{k_c^3}{2\pi^2} \frac{\sin(k_c r) - (k_c r) \cos(k_c r)}{(k_c r)^3} \quad (4)$$

where N_f is the normalization factor, k_c is the inverse of screening length, and r is the distance from the discrete dopant. The screening length can be calculated by using Conwell–Weisskopf model [35, 36] and defined as $k_c \approx 2(N_{D/A})^{1/3}$ where $N_{D/A}$ represent donor/acceptor concentration.

$I_D V_G$ plots of 14 nm gate length SNSFET are shown in Fig. 6, including discrete dopants fluctuations in the S/D extension regions at a drain bias of 50 mV and 0.7 V. The random dopant fluctuations in the source and drain extension induce the change in the V_{TH} , channel electrostatic potential, and source-channel potential barrier, which further results in I_{ON} variation in these regions. In RDD, the potential fluctuations due to donors in the source and drain extensions lead to large fluctuations in the source/drain access resistance which interpret an enhancement in the on-current variation. This effect will become increasingly important with further scaling because of the reduced volume of the access regions. From Fig. 7, it

is observed that the figure of merits: V_{TH} , I_{OFF} , I_{ON} , and SS distributions subject to random dopants, i.e., RDD in the S/D extension. The mean (μ) and standard deviation (σ) of V_{TH} , I_{OFF} , I_{ON} , and SS are evaluated. An analytical model for V_{TH} , due to statistical dopant fluctuations has been reported for two-dimensional (2D) cross section in reference [37]. As slices of a 2D sheet can be integrated over the depth to give a 3D sheet, the use of the reported analytical model can be extended to compute V_{TH} for the 3D NSFET. The variance of dopant fluctuations in a sheet is the total number of dopants in the sheet. The number of dopants fluctuations per unit depth of cross section of the sheet of dopant is considered as $N_{sheet} = N_A W_{NS} H_{NS}$. Since $dN_{sheet}(y)$ is the random variable for the area of $W_{NS} H_{NS}$ at a depth 'y' of the sheet, $dV_{TH}(y)$ becomes the random function in this sheet of depth dy and can be expressed as [8]:

$$dV_{TH}(y) = \frac{q}{\epsilon_{Si}} \frac{dN_{sheet}(y)}{W_{NS} \times H_{NS}} y \quad (5)$$

where q is the electronic charge, ϵ_{Si} is the relative permittivity of Si. $dV_{TH}(y)$ is solved for a particular value of dz along the longitudinal axis (z-axis). The solution of each

Fig. 5 **a** SS **b** DIBL **c** I_{ON}/I_{OFF} and **d** I_{OFF} as a function of W_{NS} for NSFETs having different L_g at $V_{DS}=0.7$ V

Fig. 6 Transfer characteristics ($I_D V_G$) of 14 nm gate length SNSFET in linear and log scale including random discrete dopants in the S/D extension at a drain bias of **a** 50 mV and **b** 0.7 V

cross section of the sheet further can be integrated over the entire length (L_{eff}) to consider the entire sheet. The V_{TH} of the SNSFET as a function of individual nanosheet can then be expressed as [38]:

$$V_{TH} = -\beta\eta \ln \left(\sum_{i=n} e^{\frac{-V_{TH,i}}{\beta\eta}} \right) \quad (6)$$

Fig. 7 Distributions of the impact of RDD-induced fluctuations in the S/D extension on **a** V_{TH} **b** I_{OFF} **c** I_{ON} and **d** SS for 200 different configurations

where $\beta = \frac{kT}{q} = 26\text{mV}$ at room temperature, $\eta = (SS(\text{mV/dec})/60)$, and $V_{TH,i}$ is the threshold voltage of each sheet. Further, the impact of RDD-induced fluctuations on the σ (standard deviation) of V_{TH} can be expressed as:

$$\sigma V_{TH,RDD} \propto \frac{\sqrt[4]{N_A}}{\sqrt{W_{NS} \times H_{NS}}} \quad (7)$$

where N_A denotes the average substrate dopant concentration.

3.3 Impact of work function variations

Metal grain granularity due to the crystal orientation of the metal grain leads to the work function variations in high-k/metal gate nanoscale devices. The grains in the TiN metal

gate region are generated by using the Voronoi approach [8, 39]. The grain position, shape, size, and orientation are taken into consideration in the simulation to create various metal-gate grain patterns. In the gate region, variation in the threshold voltage is based on the work functions of different crystallographic metal grains at the metal/oxide interface. The various metal grains have different orientations, the probability of its occurrence, the work function values, and the average grain sizes. The simulation of the polycrystalline grain structures uses the Poisson–Voronoi model. For the assignment of boundary conditions on the gate area, it is divided into grids, and each grid point is assigned with a random number generated following the Poisson distribution function. The Voronoi algorithm is used to define the grain boundaries and separate gate area into different grains. Figure 8 shows two different work function patterns generated with three different average grain sizes of 1, 3, and 5 nm. Poisson–Voronoi

Fig. 8 MGG profile shows the generated Voronoi pattern for grain sizes of 1, 3, and 5 nm of the 14 nm gate length SNSFET

approach creates the appropriate metal grain area distribution, which is a similar distribution observed in the experimental results [40]. I_D - V_G plots of 14 nm gate length SNSFET for MGG variations are shown in Fig. 9. The σV_{TH} distribution due to MGG can be related to grain size as:

$$\sigma V_{TH} \propto \frac{\text{Grain size}}{\sqrt{W_{eff} \times L_{eff}}} \quad (8)$$

The work function variability in the TiN metal grain is calculated by the Voronoi method [39, 41]. By employing two possible grain orientations $\langle 200 \rangle$ and $\langle 111 \rangle$, for the TiN metal gate with a difference of 0.2 eV between the work function values. According to grain orientations, the effective work function and shape of each metal grain vary. In this work, we analyze for three different grain sizes 1, 3, and 5 nm and assume that the distribution of work function of TiN metal gate grain orientations is 4.55 (red color) and 4.35 eV (blue color) with 60% and 40% probability, respectively, as shown in Fig. 8. As the work function fluctuations consider only two different grains to calculate the effective grain number (N_{eff_grain}), which has been proposed in reference [41]. Therefore, N_{eff_grain} distributed on the metal surface of SNSFET is expressed as

$$N_{plate_region} = \frac{L_g \times 2 \times \pi \{H_{NS}/2 + (W_{NS} - H_{NS})/\pi + T_{OX}\}}{\pi \times \left(\frac{\text{Grain size}}{2}\right)^2} \quad (9)$$

Considering ' i ' is the number of grains having a work function of 4.55 eV and ($N_{eff_grain} - i$) is the number of grains having a work function of 4.35 eV. The metal gate work function can be calculated as the area-weighted average work function of all the grains present on the surface of the metal. The σV_{TH} of work function variation shows a higher sensitivity to the number of grains or the size of the grain, as shown in Eq. (10). The probability distribution function (P_i) is the probability of all grains distributed

on the metal surface, as shown in Eq. (11). The metal gate work function (ϕ_i) is shown in Eq. (12):

$$\sigma V_{TH} = \sqrt{\frac{1}{N_{eff_grain}} \left(\sum_{i=0}^{N_{eff_grain}} (P_i \phi_i^2) - \sum_{i=0}^{N_{eff_grain}} (P_i \phi_i)^2 \right)} \quad (10)$$

$$P_i = \frac{N_{eff_grain}!}{i! (N_{eff_grain} - i)!} (0.6)^i (0.4)^{N_{eff_grain} - i} \quad (11)$$

$$\phi_i = \frac{i}{N_{eff_grain}} (4.55 \text{ eV}) + \frac{N_{eff_grain} - i}{N_{eff_grain}} (4.35 \text{ eV}) \quad (12)$$

The V_{TH} distribution, due to MGG, spreads more toward the head and tail regions with an increase in grain size is shown in Fig. 10. As nano-sized grains are considered, these distribution curves are very close [39]. This results in more deviation of the distribution shape from its normal distribution. As the grain size increases, the V_{TH} distribution due to MGG for both $V_{TH, Lin}$ and $V_{TH, Sat}$ becomes more and more constrained at both the upper and lower tails alike to the behavior reported for bulk MOSFETs [42]. Due to the increase in the grain size, the total number of grains present in the gate surface decreases. As a result, the work function probability distribution diverges from the normal distribution and becomes discrete. Therefore, the increase in potential fluctuations will increase V_{TH} variability. With the increase in grain size from 1 to 5 nm, σV_{TH} increases by 161.2% and 151.2% in linear and saturation regions, respectively.

Figure 11 shows that the σ value of V_{TH} , I_{OFF} , I_{ON} , and SS variations increases with larger grain size at both the linear and saturation mode in SNSFETs. It is observed that when the grain size decreases, the σ is reduced. This reduction is almost linear, dependent on the grain size for σV_{TH} , σI_{ON} , σI_{OFF} , and σSS . In Fig. 11, as the grain size is increased from 1 to 5 nm, the σV_{TH} is increased from 3.8 to 9.6 mV (a factor

Fig. 9 Transfer characteristics (I_D - V_G) of 14 nm gate length SNSFET with MGG variations at an average grain size of **a** 1 nm, **b** 3 nm, and **c** 5 nm with 200 different probability configurations

Fig. 10 Q-Q plot of V_{TH} distribution due to MGG for different metal gate grain sizes in **a** 50 mV and **b** 0.7 V of drain bias, respectively

Fig. 11 Normalized distribution of V_{TH} , I_{OFF} , I_{ON} , and SS due to grain size variations for the 14 nm SNSFET at $V_D = 0.7$ V

Table 2 Footprint of grain size on standard deviations (σ) of V_{TH} , I_{OFF} , I_{ON} , and SS at $V_D = 0.7$ V

MGG (Grain size)	σV_{TH} (mV)	σI_{OFF} (pA)	σI_{ON} (μA)	σSS (mV/dec)
1 nm	3.8	2.65	0.167	0.174
3 nm	6.3	4.57	0.292	0.267
5 nm	9.6	7.67	0.441	0.447

of 2). The standard deviation of the subthreshold characteristics is summarized in Table 2.

The effect of MGG on V_{TH} with different grain sizes, i.e., 1, 3, and 5 nm, is shown in Fig. 11. The σV_{TH} in saturation mode is found to be 3.8 mV, 6.3 mV, and 9.6 mV for 1, 3, and 5 nm grain sizes, respectively. The effect of MGG on the V_{TH} is more noticeable in 5 nm grain size as the grain size is linearly dependent on the σV_{TH} . The V_{TH} variation is more severe when the grain size increase, as shown in

Fig. 11. This is because of the large number of grains in the metal gate area, suppressing the WFV-induced σV_{TH} .

The DIBL variability as a function of V_{TH} for different grain sizes at low and high drain biases is shown in Fig. 12. The DIBL shows a minimal correlation with V_{TH} , mainly for grain sizes of 3 nm and 5 nm. The linear dependence between these variables is evaluated by the Pearson correlation coefficient (CC). Even the grain size reduces from 5 to 1 nm, the CC of the DIBL is larger for $V_{TH, Lin}$ than $V_{TH, Sat}$. This trend has also been reported by Seoane et al. [43]. The significant separation between the linear and saturation drain biases for the 1 nm grain size is pronounced due to the DIBL effect.

3.4 Impact of combined variability sources

The effects of combined variability, i.e., RDD and MGG on the performance of SNSFETs, are shown in Fig. 13. Electrical transfer characteristics of 14 nm gate length SNSFET

including combined (RDD + MGG) variation are shown in Fig. 13.

The effect of fluctuation of random variations can be analyzed quantitatively using the statistical data. When the combined variability sources considered, it is observed that σV_{TH} increases by 12.7%, σSS increases by 54%, and σI_{OFF} decreases by 23.7% compared to RDD alone. When RDD is combined with MGG variability, they exhibit

substantially different potential perspective and carrier distribution which results these quantitative changes. It is found that the impact of MGG variability on I_{OFF} is more effective than the combined variability analysis cases. However, the impact of RDD variability on I_{ON} has a stronger effect than MGG and combined cases.

The V_{TH} variability arises due to RDD and MGG, and the correlation plot between SS and V_{TH} is shown in Fig. 14.

Fig. 12 Scatter plots due to MGG variation in the 14 nm SNSFET for three different grain sizes: 1 nm, 3 nm, and 5 nm for the DIBL as a function of V_{TH}

Fig. 13 $I_D V_G$ plot for the scaled 14 nm gate length SNSFET including combined (RDD + MGG) variations at a drain bias of **a** 50 mV and **b** 0.7 V

Fig. 14 Scatter plots showing the correlation between SS and V_{TH} considering the impact of RDD and MGG variability in SNSFET at $V_D = 0.7$ V

The linear regressions indicate the sensitivity of SS as a function of V_{TH} at a high drain bias. The SS shows negative correlations with V_{TH} , and the higher correlation is also observed in the combined variability effect. The higher the correlation coefficient (ρ) value, the less sensitive the variability is to a change in the drain bias.

Figure 15 shows the quantile–quantile plot of the distribution of SS due to the impact of the RDD and MGG variability sources, which follow a Gaussian distribution

Fig. 15 Statistical distribution of SS using a quantile plot for RDD and MGG variability sources at high drain bias

Fig. 16 Correlations between the device performance variations for SNSFETs with combined sources of statistical variability. The correlation scatter plots and correlation coefficients at high drain bias are also listed in the table

entirely. An increase in the σ_{SS} is due to combined variability sources and increases by 55.6% and 58.8% compared to MGG and RDD alone, respectively. The spread due to combined statistical variability increases and departs further from the normal distribution, as shown in Fig. 15.

Figure 16 shows the correlation and distribution between the device performance variations (V_{TH} , I_{OFF} , I_{ON} , and DIBL) summarize in terms of scatter plots and correlation coefficients. I_{OFF} shows strong negative correlations with V_{TH} ($\rho = -0.98$) for combined variability sources. Besides, the V_{TH} and I_{ON} are negatively correlated with $\rho = 0.67$ but less compared to the ρ value between V_{TH} and I_{OFF} . Positively correlated are I_{OFF} and I_{ON} with a $\rho = 0.63$. The DIBL shows negative correlations with V_{TH} . However, the relationship between DIBL and other variations are comparatively weak. It can be observed that the changes in DIBL are more pronounced in the combined case compared to MGG and RDD separately. Due to the MGG variation, the drain end channel barrier is lower due to the drain field, which results in surface potential variation. Therefore, DIBL exhibits considerable variation.

4 Conclusions

We have analyzed the DC performances of sub-7nm node SNSFETs having different geometrical structures to study their impacts on the various nanosheet transistor parameters. The wide NSFET results in improved I_{ON} because of

larger effective widths per footprint. I_{OFF} also increases with increase in the sheet width and this can be alleviated by using thinner nanosheet. DIBL is minimum for thinner nanosheet provided by enhanced gate control over the channel. SNSFETs provides more freedom for power-performance optimization due to the fine-tuning of W_{NS} . It is also evident that reducing the gate length can increase the drive current. I_{OFF} goes down drastically while scaling gate length from 14 to 8 nm in NSFET. We have also studied the intrinsic fluctuations including RDD, MGG and combined effect by 3D TCAD simulation. We have observed that the MGG sources predominantly affect the V_{TH} variability. We find that the σV_{TH} due to MGG variability is 12% higher than RDD variability. MGG-induced standard deviation shows linear reduction when the grain size decreases. The RDD sources strongly influence the I_{ON} variations because of access resistance variations. Furthermore, the combined sources of variability influence both the V_{TH} and SS variability. Finally, it is concluded that SNSFETs with larger width induces higher on-state drive current and smaller metal grains to improve device statistical variability immunity for future sub-7nm node devices.

Authors contributions E. Mohapatra has contributed to Concept Generation, Methodology, Result Analysis, and Drafting; T. P. Dash has contributed to Concept Sharing, Drafting, and Revising of the manuscript; J. Jena has contributed to Resource Collection, Simulation, and Result Analysis; S. Das has contributed to Resource Collection, Simulation, and Calibration; C. K. Maiti has contributed to Overall Supervising, Concept Sharing, Reading, and Editing.

Data availability The data may be provided as per requirement on request.

Code availability The code may be provided as per requirement on request.

Declarations

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

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