Research Article

Design of power-efficient CMOS based oscillator circuit with varactor tuning control

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Abstract
This paper presents a low-power, wide tuning range CMOS voltage-controlled oscillator with MCML (MOS current mode logic) differential delay cell. Voltage controlled oscillator (VCO) circuit is designed in TSMC 0.25 µm CMOS process. To achieve the broad frequency range concept of variable capacitance is employed in the proposed VCO circuit. Source/drain tuning voltage (V_{tune}) and body bias voltage (V_b) of I-MOS varactor are used to achieve variable capacitance at different I-MOS varactor widths (W). The dual control voltage of I-MOS varactor results in a tuning range from 0.528 GHz to 2.014 GHz. VCO's figure of merit (FoM) is 152.13 dBc/Hz with phase noise of −93.77 dBc/Hz at 1 MHz offset from the oscillation frequency. The proposed VCO dissipates maximum power of 3.127 mW.

Keywords Delay cell · I-MOS varactor · MOS current mode logic · Phase noise · Voltage controlled oscillator

1 Introduction

With the rapid growth in the high-speed wireless communication system, the demand for integrating high-performance CMOS circuit's on-chip is raising [1, 2]. Conventional CMOS circuit suffers from large power consumption at high speed due to dynamic power consumption directly related to the operation frequency. The different logic style has been proposed in the literature for low power consumption among them MOS current mode logic (MCML) is extensively used as an option to CMOS logic style for high-speed circuits. MCML dissipates less power at high frequency and provides high noise immunity [3–5]. Static power consumption due to the use of constant current sources is also a concern in MCML logic.

In comparison to the CMOS logic approach, MCML shows better power delay products at high frequency. In this paper, a power-efficient VCO is designed using the MCML technique for low-power applications. VCO circuits are designed by inductor-capacitor (LC) based or ring-based approach. A ring topology-based VCO is preferred over LC topology since its starting time is significantly less, and it avoids the use of passive inductors. Also, integration is straightforward and compatible with the digital CMOS fabrication process. Ring oscillator structures are usually constructed by several delay elements such as a logic gate and an operational amplifier. In the logic gate, the control current is modified to change the transition time of each delay stage. In the operation amplifier, the current is adjusted to vary the bias current so that the operation amplifier gains are modified to vary the oscillation frequency of VCO. Ring oscillators are widely used in applications like clock generators, frequency synthesizers, and analog to digital converters circuits [6, 7]. Ring oscillator provides a wide tuning range, quadrature or multiphase output, small die area compared to LC oscillator [8].

Further, various design structures of VCOs can be grouped into two major design categories as VCOs with

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single-ended and differential-ended delay cells [9, 10]. In a single-ended configuration, the maximum frequency is mainly depends on the delay time of delay cell. Various methods have been proposed to tune the ring oscillator frequency [11, 12]. On the other hand, differential-ended topologies are more preferable for high-speed applications because they provide better common-mode and supply voltage rejection performance. Differential-ended delay cells have many advantages over the single-ended cell-like single-ended VCO. They can be designed only by the odd number of delay stages compared with differential ended delay cell, and it has no common-mode rejection of supply voltage and body noise [13]. Multiphase output can also be obtained in differential-ended VCO [14]. Each delay stage in single-ended VCO is designed by an inverter that consist an NMOS and PMOS transistor. Alternatively, a differential-ended delay cell is designed by a load element (active and passive) and a differential pair. In both types of configuration, frequency variation is achieved by varying the delay cell's delay time. In this paper, MOS based varactor is used to vary the delay time of the proposed delay stage. In comparison to reverse-biased diode varactor, MOS varactors are more preferably used in CMOS circuits. This kind of varactors shows large capacitance and easiness of implementation in CMOS technology. Different configurations of MOS transistors are reported to work as MOS varactors. Different VCO designs based on the MOS varactors have been reported in [15–17]. In conventional structure drain, source, and substrate of a MOS transistor are tied together to form one end of the varactor. Variable capacitance is obtained with a change in the voltage across the varactor. In this paper, the MOS varactor working in inversion mode is used to obtain frequency tuning. In inversion mode, the bulk of the NMOS/PMOS transistor is connected with the lowest/highest voltage in the circuit. MOS varactor is placed at the output of each stage as a variable load element. With the change in load element, a tunable range of frequency is obtained in the proposed VCO.

Further, the paper is organized as follows: Sect. 2 describes the architecture of the proposed VCO. Section 3 discusses the result and performance analysis of the proposed VCO. Finally, Sect. 4 provides the conclusion.

2 VCO architecture

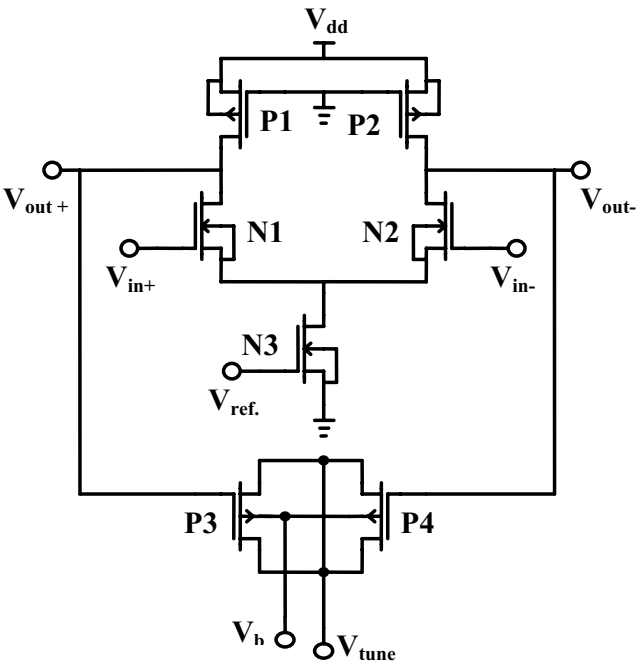
The circuit diagram of the proposed delay stage, along with a four-stage ring VCO with I-MOS varactor, is shown in Fig. 1. Figure 1a shows a differential-ended delay stage designed with MCML logic. MCML based delay cell include a pull-down network (PDN), a constant current source, and a pull-up load circuit. Pull down the network is designed with two NMOS transistors (N1, N2) as an input that performs the logic function. Two PMOS transistors (P1, P2) are used as a load element responsible for the voltage swing, and transistors (N3) function as a constant current source. PMOS transistors (P3, P4) of the I-MOS varactor are included to change the oscillation frequency of the proposed VCO. The function of the MCML delay cell is based on the principle of current steering. As the input voltage across the input transistor is high (low), the source coupled NMOS transistor pair steers the bias current (I_{ref}) to drain of N1 and N2, thus generates a low (high) output voltage. In the MCML delay cell, the PMOS transistor operates in the triode region, and the reference current generated by the transistor N3 is divided into two NMOS drain currents. The differential input voltage is applied at the input of NMOS transistors that is (V_{in+}) – (V_{in-}), the reference current is flowing through the transistor N3. A tunable frequency range is obtained by changing the control voltage V_{tune} and V_b of the I-MOS varactor. Figure 1b shows the four-stage ring VCO designed using four identical differential stages connected in a closed-loop. By varying the control voltage, the equivalent capacitance at the delay stage's output terminal varies, and subsequently output frequency of VCO changes.

The delay stage's working can be explained by considering the half part of the differential pair circuit. Input voltage is applied at transistor (N1), and the output voltage is obtained at the drain terminal of the N1 transistor. For a fixed value of reference voltage ($V_{ref.}$), transistor N3 works as a constant current source $I_{ref.}$ MOS transistor (P1) is acting as a load element. A frequency variation in VCO is achieved by connecting an I-MOS varactor at the delay cell's output node. A dual control voltage is applied to the I-MOS varactor. Due to a change in the capacitance, a wide range of frequency is achieved. The I-MOS varactor's capacitance is estimated with the model as shown in Fig. 2.

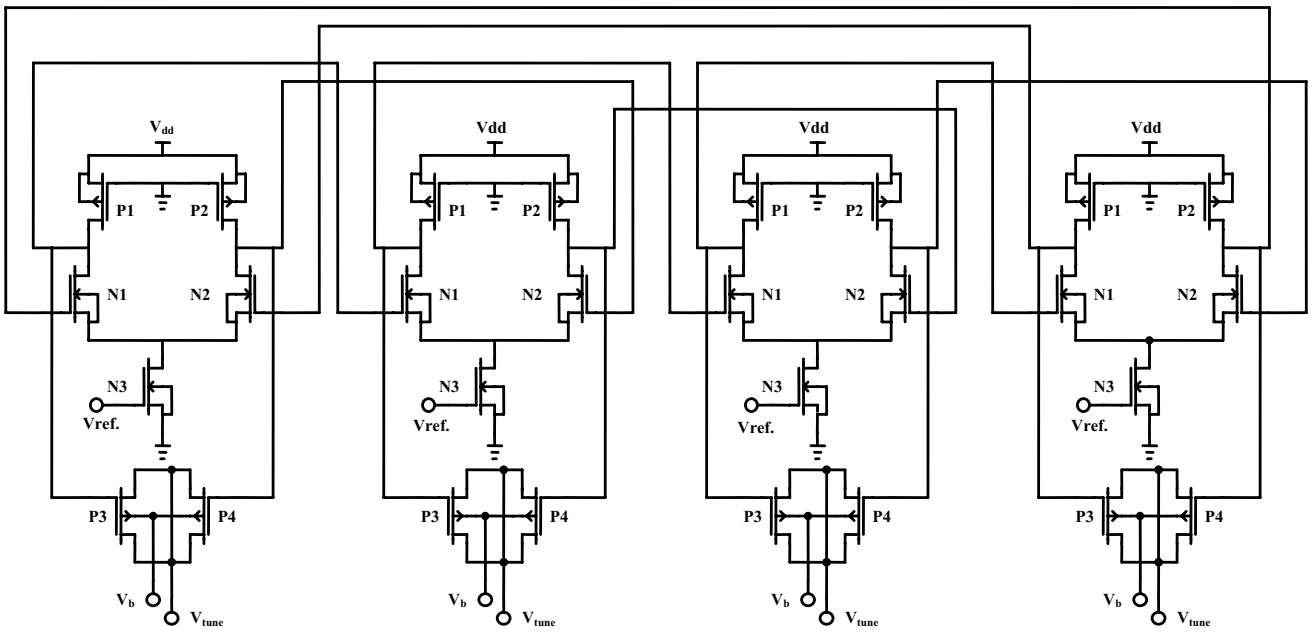
Due to variation in load capacitance, frequency tuning is achieved in the proposed VCO while keeping power consumption remains constant. Equivalent capacitance of I-MOS varactor is given by the Eq. (1).

$$C_{equi.} = C_{para.} + \frac{C_{ox} \times C_{dep.}}{C_{ox} + C_{dep.}} \tag{1}$$

where: $C_{para.}$, C_{ox} and C_{dep} are the parasitic capacitance, oxide capacitance and depletion capacitance under the gate, per unit area, respectively. Depletion capacitance under the gate oxide is given by the Eq. (2).



(a)



(b)

Fig. 1 Proposed (**a**) MCML based delay stage (**b**) four stages ring VCO

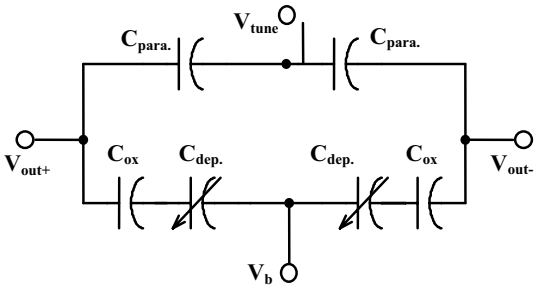


Fig. 2 Equivalent capacitive model of I-MOS varactor

Table 1 Frequency variation with tune voltage (V_{tune})

Source/drain voltage (V_{tune})	Output frequency (GHz)		
	W = 5 µm	W = 10 µm	W = 15 µm
1.5 V	1.472	0.965	0.721
1.6 V	1.431	0.936	0.694
1.7 V	1.393	0.898	0.661
1.8 V	1.342	0.861	0.633
1.9 V	1.303	0.828	0.606
2.0 V	1.273	0.800	0.584
2.1 V	1.244	0.779	0.565
2.2 V	1.221	0.759	0.553
2.3 V	1.194	0.745	0.542
2.4 V	1.174	0.735	0.532
2.5 V	1.166	0.731	0.528

$$C_{dep.} = \frac{\varepsilon_{si}}{X_d} \tag{2}$$

In Eq. (2), ε_{si} and X_d denotes the permittivity of silicon material and depletion width under the gate oxide. Variation in C_{equi} depends on the applied voltage across I-MOS varactor. As the control voltage increases, depletion width (X_d) under the gate oxide increases that result to decrease in the equivalent capacitance.

3 Results and discussions

The proposed VCO has been implemented in 0.25 µm CMOS technology. Frequency tuning range has been obtained with a change in control voltage i.e., V_{tune} and V_b of I-MOS varactor. Effect of change in supply voltage (V_{dd}) also has been observed. Output frequency tuning range of proposed VCO with V_{tune} variation from 1.5 V to 2.5 V at V_{dd} = 2.5 V and V_b = 2.5 V has been shown in Table 1. Proposed VCO achieved a variable frequency from 0.528 GHz to 1.472 GHz. Figure 3 shows the effect of V_{tune} on the output frequency. With rise in the tuning voltage, the equivalent capacitance at the output node of the delay stage increases, affecting the delay time of the delay stage. As a consequence, the output frequency of VCO decreases.

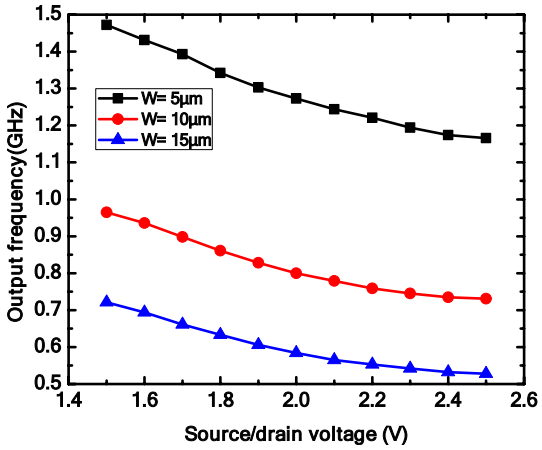


Fig. 3 Output frequency tuning characteristic with source/drain voltage (V_{tune})

Table 2 Frequency variation for different V_{dd}

Supply voltage (V_{dd})	Output frequency (GHz)			Power dissipation (mW)
	W = 5 µm	W = 10 µm	W = 15 µm	
2.0 V	1.428	0.940	0.710	1.744
2.1 V	1.573	1.042	0.770	1.923
2.2 V	1.686	1.127	0.839	2.080
2.3 V	1.808	1.199	0.900	2.223
2.4 V	1.913	1.272	0.954	2.359
2.5 V	1.992	1.332	1.000	2.490
2.6 V	2.055	1.378	1.032	2.618
2.7 V	2.119	1.415	1.060	2.746
2.8 V	2.152	1.443	1.085	2.873
2.9 V	2.196	1.461	1.095	3.000
3.0 V	2.198	1.477	1.115	3.127

Table 2 provides the output frequency variation with change in V_{dd} at fixed V_{tune} = 1.5 V, and V_b = 2.5 V. VCO shows a tuning range from 0.710 GHz to 2.198 GHz with variation in V_{dd} from 2 to 3 V with power dissipation variation from 1.744 mW to 3.127 mW. With the rise in the V_{dd}, the current is flowing in the delay stage increases, increasing the output oscillation frequency. Further, power

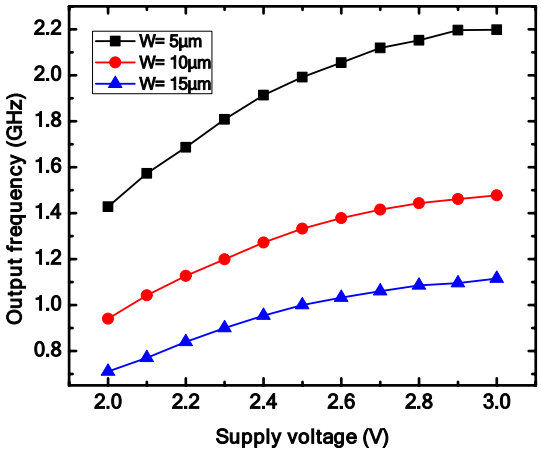


Fig. 4 Output frequency change with supply voltage variation (V_{dd}) at different value of MOS varactors width (W)

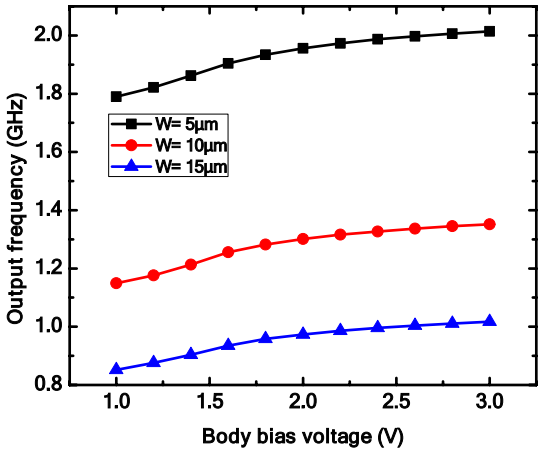


Fig. 5 Output frequency variation with body bias voltage (V_b) at different MOS varactor width (W)

Table 3 Output frequency variation with V_b

Body bias voltage (V_b)	Output frequency (GHz)		
	W = 5 µm	W = 10 µm	W = 15 µm
1.0 V	1.790	1.099	0.852
1.2 V	1.822	1.176	0.876
1.4 V	1.862	1.213	0.904
1.6 V	1.904	1.256	0.935
1.8 V	1.934	1.282	0.958
2.0 V	1.956	1.301	0.973
2.2 V	1.973	1.316	0.986
2.4 V	1.987	1.327	0.996
2.6 V	1.997	1.337	1.004
2.8 V	2.006	1.345	1.011
3.0 V	2.014	1.352	1.017

consumption directly related to the V_{dd} also shows the rising trends, as shown in Table 2. Figure 4 illustrates the frequency variation with I-MOS varactor width (W).

Table 3 shows the effect of variation in the V_b of the I-MOS varactor. Output frequency Variation with V_b is obtained at fixed V_{dd} = 2.5 V and V_{tune} = 1.5 V. From Table 3, it is evident that ring VCO oscillates in a range of 0.852 GHz to 2.014 GHz at a different value of MOS varactor widths (W). Figure 5 shows the trends for the frequency variation with V_b. With the increase in the V_b, equivalent capacitance across the gate and substrate terminal decreases, increasing the proposed VCO output frequency. Output waveforms for the VCO are shown in Fig. 6 with variation in V_{dd} and MOS varactor width (W).

Frequency tuning characteristic of the proposed VCO for different temperatures is presented in Table 4 at V_{dd}=1.8 V. Dual control voltages (V_{tune} and V_b) are fixed at 1.5 V and 2.5 V, respectively. The output frequency of proposed VCO decreases as temperature rises. With the change of temperature, parasitic effects in the circuit vary along with the carriers' mobility effects. Overall current in the circuit is affected by these variations, and output frequency decreases. The temperature dependence of generated frequency is plotted, as shown in Fig. 7.

Performance characteristics of the proposed VCO at various V_{dd} are presented in Table 5. At low V_{dd} phase, noise and merit figures are improved due to the power consumption reduction. The circuit, however, shows a reasonably good phase noise performance over the wide range of supply voltage. Phase noise and jitter are continuous random variations in VCO. Phase noise is generally represented in the frequency domain, and jitter is usually characterized in the time domain. Figure 8 shows the phase noise waveform of the proposed VCO at 1 MHz offset.

Table 6 shows the major performance parameters for the proposed VCO design and comparison with the previous reported work using the Figure of merit (FoM) is given by the Eq. (3). [17] Which evaluate three performance parameters of VCOs; phase noise, frequency and power consumption.

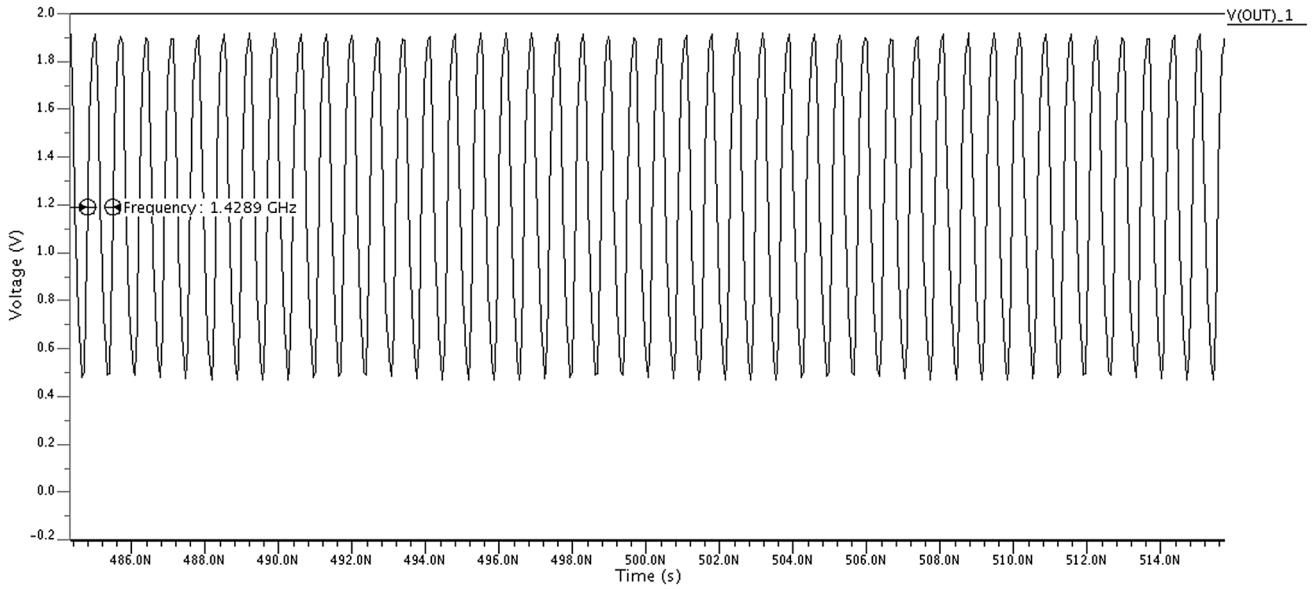


Fig. 6 Output waveform at supply voltage V_{dd} = 2 V with MOS varactors width W = 5 µm

Table 4 Parameters of proposed VCO for different temperatures

Temperature (°C)	Output frequency (GHz)		
	W = 5 µm	W = 10 µm	W = 15 µm
10	1.277	0.832	0.617
20	1.230	0.800	0.593
30	1.185	0.769	0.572
40	1.141	0.741	0.551
50	1.100	0.715	0.531
60	1.060	0.689	0.512
70	1.021	0.665	0.494
80	0.986	0.642	0.477

$$\text{FoM(dBc/Hz)} = 20\log\frac{f_{osc.}}{f_{off.}} - 10\log\frac{P_{diss.}}{1\text{mW}} - \text{PN} \quad (3)$$

where: f_{osc} is the resonating frequency of proposed VCO, $f_{off.}$ is offset frequency, P_{diss} represents the power consumption and PN define the phase noise in dBc/Hz of proposed VCO.

4 Conclusions

In this work, a low-power MCML based ring-based VCO in 0.25 µm standard CMOS technology is presented. MOS varactor tuning technique is utilized to obtain a wide range of frequencies. The proposed technique's results showed that improvements in power consumption, tuning range, and phase noise are obtained. The range of frequency

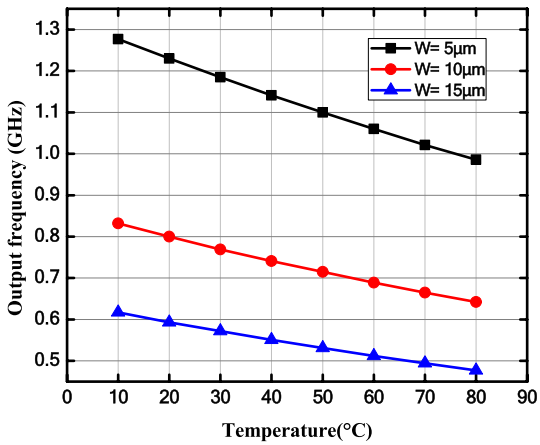


Fig. 7 Temperature dependence of output frequency with different I-MOS varactors width (W)

from 0.528 GHz to 2.014 GHz is achieved for the proposed VCO by altering the I-MOS varactor's dual control voltage. Proposed VCO achieves -93.77 dBc/Hz phase noise at an offset of 1 MHz from 1.272 GHz oscillation frequency. Proposed VCO has a figure of merit (FoM) of 152.13 dBc/Hz with a power dissipation of 2.359 mW. More design improvements in the proposed delay cell can be explored for nano scale VCO design with wider frequency range and low power. Additional tuning techniques in addition to MOS varactors with improved delay cell can results in better VCO design.

Table 5 Phase noise results at different supply voltage (V_{dd})

Supply voltage (V)	Source/drain voltage (V)	Body bias voltage (V)	Reference voltage (V)	Output frequency (GHz)	Power dissipation (mW)	Phase noise (dBc/Hz)	FoM (dBc/Hz)
2.0	1.5	2.5	1.5	0.940	1.744	-96.791	153.83
2.2	1.5	2.5	1.5	1.127	2.080	−94.948	152.80
2.4	1.5	2.5	1.5	1.272	2.359	−93.777	152.13
2.6	1.5	2.5	1.5	1.378	2.618	−93.230	151.83
2.8	1.5	2.5	1.5	1.443	2.873	−92.748	151.35
3.0	1.5	2.5	1.5	1.477	3.127	−92.333	150.56

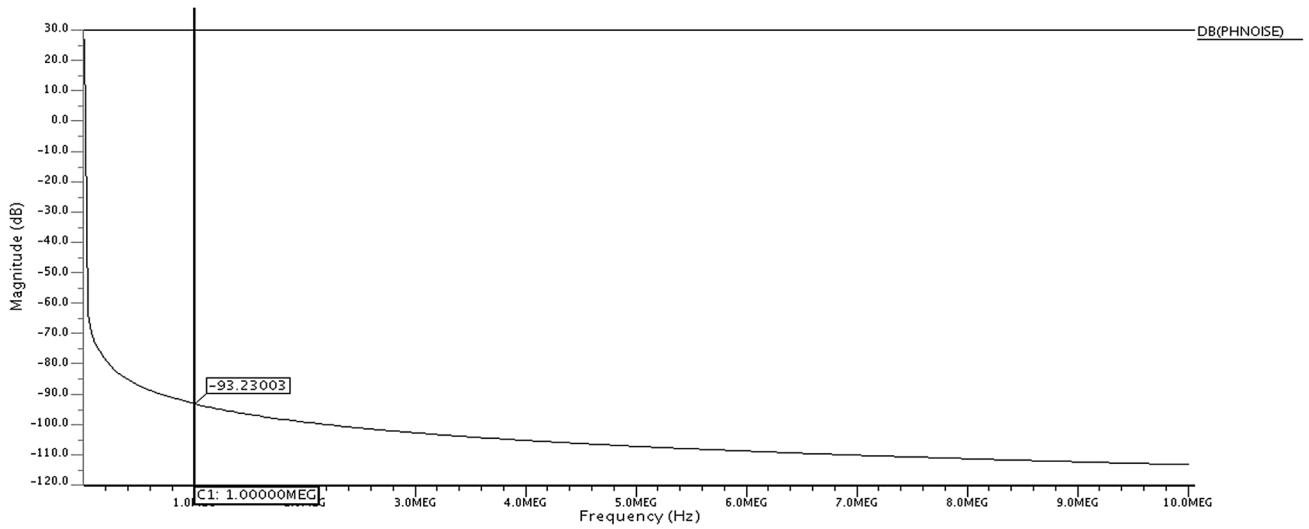


Fig. 8 Phase noise waveform at $V_{dd} = 2.6$ V with ($V_{tune} = 1.5$ V and $V_b = 2.5$ V)

Table 6 Proposed VCO comparison with earlier presented work

References	Frequency range (GHz)	Technology (μm)	Phase noise (dBc/Hz)	Power consumption (mW)	FoM (dBc/Hz)
[8]	9.8–11.5	0.50	−98@2 MHz	75	153.1
[9]	4.2–5.9	0.18	−99.1@ 1 MHz	58	156.28
[10]	1.77–1.92	0.18	−102@ 1 MHz	13	156.3
[18]	0.8–2.1	0.25	−85.4@1 MHz	45	–
[19]	0.8–2.4	0.25	−98.5 400KHz	59	152.83
[20]	5.16–5.93	0.18	−99.2 @ 1 MHz	80	166
[21]	0.661–1.27	0.50	−106@1 MHz	15.4	153.2
[22]	1.82–10.18	0.13	−88.4@1 MHz	5	156.5
This Work	0.528—2.014	0.25	−93.77@1 MHz	2.35	152.13

Declaration

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

References

1. An TJ, Son KS, Kim YJ, Kong IS, Kang JK (2014) A 8.7 mW 5-Gb/s clock and data recovery circuit with 0.18-µm CMOS. IEEE Int Symp Circuits Syst (ISCAS) 2014:2329–2332
2. Shylu DS, Paul PS, Moni DJ, Monica Helan JA (2020) A power efficient delta-sigma ADC with series-bilinear switch capacitor voltage-controlled oscillator. Telkomnika 18(5).
3. Pradeep KS, Kumar SS (2018) Design and development of high performance MOS current mode logic (MCML) processor for fast and power efficient computing. Clust Comput, 1–9. https://doi.org/10.1007/s10586-018-1917-5
4. Yamashina M, Yamashina H (1992) An MOS current mode logic (MCML) circuit for low-power sub-GHz processors. IEICE Trans. Electron. E75-C (10), pp 1181–1187.
5. Jamshidi V, Fazeli M (2018) Design of ultra-low power current mode logic gates using magnetic cells. AEU-Int J Electr Commun 83:270–279
6. Abiri E, Salehi MR, Salem S (2014) A low phase noise and low power 3–5 GHz frequency synthesizer in 0.18 µm CMOS technology. Microelectronics J 45(6):740–750.
7. Sai A, Kobayashi Y, Saigusa S, Watanabe O, Itakura T (2012) A digitally stabilized type-III PLL using ring VCO with 1.01 psrms integrated jitter in 65nm CMOS. In: IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp 248–250.
8. Van der Tang JD, Kasperkovitz D, Van Roermund A (2002) A 9.8–11.5-GHz quadrature ring oscillator for optical receivers. IEEE J Solid-state Circuits 37(3):438–442.
9. Danfeng C, Junyan R, Jingjing D, Wei L, Ning L (2009) A multiple-pass ring oscillator based dual-loop phase-locked loop. J Semiconductors 30(10):105014
10. Chen ZZ, Lee TC (2011) The design and analysis of dual-delay-path ring oscillators. IEEE Trans Circuits Syst I Regul Pap 58(3):470–478
11. Jangra V, Kumar M (2020) New low power differential VCO circuit designs with active load and IMOS varactor. AEU-International Journal of Electronics and Communications, 153191.
12. Kumar M (2018) Design of Linear Low-Power Voltage-Controlled Oscillator with I-MOS Varactor and Back-Gate Tuning. Circuits, Systems, and Signal Processing, pp 1–17. https://doi.org/10.1007/s00034-018-0748-1
13. Lee TH, Hajimiri A (2000) Oscillator phase noise: a tutorial. IEEE J Solid-State Circuits 35(3):326–336
14. Toh Y, McNeill JA (2003) Single-ended to differential converter for multiple-stage single-ended ring oscillators. IEEE J Solid-State Circuits 38(1):141–145
15. Kumar M, Dwivedi D (2018) A low power CMOS-based VCO design with I-MOS varactor tuning control. J Circuits Syst Comput 27(10):1850160
16. Karimi A, Ebrahimi E (2019) A new modified I-MOS varactor for linear range enhancement. Microelectron J 90:181–186
17. Andreani P, Mattisson S (2000). A 2.4-GHz CMOS monolithic VCO with an MOS varactor. Analog Integrated Circuits Signal Process 22(1):17–24.
18. Yang WR, Jiang WY (2007) A dual-path three-stage VCO with wide tuning range. In: 2007 7th International Conference on ASIC, pp 542–544.
19. Do MA, Zhao RY, Yeo KS, Ma JG (2003) New wideband/dualband CMOS LC voltage-controlled oscillator. IEE Proc Circuits Devices Syst 150(5):453–459
20. Eken YA, Uyemura JP (2004) A 5.9-GHz voltage-controlled ring oscillator in 0.18µm CMOS. IEEE J Solid-State Circuits 39(1):230–233.
21. Yan WST, Luong HC (2001) A 900-MHz CMOS low-phase-noise voltage-controlled ring scillator. IEEE Trans Circuits Systems II Analog Digital Signal Process 48(2):216–221
22. Fahs B, Ali-Ahmad WY, Gamand P (2009) A two-stage ring oscillator in 0.13 µm CMOS for UWB impulse radio. IEEE Trans Microw Theory Tech 57(5):1074–1082.