A 219- μ W ultra-low power low-noise amplifier for IEEE 802.15.4 based battery powered, portable, wearable IoT applications

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Abstract

Due to the increased processing data rates, which is required in applications such as fifth-generation (5G) wireless networks, the battery power will discharge rapidly. Hence, there is a need for the design of novel circuit topologies to cater the demand of ultra-low voltage and low power operation. In this paper, a low-noise amplifier (LNA) operating at ultra-low voltage is proposed to address the demands of battery-powered communication devices. The LNA dual shunt peaking and has two modes of operation. In low-power mode (Mode-I), the LNA achieves a high gain (S_{21}) of 18.87 dB, minimum noise figure (NF_{min}) of 2.5 dB in the -3 dB frequency range of 2.3–2.9 GHz, and third-order intercept point (IIP3) of -7.9 dBm when operating at 0.6 V supply. In high-power mode (Mode-II), the achieved gain, NF, and IIP3 are 21.36 dB, 2.3 dB, and 13.78 dBm respectively when operating at 1 V supply. The proposed LNA is implemented in UMC 180 nm CMOS process technology with a core area of 0.40 mm^2 and the post-layout validation is performed using Cadence SpectreRF circuit simulator.

Keywords 5G · CMOS · Dual shunt peaking · IoT · Low-voltage · Low-power · LNA · IIP3 · NF · Positive feedback

1 Introduction

The current technology trends in the world of electronics and communication are focused on wireless, portable, and wearable devices such as Internet-of-Things (IoT). The portable and wearable devices implicitly require battery power for operation. The present generation of electronics consumers have sophisticated personal communication because of the large number of portable and wearable communication devices available in the market. These portable and wearable devices are designed to create a wireless personal area network (WPAN). The backbone of these portable and wearable devices is the IEEE 802.15.4 standard for low-rate wireless personal area network (LR-WPAN) [1–3]. The specifications of the standard are listed in Table 1. The IEEE 802.15.4 standard applies stringent requirements on power consumption and silicon area

consumption since the devices are required to be portable and wearable.

The power consumption is prominent in the radio frequency (RF) front-end circuits such as LNA, Mixer, and VCO employed in the communication devices. Due to the movement of the communication devices, the signal strength varies and hence, more power is required by the RF circuits for proper signal reception. These devices are designed to be battery-operated, and hence, rapid battery discharge occurs due to the RF circuit operation. Therefore, the current necessity in the electronics and communication industry is to design energy-harvesting RF circuits for low-power operation of the wireless, portable, and wearable devices. This work intends to meet the necessity by proposing an ultra-low power LNA realised using UMC 180 nm process technology and its performance is validated using Cadence SpectreRF simulations.

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Table 1 Specifications of IEEE 802.15.4 receiver [1–3]

Noise figure	< 20.5 dB
IIP3	> − 32 dBm at high gain > − 10 dBm at minimum gain
Receiver sensitivity	−85dBm (minimum)
Input power	−85 to − 20 dBm
Frequency range	2.405–2.485 GHz
Channel bandwidth	2 MHz
No. of channels	16
Channel spacing	5 MHz

There are low-power LNA topologies reported in the literature [4–12]. The sub-mW low-power LNA design techniques include current reuse and inductive g_m -boosting [4], double g_m -enhancement [5], inductive peaking feedback [6], inductive degeneration [7], forward body bias (FBB) [8], current reuse with negative feedback [9], active shunt-feedback [10], shunt feedback with dual capacitive cross-coupling (DCCC) [11], push–pull and current steering with shunt feedback [12]. From the analysis of the existing low-power LNA topologies, it is found that feedback techniques are more suitable for low-power design. Also, in sub-mW designs [4–6, 8, 10, 12], it can be noted that the noise figure (NF) less than 3 dB is difficult to achieve. In [9], low NF is achieved by sacrificing linearity and in [11], the extra transistors will lead to process and device mismatch deterioration. Hence, it is beneficial to develop techniques that will help in achieving sub-3 dB NF in sub-mW operation without deterioration in process and device mismatches.

One of the techniques for noise cancellation is using feedback. Some of the other LNA topologies employing feedback are reported in [6, 9–21] and they include active-feedback [13], resistive-feedback [14], dual negative feedback [15], local feedback [16], negative feedback [17], positive feedback [18], double feedback [19], dual capacitor cross-coupled feedback with negative impedance [20], and active-feedback using complementary source follower (CSF) [21]. It can be seen that by using feedback, the trade-off between input matching, gain, noise figure and transconductance (g_m) of the input transistor is reduced. In CG based LNAs, input impedance, $Z_{in} \approx 1/g_m$. By employing current feedback, Z_{in} can be reduced by a factor of $(1 + A_{v,CG})$, such that $Z_{in} \approx 1/(1 + A_{v,CG})g_m$. Hence, g_m of the CG transistors can be lowered to achieve the required input impedance, thus leading to reduced power consumption. Also, it can be noted that the g_m is now boosted by a factor of $(1 + A_{v,CG})$ leading to improved gain and noise performance of the CG based LNAs employing feedback. In sub-mW LNA designs, it is difficult to simultaneously achieve proper NF and linearity performance. Since, NF

and linearity performance is vital for portable electronic devices, in this paper, an ultra-low power LNA topology employing cross-coupled positive feedback and dual shunt peaking is proposed. It will be shown that the proposed LNA topology provides a scaling factor of $(1 + A^2)$ thus achieving proper gain, NF and linearity performance required by the IEEE 802.15.4 standard for WPAN applications while operating at extremely low supply voltages.

The topology of the proposed LNA is discussed in the Sect. 2, where the expressions for gain, noise figure and linearity are derived. The proposed LNA's post-layout performance is validated using UMC 180 nm CMOS process, and the results are discussed in the Sect. 3 and Sect. 4 concludes the work by highlighting the salient features.

2 Proposed low-noise amplifier topology

Before proceeding to the main theme of this work, a brief background on the use of positive feedback is illustrated in Fig. 1a. The feedforward network has a gain A and the feedback network has a gain β . The difference between the input signal (V_{in}) and the feedback signal is the error signal (V_e). The characteristics of positive feedback in circuits and its subsequent effect on impedance and gain has been reported in [22–26]. In Fig. 1b, conceptual illustration of output voltage sensing and input current returning amplifier is shown. The gain of the feedforward network is a resistance (R_o) and the gain of the feedback network is a transconductance (g_{mf}). It can be seen that the input impedance of the amplifier is reduced by the current returning mechanism of the feedback network. The proposed LNA with positive feedback is shown in Fig. 1c. The input RF signal (v_{rf}) is sensed at the source node of transistors M_1 and M_3 and the necessary bias for these transistors is given by V_{bias} . The transistors M_2 and M_4 are the cascode transistors whose bias (V_{cas}) is used to control the current consumption in the circuit. The resistor R is the biasing resistor and C_c is the coupling capacitor. The transistors M_{f1} and M_{f2} are connected to the source of the transistors M_1 and M_3 respectively, and their output resistances ($r_{o,Mf1}$ and $r_{o,Mf2}$) provide degeneration to the transistors M_1 and M_3 . M_{f1} and M_{f2} also provide the necessary phase shift for positive feedback operation of the circuit. The inductors L_1 and L_3 are present at the drain node of transistors M_1 and M_3 respectively to provide shunt peaking. The inductors L_2 and L_4 are connected to the drain of the cascode devices M_2 and M_4 to act as both the load and the shunt peaking impedance. The shunt peaking inductors $L_{1,3}$ help in tuning out the parasitic capacitance at the drain node of transistors $M_{1,3}$. The second pair of peaking inductors $L_{2,4}$ tune with the capacitors at the drain node of $M_{2,4}$. In wideband LNA with shunt peaking, the inductors are

Fig. 1 **a** Positive feedback network, **b** sensing and return mechanism of the proposed topology, **c** proposed LNA with cross-coupled positive feedback with dual shunt peaking

chosen to add a zero and not to tune with the capacitors. The same inductors when used to tune capacitances can yield good narrowband response and hence used in this work. The amplified differential output (v_{out+} and v_{out-}) is sensed at the drain node of the cascode devices M_2 and M_4 , and the differential output is fed back through the feedback transistors M_{f2} and M_{f1} respectively by means of cross-coupling.

The use of cross coupling provides the necessary phase shift without requirement of external circuitry. This method is more economical in terms of power and area and hence adopted in this work. The inductive load removes the voltage headroom difficulty and enable the circuit to operate at even 0.6 V. Ideally, the inductors remove the voltage headroom difficulty. However, the parasitic resistances cause few micro-volt drop and this drop in voltage is generally small and doesn't affect the performance of the system substantially. Hence, the effect of parasitic resistances are ignored in the simulation. The inherent positive feedback to the output which effectively boosts the g_m by a factor of $(1 + A^2)$ helps in achieving the required performance of the LNA at low supply voltages. In [18], separate transconductance stage is used for

generating positive feedback while in the proposed work the positive feedback is inherently generated by making use of the active source degenerators. As per the equation for closed loop gain in positive feedback from Fig. 1a, $\frac{v_{out}}{v_{in}} = \frac{A}{1 - A\beta}$, we have magnitude of closed-loop gain $|A_{CL}| \approx \frac{1}{\beta}$, when $A\beta \gg 1$. And if $\beta \gg 1$, $|A_{CL}|$ will always be less than 1 and the positive feedback will not be dominant. In this work, clearly feedback factor is $\gg 1$ and hence, the system is stable. Also, it is worth noting that the source and bulk of the input transistors are tied together to eliminate body effect. This is achieved by using triple well transistors offered by UMC. However, due to process and device mismatches, body effect may be prevalent and hence its effect is included in the analysis for completeness in this work. The effect of the cross-coupled positive feedback and dual shunt peaking on the circuit's performance is analysed next.

2.1 Gain analysis

From the circuit schematic shown in Fig. 1c, the proposed circuit is analysed using the small-signal analysis to obtain

the expression for mid-band gain. For calculating the dominant poles and zeros associated with the circuit, open-circuit time constant (OTC) analysis is carried out. From Fig. 1c, the mid-band gain without feedback (A_v) can be derived as

$$A_v \approx \frac{(g_{m,M1,3} + g_{mb,M1,3})}{1 + (g_{m,M1,3} + g_{mb,M1,3})r_{o,Mf1}} \cdot (Z_{L2,4} || R_{down}) \quad (1a)$$

where $g_{m,M1,3}$ —transconductance due to the gate to source voltage of the transistors $M_{1,3}$, $g_{mb,M1,3}$ —transconductance due to the bulk to source potential of the transistors $M_{1,3}$, $Z_{L2,4}$ —inductive impedance offered by the shunt peaking inductor, and R_{down} —resistance looking down from the drain node of the cascode device.

Similarly, the gain with feedback can be derived by considering the gains offered by path due to transistors M_{f1} and M_{f2} respectively. By achieving proper symmetry, the proposed circuit will have $g_{m,Mf1} = g_{m,Mf2}$, and $Z_{L1} = Z_{L2}$. Therefore, with feedback, the gain of the proposed LNA ($A_{v,fb}$) is derived as

$$A_{v,fb} \approx A_v \cdot \left(1 + g_{m,Mf1,2}^2 (Z_{L2,4} || R_{down})^2\right) \quad (1b)$$

By comparing (1a) and (1b), it can be noted that the gain with feedback $A_{v,fb}$ has a square dependence on the transconductance of the feedback transistors $g_{m,Mf1,2}$. In existing feedback techniques, the gain is improved by a factor of $(1 + A)$, whereas in this work, the gain is improved

by $(1 + A^2)$. Therefore, high gain can be achieved at low-power consumption.

The expression for R_{down} is derived using small-signal analysis as

$$R_{down} \approx (g_{m,M2,4} + g_{mb,M2,4}) \cdot r_{o2,4} \cdot [Z_{L1,3} + (g_{m,M1,3} + g_{mb,M1,3}) \cdot r_{o1,3} \cdot r_{oMf1,Mf2}] \quad (2)$$

In (2), $g_{m,M2,4}$ —transconductance due to the gate to source voltage of the transistors $M_{2,4}$, $g_{mb,M2,4}$ —transconductance due to the bulk to source potential of the transistors $M_{2,4}$, $r_{o2,4}$ —output resistance of the cascode transistors $M_{2,4}$, $Z_{L1,3}$ —inductive impedance offered by the shunt peaking inductors L_1 and L_3 , $r_{o1,3}$ —output resistance of the input transistors $M_{1,3}$, and $r_{oMf1,Mf2}$ —output resistance of the feedback transistors M_{f1} and M_{f2} respectively.

Since R_{down} is quantitatively very large as derived in (2), the expression for the mid-band gain of the circuit can be simplified as

$$A_{v,fb} \approx \frac{(g_{m,M1,3} + g_{mb,M1,3})}{1 + (g_{m,M1,3} + g_{mb,M1,3})r_{o,Mf1}} \cdot Z_{L2,4} \cdot (1 + g_{m,Mf1}^2 (Z_{L2,4})^2) \quad (3)$$

For high-frequency analysis, the expression for gain as a function of frequency in radians (ω) is given as

$$A_{v,fb}(\omega) \approx A_{v,fb} \cdot H(\omega) \quad (4)$$

In (4), $H(\omega)$ is found using OTC analysis using the equivalent circuit in Fig. 2 and, the expression for the frequency response of the proposed LNA is derived as

Fig. 2 Equivalent half-circuit of the proposed LNA. **a** TC with node-1, **b** TC with node-2, **c** TC with output node-3, **d** Noise sources in the LNA

$$A_{v,fb}(\omega) \approx \frac{\frac{(g_{m,M1,3} + g_{mb,M1,3})}{1 + (g_{m,M1,3} + g_{mb,M1,3})r_{o,Mf1}} \cdot Z_{L2,4} \cdot (1 + g_{m,Mf1}^2 (Z_{L2,4})^2)}{\left[r_{o,Mf1} \parallel \frac{R_{p,L1}}{g_{m,M1} + \frac{1}{r_{o,M1}}} \right] \cdot [c_{gs,M1} + c_{sb,M1} + c_{gs,Mf1} + c_{db,Mf1} + c_{gd,Mf1} \left(2 + \frac{1}{g_{m,Mf1} \cdot r_{o,Mf1}} + g_{m,Mf1} \cdot r_{o,Mf1} \right)] + (c_{gs,M2} + c_{sb,M2}) \cdot \left(\frac{1}{g_{m,M2} + g_{mb,M2}} \parallel (R_{p,L1} + (g_{m,M1} r_{o,M1} r_{o,Mf1})) \right) + (c_{gd,M1} + c_{db,M1}) \cdot (R_{p,L1} \parallel (g_{m,M1} r_{o,M1} r_{o,Mf1})) + (c_{gd,M2} + c_{db,M2}) \cdot R_{down}} \quad (5)$$

Thus, (5) is the quantified expression for the frequency response of the proposed LNA. It can be noted that the shunt peaking inductor $L_{2,4}$ contributes a zero while the parasitic resistance of the shunt inductor $L_{1,3}$ contributes to the pole frequency. Since, the parasitic resistance, $R_{p,L1} \ll Z_{L2,4}$, the effect of $Z_{L2,4}$ is comparatively dominant and hence, results in a -3 dB bandwidth (BW) extension up to 600 MHz as shown in the next section.

2.2 Noise figure analysis

The equivalent half-circuit with noise contributing sources is shown in Fig. 2d. For the analysis, flicker noise and thermal noise contributed by the MOS devices are considered. The equations for flicker noise and thermal noise is based on the models reported in [3]. Based on the equivalent circuit, the output noise ($\widehat{V_{o,n}^2}$) contribution by the proposed LNA can be given as

$$\widehat{V_{o,n}^2} = \widehat{V_{o,M1}^2} + \frac{\widehat{V_{o,M2}^2}}{a_{v,M1}^2} + \widehat{V_{o,Mf1}^2} \quad (6)$$

where

$$a_{v,M1} \approx (g_{m,M1} + g_{mb,M1}) \cdot \left(r_{o,M1} \parallel \left(Z_{L1} + \frac{1}{g_{m,M2} + g_{mb,M2}} \right) \right) \quad (7)$$

$$\widehat{V_{o,M1}^2} = \left(\frac{8kT}{3} g_{m,M1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 \quad (8)$$

$$\widehat{V_{o,M2}^2} = \left(\frac{8kT}{3} g_{m,M2} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 \quad (9)$$

$$\widehat{V_{o,Mf1}^2} = \left(\frac{8kT}{3} g_{m,Mf1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 \quad (10)$$

$\widehat{V_{o,M1}^2}$ is the noise contributed by the input transistor M_1 , $\widehat{V_{o,M2}^2}$ is the noise contributed by the cascode transistor M_2 , $\widehat{V_{o,Mf1}^2}$ is the noise contributed by the current source M_{f1} , k is Boltzmann's constant, T is the temperature in Kelvin, k_f is flicker noise coefficient, αf is technology parameter,

I_D is the current through the transistor, C_{ox} is the gate-oxide capacitance, W is the width of the transistor, and L is the length of the transistor. From (6) and (7), it can be seen that the overall noise contribution is affected by the shunt inductor Z_{L1} . The presence of Z_{L1} is also responsible for the frequency-dependent characteristic of the NF as discussed in the next section. By substituting (7)–(10) in (6), and dividing the output noise contribution ($\widehat{V_{o,n}^2}$) by $A_{v,fb}^2$, the input-referred noise ($\widehat{V_{i,n}^2}$) can be derived as

$$\widehat{V_{i,n}^2} \approx \frac{\left(\frac{8kT}{3} g_{m,M1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 + \frac{\left(\frac{8kT}{3} g_{m,M2} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2}{\left[(g_{m,M1} + g_{mb,M1}) \cdot (r_{o,M1} \parallel (Z_{L1} + \frac{1}{g_{m,M2} + g_{mb,M2}})) \right]^2} + \frac{\left(\frac{8kT}{3} g_{m,Mf1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 + \left(\frac{16KT}{R_{p,L1-4}} \right) \cdot R_{out}^2}{(A_{v,fb})^2} \quad (11)$$

Thus, from (11), for a source resistance R_s , the NF of the proposed LNA can be quantified as

$$NF \approx 1 + \frac{\left(\frac{8kT}{3} g_{m,M1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 + \frac{\left(\frac{8kT}{3} g_{m,M2} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2}{\left[(g_{m,M1} + g_{mb,M1}) \cdot (r_{o,M1} \parallel (Z_{L1} + \frac{1}{g_{m,M2} + g_{mb,M2}})) \right]^2} + \frac{\left(\frac{8kT}{3} g_{m,Mf1} + \frac{k_f \cdot I_D^{\alpha f}}{C_{ox}^2 WL} \right) \cdot R_{out}^2 + \left(\frac{16KT}{R_{p,L1-4}} \right) \cdot R_{out}^2}{(A_{v,fb})^2 \cdot (4KTR_s)} \quad (12)$$

From the above expression, the effect of the inductors on NF performance can be observed. The inductors in the proposed LNA will have parasitic series resistances which contribute noise, and hence their noise contribution is also included in the analysis. The parasitic series resistance associated with the inductors is denoted as $R_{p,Li}$, and each resistor will contribute a noise current of $(4KT/R_{p,Li})$. Since we have four inductors in the circuit, the total noise current is equal to $(16KT/R_{p,L1-4})$. Also, the transconductance of transistors $M_{1,3}$ also plays a significant role in reducing NF. It should be noted that the noise contribution is scaled down by a factor of $(1 + A^2)$, thus enabling low NF even at reduced supply voltages. The proposed LNA is analysed for linearity performance using Volterra series expansion in the next sub-section.

2.3 Linearity analysis

The nonlinearity of RF circuits arises because of the nonlinear current–voltage relationship of the MOS (metal–oxide–semiconductor) devices. The nonlinearity behaviour of the RF CMOS circuits in deep sub-micron technologies is extensively studied and reported in [27–35]. For memoryless systems, the nonlinear output current (i_d) as a function of the gate to source voltage (v_{gs}) can be expanded using Taylor series as

$$i_d = g_m^1 v_{gs} + g_m^2 v_{gs}^2 + g_m^3 v_{gs}^3 + \dots + g_m^n v_{gs}^n \quad (13)$$

where g_m^n is the n th-order transconductance and it is expressed as

$$g_m^n = \frac{1}{n!} \cdot \frac{\partial^n}{\partial v_{gs}^n} (i_d) \quad (14)$$

The MOS devices have various capacitances associated with them, and the capacitive reactance is frequency-dependent. Hence, the nonlinear output expression must include the frequency-dependent components for accurate analysis and therefore, Volterra series expansion is used [27, 36–38]. The expression for Volterra series expansion of v_{gs} due to an input signal v_{in} restricted up to third-order can be given as

$$v_{gs} = A_1(s_1) \circ v_{in} + A_2(s_1, s_2) \circ v_{in}^2 + A_3(s_1, s_2, s_3) \circ v_{in}^3 \quad (15)$$

where $A_1(s_1)$, $A_2(s_1, s_2)$ and $A_3(s_1, s_2, s_3)$ are the Laplace transforms of the first-, second-, and third-order Volterra kernels. ‘ $\circ$ ’ is the volterraa operator. Combining (13) and (15), the output drain current i_d can be expressed as a function of the input signal v_{in} as

$$i_d(v_{in}) = B_1(s_1) \circ v_{in} + B_2(s_1, s_2) \circ v_{in}^2 + B_3(s_1, s_2, s_3) \circ v_{in}^3 \quad (16)$$

In (16), $B_1(s_1)$, $B_2(s_1, s_2)$ and $B_3(s_1, s_2, s_3)$ are determined in terms of first-, second-, and third-order terms of (13) respectively. If Z_{in} is the input impedance, then the input-referred third-order intercept point (IIP3) can be found by solving for the unknowns in (13)–(16). The expression for IIP3 using Volterra kernels has been studied extensively [27, 36]. The dominant source of nonlinearity in the circuit is due to the transistors $M_{1,3}$ and it is considered in this work. From [39], the expression for IIP3 in circuits having frequency-dependent components can be expressed as

$$IIP3 = \frac{1}{6\Re(Z_{in}(s))} \left| \frac{g_m^1 A_1(s)}{|A_1(s)|^2 [1 - g_m^1 A_1(s) Z_s] \epsilon} \right| \quad (17)$$

In (17), the expression for variables $Z_{in}(s)$, $A_1(s)$, Z_s and ϵ are derived for the proposed LNA given in Fig. 1 and are as follows:

$$Z_{in}(s) \approx \frac{\left(\frac{1}{g_{m,M1}} || r_{o,M1}\right) || (r_{o,Mf1} || X_c)}{\left(1 + \frac{R_T}{r_{o,M1}}\right)} \quad (18)$$

$$Z_s \approx r_{o,Mf1} || X_c \quad (19)$$

$$A_1(s) \approx \frac{\omega c_{gs} + r_{o,Mf1}}{2g_m^1 \omega c_{gs} r_{o,Mf1}} \quad (20)$$

$$\epsilon \approx \frac{g_m^3 - \frac{2}{3}(g_m^2)^2}{\frac{1}{2r_{o,Mf1}} - 2\omega c_{gs} r_{o,Mf1} + g_m^1} \quad (21)$$

In (18), R_T is the resistance connected to the drain of transistor M_1 and derived as

$$R_T \approx \frac{Z_{L2}}{r_{o,M2} \left(\frac{1}{g_{m,M2}} || r_{o,M2}\right)} + Z_{L1} \quad (22)$$

In (19), Z_s is the impedance connected to the source of the transistor M_1 and X_c denotes the reactance of the gate to source capacitance c_{gs} . Therefore, by using the expressions derived in (18)–(22), the IIP3 of the proposed LNA including the frequency-dependent components is derived as

$$IIP3 = \frac{g_m^1 \frac{\omega c_{gs} + r_{o,Mf1}}{2g_m^1 \omega c_{gs} r_{o,Mf1}} \cdot \left(\frac{1}{2r_{o,Mf1}} - 2\omega c_{gs} r_{o,Mf1} + g_m^1\right)}{6 \left(\frac{1}{g_{m,M1}} || r_{o,M1}\right) || (r_{o,Mf1} || X_c) \cdot \frac{\omega^2 c_{gs}^2 + r_{o,Mf1}^2 + 2\omega c_{gs} r_{o,Mf1}}{4\omega^2 (g_m^1)^2 (r_{o,Mf1})^2 c_{gs}^2} \cdot \left[1 - g_m^1 \frac{\omega c_{gs} + r_{o,Mf1}}{2g_m^1 \omega c_{gs} r_{o,Mf1}}\right] \cdot \left(g_m^3 - \frac{2}{3}(g_m^2)^2\right)} \quad (23)$$

From (23), it can be seen that the IIP3 is dependent on the frequency, and IIP3 increases with an increase in spacing between the fundamental signal and the interferer.

3 Results

The proposed LNA is designed using UMC 180 nm mixed-mode radio frequency (MMRF) CMOS process technology. The performance of the LNA with extracted parasitic RC components is studied using Cadence SpectreRF circuit simulator. For analysis, the input signal power is set at –85dBm because the minimum receiver sensitivity required for WPAN applications is –85dBm [1–3]. The gain offered, and the noise contributed by the LNA are analysed using S-parameter analysis and the results are plotted

Fig. 3 Gain and input matching of the LNA

Fig. 4 NF of the LNA

in Figs. 3 and 4 respectively for the targeted frequency range of 2.4–2.485 GHz. It can be observed that the LNA offers a peak gain of 18.87 dB and 21.36 dB when operating in Mode-I and Mode-II respectively. In Mode-I, the LNA has a 3 dB bandwidth of 600 MHz from 2.3 to 2.9 GHz whereas in Mode-II, its bandwidth is 500 MHz from 2.3 to 2.8 GHz. Also, the input matching of the LNA is analysed using the S11 parameter and is shown in Fig. 3. It can be found that the LNA provides proper input matching and the proposed LNA has a flat S11 of –11 dB in the required operating frequency range of 2.4–2.485 GHz. The small signal g_m changes with change in small signal current. For DC conditions, it is possible to fix g_m independent of the current given by the equation $[k_L^W(V_{GS} - V_{TH})]$. In the equation, g_m is independent of the current. In this work, the

Fig. 5 Variation of $g_{m,M1}^1$ and $g_{m,M1}^3$ with V_{bias} Fig. 6 Variation of $g_{m,M2}^1$ and $g_{m,M2}^3$ with V_{cas}

source of the transistor is degenerated with an inductor and hence, V_s does not change and therefore, g_m does not change. Although, the inductors will have parasitic series resistance, the voltage drop is very small and can be negligible. Thus, with change in supply voltage, in this topology, the effect on change in g_m is negligible and hence, S11 is almost the same as shown in Fig. 3.

In Mode-I, the LNA has NF of 3.2–2.5 dB in the range of 2.3–3 GHz, and in Mode-II, the LNA has NF of 2.9–2.3 dB in the frequency range of 2.3–3 GHz. The NF of the proposed LNA is better than the other sub-mW designs reported in [4–6, 8–12, 18]. Also, it is worth noting that the LNA has a wide unity-gain bandwidth (UGB) ranging from 1.5–6 GHz in Mode-I, and 1.4–6.5 GHz in Mode-II respectively. In (3), (5), and (12), the parameters affecting the gain and NF is determined and to assist the design, the variation of the design parameters with bias voltage is plotted in Figs. 5 and 6. In Fig. 5, the effect of the gate voltage (V_{bias})

of transistors $M_{1,3}$ on the transistor's first-order transconductance g_m^1 and the second-derivative of the transconductance g_m^3 is shown for both Mode-I and Mode-II respectively. Similarly, the effect of the gate bias voltage (V_{cas}) of the transistors $M_{2,4}$ on the transistor's g_m^1 and g_m^3 is shown in Fig. 5. In Mode-I, the LNA operates at a supply voltage of 0.6 V whereas, in Mode-II, the LNA operates at 1 V supply. From (3), (5), and (12), it should be noted that the gain is enhanced by a factor of $(1 + A^2)$ whereas the NF is scaled down by a factor of $(1 + A^2)$. This is achieved by the positive shunt feedback topology of the proposed LNA.

IIP3 in dB calculated based on Taylor series approximation is given by $\sqrt{\frac{4}{3} \cdot \frac{g_m^1}{g_m^3}}$. By definition, making $g_m^3 \approx 0$, increases IIP3. To assist in the design process, the variation of transconductance (g_m^1) and the second derivative of transconductance (g_m^3) with respect to the gate bias voltage of the transistor $M_{1,3}$ is shown in Fig. 6. It can be seen from Fig. 5 that in Mode-I, g_m^3 is much closer to 0 than in Mode-II. Thus, it is expected that the IIP3 in Mode-I will be greater than the IIP3 in Mode-II. In Fig. 5, around 600 mV, g_m^3 of input transistor is near to zero and hence the IIP3 can be enhanced.

However, IIP3 depends on various other parameters such as Z_{in} , parasitic capacitors (17)–(23), and therefore, the IIP3 is swept as a function of the input transistor bias voltage in Fig. 8, where maximum IIP3 is obtained at 550 mV. It can be noted that the input transistor dominates the distortion more than the cascode as the cascode transistor can be viewed as a common-gate transistor where the signal path due to $c_{gs,M3}$ is grounded. The linearity of the RF circuits is a pivotal performance parameter in WPAN applications since the circuits are employed in

Fig. 8 IIP3 variation with V_{bias}

the dense 2.4 GHz band where the interferer signal will be closely spaced to the fundamental signal, resulting in intermodulation components (IM) within the frequency band of operation. The linearity performance of the LNA is characterized using IIP3 by harmonic-balance (HB) analysis combined with harmonic-balance AC analysis (HBAC), and the results are shown in Fig. 7. The LNA achieves an IIP3 of -8.4 dBm in Mode-I and 14.5 dBm in Mode-II for the fundamental signal at 2.4 GHz and an interferer spaced 100 MHz away. From (23), the IIP3 depends on g_m^1 and g_m^3 of the transistor $M_{1,3}$ and since, the g_m^1 and g_m^3 depends on the gate bias (V_{bias}), the IIP3 variation with (V_{bias}) is plotted in Fig. 8.

Thus, appropriate gate bias of the transistor $M_{1,3}$ can be chosen for optimal linearity performance of the LNA. It can

Fig. 7 IIP3 performance of the LNA

Fig. 9 Variation of gain with process corners

Fig. 10 Variation of NF with process corners

Fig. 12 Variation of NF with supply voltage

Fig. 11 Variation of gain with supply voltage

Fig. 13 Variation of gain with temperature

be seen that for a gate bias of $\sim 550\text{mV}$, the LNA achieves 13.78dBm IIP3 in Mode-II and in Mode-I, the corresponding IIP3 is -7.9dBm . The IIP3 achieved by the proposed LNA in Mode-II is better than the other sub-mW designs proposed in the literature [4, 8–12, 18].

The reliability of the LNA to operate under diverse operating conditions is studied by conducting corner, voltage, and temperature variation analysis. The LNA performance is characterized at different process corners (FF, FN, SN, SS) for both Mode-I and Mode-II and the results for gain and NF variation are shown in Figs. 9 and 10 respectively. For studying the effect of voltage variation on the performance of the LNA, the supply voltage is varied $\pm 10\%$

from the nominal supply voltage of 0.6V in Mode-I, and 1V in Mode-II. The gain and NF performance of the LNA for supply voltage variation is plotted in Figs. 11 and 12 respectively and finally, the gain and NF performance of the LNA at different operating temperatures (-40°C , 0°C , 125°C) is shown in Figs. 13 and 14 respectively. The corner, voltage, and temperature effects on IIP3 for Mode-I and Mode-II are listed in Tables 2 and 3 respectively. It can be noted from the analysis that the performance of the LNA is intact and within acceptable limits even under diverse operating conditions.

IIP3 is very sensitive to bias voltages, resistances and impedances present in the circuit. This can be seen from

Fig. 14 Variation of NF with temperature

the transconductance variation shown in Figs. 5 and 6. In Mode-I, especially with reduced headroom and

subthreshold region of operation at low-power mode, the sensitivities are enhanced. Nevertheless, the performance characterized by the PVT analysis shows that the LNA is robust to such variations in the operating environment.

To account for the process and device mismatches arising in the fabrication process, the performance parameters of the LNA is analysed using statistical models and Monte-Carlo (MC) simulations. Since the first-order transconductance g_m^1 of the transistors $M_{1,3}$ and $M_{2,4}$ affect the gain, NF and IIP3 of the LNA, the random variation of $g_{m,M1}$ and $g_{m,M2}$ with device parameters are analysed using MC simulations and plotted in Figs. 15, 16, 17 and 18. The MC simulations are carried out for 100 iterations of random variations of the process and device mismatch parameters. The MC simulation results show the mean (μ) and standard deviation (σ) of the parameters. Similarly, MC simulation results for NF and IIP3 in Mode-I and Mode-II are shown in Figs. 19, 20, 21 and 22. The process and device mismatch analysis using MC simulation is performed for both Mode-I and Mode-II respectively. Thus, from the results obtained from the corner, voltage, and temperature variation analyses and MC simulations, it can be concluded that the designed LNA is robust, dependable and reliable for battery-powered,

Table 2 CVT variation of IIP3 in Mode-I

Parameters	Corners				Temperature			Voltage	
	FF	FNSP	SNFP	SS	−40 °C	0 °C	125 °C	0.54 V	0.66 V
IIP3 (dBm)	−8.162	−7.56	−8.529	−4.652	−4.458	−7.246	−6.754	0.702	−3.702

Table 3 CVT variation of IIP3 in Mode-II

Parameters	Corners				Temperature			Voltage	
	FF	FNSP	SNFP	SS	−40 °C	0 °C	125 °C	0.9 V	1.1 V
IIP3 (dBm)	4.525	4.761	2.477	−1.171	−3.941	2.47	5.171	14.62	12.65

Fig. 15 MC analysis of $g_{m,M1}^1$ in Mode-I

Fig. 16 MC analysis of $g_{m,M1}^1$ in Mode-II

Fig. 17 MC analysis of $g_{m,M2}^1$ in Mode-I

Fig. 19 MC analysis for NF in Mode-I

Fig. 18 MC analysis of $g_{m,M2}^1$ in Mode-II

Fig. 20 MC analysis for NF in Mode-II

portable and wearable devices. Since the proposed LNA concentrates on low-power consumption, the characteristics of transconductor efficiency (g_m/I_d), Power, current consumption (I), and Inversion coefficient (IC) of the transistors $M_{1,3}$ and $M_{2,4}$ is plotted with respect to their gate bias voltages V_{bias} and V_{cas} respectively and shown in Figs. 23, 24, 25 and 26. From Figs. 23, 24, 25 and 26, the weak inversion operation of the input transistors $M_{1,3}$ can be seen and the required gate bias for the transistors can be chosen.

For a fair comparison of the proposed LNA with existing LNA topologies, the following figure-of-merit (FoM) is adopted [52].

$$FoM_1 = 10 \cdot \log_{10} \frac{10^{Gain/20} \cdot 10^{IIP3/20}}{10^{NF/10} \cdot P} \quad (24)$$

In sub-mW designs, it is difficult to provide NF less than 4 dB and improve IIP3 simultaneously.

The comparison of the proposed LNA with recently reported low-power LNA topologies [9–12, 20, 21, 40–43] is shown in Table 4. In Table 4, [9, 11, 20, 21, 40–43] are post-layout simulation results. It can be seen that the proposed LNA offers a better alternative for ultra-low power applications. The proposed LNA has a core area of 0.45 mm^2 and the layout of the LNA is shown in Fig. 27 and the size of the devices and component values used in the circuit are listed in Table 5. The inductors used are from the process library provided by UMC and the required

Fig. 21 MC analysis for IIP3 in Mode-I

Fig. 22 MC analysis for IIP3 in Mode-II

diameter, width, number of turns for achieving the inductance value is specified in Table 5. The input and output waveforms are shown in Figs. 28 and 29 for Mode-I and Mode-II respectively. The input signal v_{in} has a peak-to-peak amplitude of $35.14\mu V$ ($\approx -85dBm$ for a 50Ω source impedance) at 2.4 GHz. The output signal v_{out} has a peak-to-peak value of $225\mu V$ for Mode-I and $297.3\mu V$ for Mode-II respectively. For a 50Ω output impedance, the output power will be $-68.97dBm$ and $-66.55dBm$ for Mode-I and Mode-II respectively. The gain plotted in Fig. 3 correlates with the values calculated from the waveform.

While the other feedback topologies rely on external circuits for feedback, the proposed LNA makes use of the active degeneration devices to provide positive feedback. Also, the topologies reported earlier scale up the gain by a

Fig. 23 g_m/I_d of $M_{1,3}$ and Power consumption vs. V_{bias} Fig. 24 g_m/I_d of $M_{2,4}$ and Power consumption vs. V_{cas} Fig. 25 IC and Current consumption of $M_{1,3}$ vs. V_{bias}

Fig. 26 IC and Current consumption of $M_{2,4}$ vs. V_{cas}

factor of $(1 + A)$ while the proposed LNA scales up the gain by $(1 + A^2)$. Thus, the proposed LNA can afford to operate at reduced voltages with reduced power consumption. Compared to the recently proposed LNA in [44], the proposed circuit operates at 55.5% reduced power consumption. Also, the proposed LNA has good performance at reduced supply voltage of 0.6 V making it viable for battery-powered, wireless applications that demand large data processing such as 5G.

Although positive feedback has been employed in [45], the proposed circuit reimagines the circuit for ultra-low-power operation with the use of series peaking inductors. Compared to [45], the proposed LNA design achieves 0.5 dB less NF, 0.96 dB higher gain in Mode-II while consuming only 0.5mW which is 5.3 times lesser in power. An LNA circuit without inductors and capacitors is reported in [46] with power consumption of 18mW. In contrast to the proposed work, the LNA in [46] trades power consumption for lower chip area. LNAs operating at sub-mW power

consumption has been proposed in [47, 48]. Although the power is drastically reduced, the IIP3 of -19dBm in the reported LNA [47] makes it susceptible to large signal interference and inadvertently causes signal blocking or erroneous signal detection. The LNA proposed in this work provides better noise performance over the ultra-low-power LNA reported in [48]. In comparison to the recent state-of-art LNA, the proposed LNA has better gain and NF performance compared to the LNAs in [52, 55]. The proposed LNA topology is more linear than the LNAs in [52–55]. Although the proposed ultra-low-power LNA consumes 50% more power than the LNA in [52], the IIP3 improvement is $\sim 16\text{ dB}$. Whereas the LNAs in [53–55] consume ~ 10 times, ~ 39 times and ~ 35 times more power than the proposed LNA in High-Power mode. Therefore, it is clear that the proposed LNA has improved the state-of-art substantially.

The input signal strength which causes the LNA to compress is characterized using 1 dB-compression point (1 dB-CP). It is found that the 1 dB-CP of the proposed LNA is -18.58dBm for Mode-I and -10.83dBm for Mode-II respectively and the graphs are plotted in Fig. 30. Since the desired signal power will be very low (-85dBm for IEEE 802.15.4 standard), LNA can work without compression. However, in the presence of an interferer, the proposed LNA can withstand an interferer power of -18.58dBm in Mode-I and -10.83dBm in Mode-II. Since the input signal power sensed by the LNA is in the order of -85dBm ($35.56\text{ }\mu\text{V}_{pp}$), the input signal will not affect the operation. The maximum input signal power that can be sensed without causing compression is characterized by the 1 dB-compression point. In the reported work, the 1 dB-CP is obtained at -18.58dBm ($\sim 79\text{mV}_{pp}$) for Mode-I and -10.83dBm ($\sim 200\text{mV}_{pp}$) for Mode-II respectively. Thus, it can be concluded that as long as the input signal level is below the 1 dB-CP, the output signal will not be

Table 4 Comparison of the proposed LNA with literature

	[9]	[11]	[20]	[42]	[48]	[52]	[53]	[54]	[55]	This work
Year	2016	2018	2017	2019	2012	2018	2019	2019	2019	2019
PLS/Meas	PLS	PLS	PLS	PLS	Meas	Meas	Meas	Meas	Meas	PLS
Tech (nm)	180	180	180	180	180	110	65	65	65	180
Supply Voltage (V)	1.8	1.8	1.8	1.8	0.6	0.7	1.4	2.2	1.2	$0.6^a/1^b$
$S_{11}(\text{dB})$	-16	-13	-10	< -10	-22	< -10	-10	-10	< -8.7	-11
Gain (dB)	20.1	16.5	25.02	21	14	14.8	22	30	15.6	$18.87^a/21.36^b$
NF (min.) (dB)	3.2	2.9	2.37	2.38	3.55	3.7	2.4	2.3	2.99	$2.5^a/2.3^b$
IIP3 (max.) (dBm)	-2.4	1	-6.49	8.03	-6.8	-3.7	-2.5	-4.1	-5.7	$-7.9^a/13.78^b$
Power (mW)	1.3	0.985	3.24	4.34	0.5	0.336	5	19.8	18	$0.219^a/0.505^b$
Core Area (mm^2)	0.032	0.045	0.03	1.05	1.2	0.624	0.065	0.0448	0.27	0.45
FoM_1	34.51	35.91	31.78	35.76	33.06	36.58	30.36	27.68	19.40	$39.58^a/48.23^b$

A—Mode-I; b—Mode-II; PLS—Post-layout Simulation; Meas.—Measured

Fig. 27 The physical layout of the proposed LNA with a core area of 0.45mm^2

Table 5 Component values for design

Component	$L_{1,3}$ (nH)	$L_{2,4}$ (nH)	$M_{1,3}$ (μm)	$M_{2,4}$ (μm)	$M_{f1,2}$ (μm)
Value	5	6	200	200	200
Diameter	198 μm	230 μm	–	–	–
Width	6 μm	6 μm	–	–	–
No. of turns	3.5	3.5	–	–	–

Fig. 28 The input and output waveforms for $V_{DD}=0.6\text{ V}$

compressed. The circuit has a common-mode gain (A_{CM}) of -231.86 dB and -229.50 dB in Mode-I and Mode-II respectively as shown in Fig. 31. These A_{CM} values combined with the differential voltage gain gives a common-mode rejection ratio (CMRR) of 250.73 dB and 250.86 dB

Fig. 29 The input and output waveforms for $V_{DD}=1\text{ V}$

Fig. 30 The 1-dB Compression Point for Mode-I and Mode-II

Fig. 31 Common-Mode Gain of the LNA in Mode-I and Mode-II

Fig. 32 The input and output matching characteristics of the proposed LNA

Table 6 Improvement in g_m achieved by the state-of-the-Art LNAs

References	Technique used	g_m Enhancement factor
[13]	Active-feedback	$1 + A_v$
[14]	Resistive-feedback	$1 + A_v$
[15]	Dual negative feedback	$1 + A_v$
[16]	Local feedback	$1 + A_v$
[17]	Negative feedback	$1 + A_v$
[18]	Positive feedback	$1 + A_v$
[18]	Double feedback x	$1 + A_v$
[20]	Dual capacitor cross-coupled feedback with negative impedance	$1 + A_v$
[21]	Active-feedback using complementary source follower (CSF)	$1 + A_v$
This work	Positive feedback	$1 + A_v^2$

for Mode-I and Mode-II respectively. Furthermore, to avoid latch-up in the proposed LNA at high-power mode, guard rings are placed in the layout. The causes and prevention of latch-up in CMOS circuits are studied in [49–51]. For completeness, the S22 characteristics is plotted in Fig. 32 along with S11. The input impedance seen by the signal source is, $Z_{in} \approx 1/g_{m1,3}$ since the values of $C_{gs1,3}$ is very small, and hence the S11 is purely resistive in the required frequency range. The effect of small capacitances will come into effect at higher frequencies outside the band of interest. It is worth mentioning that this LNA is designed for on-chip radio receivers where the output of the LNA is given to the RF Mixer stage. Hence, simulations excluded the use of output buffers since the buffers only add to the NF and degrade the SNR of the receiver system. The

presence of inductive load gives a tuned S22 as shown in Fig. 32.

Finally, Table 6 compares the feedback LNA techniques active-feedback [13], resistive-feedback [14], dual negative feedback [15], local feedback [16], negative feedback [17], positive feedback [18], double feedback [19], dual capacitor cross-coupled feedback with negative impedance [20], and active-feedback using complementary source follower (CSF) [21] with the proposed LNA in terms of the achieved improvement in g_m . Table 6 clearly shows that the proposed LNA doubles the enhancement factor.

4 Impact of technology scaling

Although the proposed topology can be used at lower technology nodes, the impact of technology scaling will be evident as similar performance may be hard to achieve. This is because of the short-channel effects (SCE) like Gate-induced-Drain-Lowering (GIDL), Drain-induced-Barrier-lowering (DIBL), velocity saturation, mobility degradation, gate tunnelling, hot carrier effects, threshold roll-off. However, with appropriate biasing and sizing of the devices along with other circuit techniques (if required), the proposed LNA topology can be implemented in lower nodes like 28 nm and beyond. Thus, making the LNA implementable in lower technology nodes for portable and wearable IoT applications. For example, the effect of velocity saturation, mobility degradation and DIBL can be modelled as follows:

$$g_m = WC_{ox} v_{sat} \quad (25)$$

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH} - DIBL)} \quad (26)$$

$$DIBL = 0.80 \frac{\epsilon_{si}}{\epsilon_{ox}} \left[1 + \frac{x_j^2}{L_{el}^2} \right] \cdot \frac{t_{ox}}{L_{el}} \cdot \frac{t_{dep}}{L_{el}} \cdot V_{bi} \quad (27)$$

where ϵ_{si} , ϵ_{ox} are the permittivity of Silicon and Oxide layers, t_{ox} is the thickness of the oxide layer, t_{dep} is the depletion thickness, L_{el} is the effective length, x_j is the source/drain junction width, V_{bi} is the built-in potential. θ is a proportionality factor and v_{sat} is the saturation velocity. The parameters vary for every technology node and is generally specified by the foundry. Using the general equations and EDA tools, the circuits can be simulated and analysed. It is to be noted that with increasing complexity, the equations only give a general idea about the design. Therefore, the equations for voltage gain, NF and IIP3 derived in (5), (12) and (23) are now functions of SCE. Due to the complexity of the equations, analysis and design of the LNA

can be carried out with EDA tools. In this work, Cadence SpectreRF is used for complex circuit simulations.

As an end note, with miniaturization of electronic devices especially for smart wearables in IoT and health-care applications, the supply voltage is also reducing with technology scaling and for better battery life. For instance, with 5 nm process node, the supply voltage is 0.6 V. The intent of providing two modes of operation is to enable the customer to use the proposed topology in various end user applications as deemed beneficial by the product manufacturers. In the industry, it is a common practice to have two or more gain modes for the LNA. The gain of the LNA affects the NF and linearity of the RF front-end circuits. With having variable gain modes for the LNA, the use of variable gain amplifier can be reduced which will further improve the size of the receiver system. Also, by showing that the LNA can operate at two different modes, the LNA can cater to a wide customer base.

5 Conclusion

An ultra-low power LNA topology is proposed in this work for use in battery-powered, portable, wireless devices such as Internet-of-Things. The LNA with cross-coupled positive feedback and dual shunt peaking is implemented in UMC 180 nm CMOS process, and it can be operated in two modes namely, low power mode and high power mode. In low power mode, the LNA is operated at a reduced supply voltage of 0.6 V and offers 18.87 dB gain, whereas, in high power mode, the LNA is operated at 1 V supply and offers a gain of 21.36 dB and IIP3 of 13.78 dBm. With the semiconductor industry approaching 5 nm technology node in the near future, the applications such as Internet-of-Things need to be powered by low-voltage, low-power RF circuits. With 219 μ W of power consumption, the proposed LNA offers an alternative to be used in the next generation communication systems. The proposed LNA offers better FoM when compared to other recently reported low-power LNA topologies. Thus, it can be concluded that the proposed LNA is a suitable alternative for low power, low voltage applications.

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Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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