Implementation of parallel computing and adiabatic logic in full adder design for ultra-low-power applications

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Abstract

In this work, the idea of parallel computing for a full adder has been proposed. Based on parallel computing, a new architecture of full adder (A-I) has been proposed in which the input needs to pass through only two transistors to reach the output node which results in reduced delay time. The second design of full adder (A-II) has been proposed with two-phase clocked adiabatic static complementary metal oxide logic which results in decreased power dissipation. The third design of full adder (A-III) uses parallel computing for both sum and carry generation. In A-III, a buffer has been introduced to restore the logic level which proves the drive capability of parallel computing logic. The adiabatic logic-based proposed design A-II shows a 61.95% improved power delay product (PDP) as compared to the best-reported body biasing approach-based adder, whereas the fully parallel computing-based design A-III shows a 53.29% improved PDP as compared to double pass transistor-based full adder. Post layout results of the proposed design A-III verified the functionality of proposed parallel computing logic. The proposed designs also perform well under varied temperature conditions. These designs show satisfactory performance at low voltages, whereas the use of adiabatic logic makes these designs energy efficient for low power applications.

Keywords Adiabatic logic · Energy efficiency · Low power adder · Parallel computing · Power delay product

1 Introduction

Energy efficiency with high speed in low-power ultra-large-scale integrated circuits has attracted the attention of researchers in the nanometer regime according to [1], as this is the prime need for modern electronic devices to prolong the battery life. The feature size of metal oxide semiconductor devices is improving (miniaturization) day by day consequently. With improved scaling in deep sub-micrometer regime, leakage current is becoming considerable, as it contributes a sizable fraction to the total power dissipation of a chip mentioned in [2]. The low-power electronic industry is progressing by leaps and bounds with the high demand for portable electronic devices. These devices consist of high-speed data processors that perform complex operations employing MOS as

fundamental blocks. Large-scale industrial automation, space applications, image processing, modern warfare industry, biomedical implantable devices, and other modern miniaturized electronic devices consist of digital signal processing (DSP) units [3]. These units are used to perform arithmetic and logical operations utilizing multiplier and high-speed adders. Therefore, the selection of adder topologies becomes the prime concern for the designer to make the system energy efficient with high speed, particularly in multipliers. Various increasing limitations of decreasing nanometer technologies have attracted the researcher's attention to the search for new hybrid circuits and techniques for electronic devices. The adiabatic logic technique is one of the prominent techniques of power reduction [4]. In the literature, various techniques have been reported which are used to implement the

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adders for modern electronic systems. Some have limitations of the area, and some other has limitations of delay, capacitance, and swing in output voltage [5]. Conventional static CMOS-based circuits occupy a large area of the chip and increased leakage currents with improved scaling. A hybrid adder based on complementary pass transistor (CPL) logic has been reported in [6]. In this circuit, the first part consists of X-OR/ X-NOR which consists of NMOS with one inverter. Reduced delay in this circuit is advantageous, but it dissipates more power as in [7] and [8]. An approximate 4–2 compressor circuit has been reported in [9] which reduces the number of adders required, but approximate compressors are erroneous. A fourth passive element memristor-based adder has been presented in [10] with some constraints such as commercial availability and speed as compared to MOS devices. Another hybrid full adder with a strong driver and good voltage swing has been reported in [11]. However, the functioning of hybrid adders requires less power, but their decreased speed and increased number of transistors become a constraint for high-frequency computations [7]. In this paper, the novelty of these new proposed designs of full adder circuits is based on parallel computing. These adders compute the sum parallelly which results in very high speed with reduced power dissipation. In A-I, carry is separately computed with three transistors-based X-OR gate [12] and multiplexer (MUX). In the second design A-II, two-phase clocked adiabatic static CMOS logic (2PASCL) [13] has been used, whereas A-III computes carry and sum both parallel.

2 Fundamental concepts and related terminologies

2.1 Mechanism of power dissipation in a CMOS

There are three dominant sources of power dissipation in a MOS device, which are responsible for the draining of the battery. This dissipated power further increases the temperature of the integrated circuits. This increased temperature affects the performance of the device in ON and OFF states [14] and [15].

Total power dissipation in a MOS device is the combination of these three components [16].

- Dynamic power dissipation
- Short circuit power dissipation
- Static power dissipation.

$$P_T = P_D + P_{SC} + P_S \quad (1)$$

where P_T is the total power dissipation of a MOS device.

Fig. 1 Basic structure of full adder

Table 1 Truth table of full adder

A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.2 Logical composition of full adder

Logically the architecture of full adder consists of three blocks as shown in Fig. 1. It consists of three modules: the first module consists of X-OR/X-NOR gates and second consists of X-OR/X-NOR/multiplexer (MUX) which gives a final sum with a MUX for carry generation. Functionally full adder has three inputs bits (A, B, Cin) and gives two outputs sum and carry out as shown in Fig. 1. Truth “Table 1” represents all possible three-bit combinations of A, B, and, Cin as input with sum and carry as output for a full adder. The basic functionality of a full adder in terms of its input and outputs is governed by the following equations.

$$Sum = A \oplus B \oplus Cin \quad (2)$$

$$Carry = \overline{(A \oplus B)} \times C + (A \oplus B) \times A \quad (3)$$

2.3 Adiabatic logic and 2PASCL

Adiabatic fundamentally represents the recycling of stored charge at capacitive nodes. For charging and discharging of a conventional CMOS inverter, the output node capacitance (C) needs some energy equivalent to CV_{dd}^2 from the power supply where V_{dd} is the supply voltage. Half of this energy $1/2 CV_{dd}^2$ is stored by the node capacitance, and the rest half

is dissipated by the PMOS ON state resistance during the charging of node capacitance [4]. The stored energy in node capacitance goes to the ground through NMOS during the discharging process and wasted away, whereas in adiabatic logic circuits, this stored energy recycled back to the power supply which decreases power consumption. Charging and discharging adiabatically can be represented by an RC model as shown in Fig. 2.

The node capacitance in this RC model is represented by C which is charged through a MOS transistor, whereas R represents the ON-state resistance of MOS with a constant current source $I(t)$ which is used to charge the capacitance instead of a fixed voltage V_{dd} in CMOS inverter. Assuming the initial charge on the capacitor is zero then the voltage across capacitor $V_c(t)$ is given by the following expression

$$V_c(t) = \frac{1}{C} i(t) * t \quad (4)$$

and,

$$i(t) = C \frac{V_c(t)}{t} \quad (5)$$

The energy dissipation can be approximated by the following equation

$$E_{diss} = R \int_0^T i^2(t) dt = R i^2(t) * T = \frac{RC}{T} C V_c^2(T) \quad (6)$$

where $V_c(T)$ is the voltage across the capacitor for time T . It is depicted from "Eq. (6)" that the energy loss can be decreased by keeping $T > 2RC$ as compared to conventional charging at V_{dd} supply voltage. Further, the energy loss can be minimized by reducing R and by using a slowly time-varying voltage supply, i.e., by increasing T .

The operation of basic CMOS inverter using 2PASCL [13] can be explained with the help of Fig. 3. Here, two extra MOS transistors are used with complementary power supply clocks PC and $\overline{PC}$. Both power clock supplies are complementary with each other, and the voltage magnitude of both power clock supplies is governed by "Eqs. (7) and (8)" [13].

$$V_{PC} = \frac{V_{DD}}{4} \sin(\omega t + \theta) + \frac{3}{4} V_{DD} \quad (7)$$

Fig. 3 a 2PASCL-based inverter b Power clock supplies

$$V_{\overline{PC}} = \frac{V_{DD}}{4} \sin(\omega t + \theta) + \frac{1}{4} V_{DD} \quad (8)$$

The magnitude of $V_{PC} V_{\overline{PC}}$ is twice of $V_{PC} V_{\overline{PC}}$ to reduce the voltage difference between the electrodes which results in decreased power dissipation. In the proposed circuit split level clock supply charges/discharges the load capacitance slowly as compared to other clock pulse used in adiabatic logic. This also minimizes energy loss. The operation of this circuit is divided into two steps, i.e., evaluation and hold.

- During evaluation when output is low and pull-up network turns ON, the load capacitance C_L charged through PMOS and output goes HIGH. When the output is high and pull-down network turns ON, discharging of load capacitance takes place via NMOS and D_2 .
- In the hold step, if no transition takes place at the input side, the output will be held by the load capacitance, consequently, reduces switching activity and results in decreased energy loss.

3 Proposed work and logical composition of full adder

The proposed logical structure of the full adder is shown in Fig. 4. The sum has been computed in a single module without any gate as compared to the conventional three-module approach as shown in Fig. 4a. Carry generation has been achieved separately by using the conventional method with the X-OR gate and with adiabatic logic circuit also following the logical structure given in Fig. 4b. In A-II, adiabatic logic has been used to increase the power efficiency. Two more transistors have been used in A-II as

Fig. 2 Adiabatic charging

Fig. 4 Logical composition of proposed full adder design, **a** for SUM, **b** for conventional carry, **c** for parallelly computed carry

compared to A-I. In the proposed design A-III carry generation has been achieved parallelly as shown in Fig. 4c.

3.1 Proposed adder-I (A-I)

The proposed design of full adder (A-I) is shown in Fig. 5. In this proposed architecture, all the inputs are applied simultaneously and SUM is computed in a single module parallelly with only two-transistor delay. Carry generation has been achieved with the help of the 3 T X-OR gate and MUX. The design consists of a series of complementary transistors, two PMOS for the upper part, and two NMOS below the PMOS. The operation of the circuit is based on the working of the pass transistor. Operation of this design can be explained as; if the input combinations A, B, and C_{in} are 110 applied, then the transistor P1, P2 will be OFF and C_{in} is low; therefore, whatever charge is present at SUM node will be pulled down through the ON transistors N1, N2 by C_{in} and SUM will be computed zero. Following this operation, we can verify all three-bit (A, B, C_{in}) possible

input combinations for SUM. This design requires twenty-one transistors which is less than conventional CMOS-based design.

3.2 Proposed adder-II (A-II)

In this approach, two-phase clocked adiabatic static CMOS logic has been used and the architecture is given in Fig. 6. Two more transistors have been used in addition to the architecture used in A-I. The working for SUM computations is the same as explained in the previous design. Operation of carry generation using adiabatic logic reduces the power requirement up to a great extent, and its operation is based on the inverter operation which is explained in Sect. 2.3 with the help of Fig. 3. Two-phase clocked supply has been used as PC and $\overline{PC}$; both are complementary with each other. The magnitude of $\overline{PC}$ has been kept half as that of PC to reduce the difference in node voltages and consequently reduces power dissipation. In Fig. 6, we have used the SPICE-based Mentor EDA tool for simulating the

Fig. 5 Full adder design for A-I

Fig. 6 Full adder design for A-II

circuit. It is used due to the only available licensed simulating software that can be accessed by a research scholar in our university.

3.3 Proposed adder-III (A-III)

This approach used the idea of parallel computing for carry generation as shown in Fig. 7. In this design, carry is generated parallelly which takes maximum three transistor delay which increases speed. The operation of this circuit is based on the working of the pass transistor. It can be explained as follows: if the input combination for A, B, and C_{in} is 111, then the transistors N10, N11, N12 will be ON and all PMOS except P12 and P13 will remain OFF. Therefore the "carry1" node will be pulled up by C_{in} through N10,

N11, N12 and carry output will be computed as "1" which is theoretically expected. However, the penalty for increased transistor count has been overcome with fast speed. Buffer has been used to increase the drive capability which also provides full voltage swing at the carry output.

4 Results and performance analysis of proposed designs

The proposed designs have been simulated in 0.18 μm CMOS technology. All the proposed designs have been simulated with varying supply voltages and temperatures. Obtained results of the proposed designs in terms of power, delay, and PDP are given in the tabular form and

Fig. 7 Full adder design for A-III

Table 2 Power, delay and, PDP results with varying supply voltage

Supply voltage (V)	A-I			A-II		
	Power(nW)	Delay(ps)	PDP(aJ)	Power(nW)	Delay(ps)	PDP(aJ)
1.2	10.27	44.64	0.45	1.36	43.85	0.059
1.3	12.09	44.64	0.53	1.42	43.76	0.062
1.4	14.12	44.59	0.62	1.49	43.75	0.065
1.5	16.38	44.47	0.72	1.56	43.73	0.068
1.6	18.88	44.28	0.83	1.64	43.61	0.071
1.7	21.65	44.04	0.95	1.72	43.44	0.074
1.8	22.68	43.62	0.98	1.81	43.20	0.078
1.9	28.07	43.59	1.22	1.90	42.89	0.081
2.0	31.78	43.44	1.38	2.06	42.39	0.087
2.1	35.84	43.36	1.55	2.10	41.39	0.086
2.2	40.30	43.18	1.74	2.20	37.12	0.081
2.3	45.18	43.09	1.94	2.32	21.64	0.050
2.4	50.51	42.88	2.16	2.43	17.76	0.043

Table 3 Power, delay and, PDP results with varying temperature

Temp. (°C)	A-I			A-II		
	Power(nW)	Delay(ps)	PDP(aJ)	Power(nW)	Delay(ps)	PDP(aJ)
10	13.73	57.02	0.78	1.79	56.83	0.101
15	16.30	55.45	0.90	1.79	55.15	0.098
20	19.39	50.46	0.97	1.80	51.86	0.093
25	22.05	45.25	0.99	1.80	46.47	0.083
30	27.39	37.24	1.02	1.81	36.17	0.065
35	32.50	23.50	0.76	1.83	23.57	0.043
40	38.50	12.63	0.48	1.87	11.77	0.022
45	45.53	5.82	0.26	1.95	2.17	0.004

also analyzed graphically. The carry generation path is the longest in all designs; therefore, the delay for carry generation has been considered for all designs for the worst-case delay. Table 2 shows the obtained results for A-I and A-II with a varying supply voltage of 1.2 to 2.4 V, whereas Table 3 represents the results with varying temperatures (10 to 45 °C).

Figures 8 and 9 show the power delay product (PDP) which is considered a figure of merit for the electronic circuits. Figure 8 shows the effect of varying supply voltage on PDP, whereas Fig. 9 shows the effect of varying temperature on PDP.

The results in terms of power, delay, and PDP for the proposed design A-III are tabulated in Tables 4 and 5. It is depicted from the tabulated data in Table 4 that carry has been computed at very high speed with a delay of 2.33 ps without a buffer at the standard supply voltage of 1.8 V. Table 5 shows the power and delay results with varying temperature conditions. However, the insertion of buffers increases the delay and area, but it restores the signal swing which proves the good drive capability and functionality of the proposed design.

Fig. 8 PDP results of A-I and A-II with variable supply voltage

The effect of buffer insertion on delay is depicted in the given figures below. Figure 10 shows that the proposed design achieved very high speed utilizing parallel computing concepts with varying voltage, whereas Fig. 11 shows the delay with and without buffer with varying temperatures.

Fig. 9 PDP results of A-I and A-II with varying temperature

Table 4 Power, delay and, PDP results with varying supply for A-III

Supply voltage (V)	Power (μ W) with buffer	Delay (ps) without buffer	Delay (ps) with buffer	PDP(aJ) with buffer
1.2	0.007	4.90	66.58	0.47
1.3	0.016	4.54	65.64	1.05
1.4	0.033	3.68	64.26	2.12
1.5	0.066	3.66	64.04	4.23
1.6	0.129	3.10	63.69	8.22
1.7	0.246	2.71	63.24	15.56
1.8	0.456	2.33	62.65	28.57
1.9	0.822	1.97	61.89	50.87
2.0	1.43	1.63	61.02	87.26
2.1	2.43	1.13	60.57	147.19
2.2	3.97	0.64	59.24	235.18
2.3	6.24	0.32	58.16	362.92
2.4	9.43	0.13	57.53	542.51

Table 5 Power, delay and, PDP results with temperature for A-III

Temp. (°C)	Power (μ W)	Delay(ps) without buffer	Delay(ps) with buffer	PDP(aJ)
10	0.24	2.52	73.19	17.57
15	0.28	2.44	70.93	19.86
20	0.33	2.43	66.46	21.93
25	0.39	2.37	63.75	24.86
30	0.50	2.27	61.49	30.75
35	0.67	2.25	60.28	40.39
40	1.24	2.25	58.71	72.80
45	1.90	2.16	57.63	109.50

Fig. 10 Delay trends with varying voltage

Fig. 11 Delay trends with varying voltage for A-III

4.1 Comparison with existing designs

The proposed designs have been compared with best-reported designs in literature in terms of device count, power, delay, and PDP with technology. The proposed designs show better performance in terms of speed and power. Table 6 shows the comparison with existing designs.

The performance of the proposed designs has been compared and represented graphically as shown in Fig. 12 based on average power, worst-case delay, and technology used. It is depicted from Fig. 12 that the proposed designs perform better as compared to the latest designs reported in the literature.

4.2 Waveforms

The output waveform in Fig. 13 given below clearly shows that the signal swing achieved is sufficient for switching purposes. Figure 13a shows graphically all the three-bit possible combinations for a full adder, whereas Fig. 13b shows the output logic waveforms of the proposed circuit A-I for carry and sum. Figure 13c represents the output logic waveforms of proposed circuit A-II for carry and sum. Figure 13d shows the output logic waveforms of proposed circuit A-III for V(carry) and

Table 6 Comparison with existing designs

Design	Supply voltage(V)	Avg. Power(μ W)	Delay (nS)	PDP (fJ)	Techno-logy(μ m)	Device count	References
CMOS	0.8	0.61	0.681	0.41	0.18	28	[17]
Maj FA	1.8	0.54	0.687	0.37	0.18	–	[17]
Mix TFA	1.8	6.76	0.099	0.67	0.18	–	[18]
FASR-CPL	1.8	60.6	0.278	16.8	0.18	26	[19]
EEPAL	0.9	–	–	3.63	0.03	26	[20]
Hybrid FA	1.8	4.15	0.224	0.931	0.18	16	[21]
SRCPL FA	1.2	1.37	0.048	67.17×10^{-3}	0.09	21	[22]
DPL FA	1.2	0.96	0.064	61.17×10^{-3}	0.09	23	[22]
Methodology-III	3.3	0.199×10^{-3}	5.10	1.01×10^{-3}	0.35	14	[23]
Methodology-IV	3.3	0.192×10^{-3}	5.10	0.97×10^{-3}	0.35	14	[23]
Proposed 1 (A-I)	1.8	22.68×10^{-3}	43.62×10^{-3}	0.98×10^{-3}	0.18	21	[Present]
Proposed 2 (A-II)	1.8	1.81×10^{-3}	43.20×10^{-3}	0.078×10^{-3}	0.18	23	[Present]
Proposed 3 (A-III)	1.8	0.456	62.65×10^{-3}	28.57×10^{-3}	0.18	23/27	[Present]

Fig.12 Comparison with existing designs in terms of avg. power, delay and, technology

sum, whereas $V(\text{carry2})$ represents the output with buffer and restores the logic completely. Output waveforms of simulated circuits verify the functioning of the proposed

design with output voltage level, above 1.14 V for high logic, and below 0.78 V for low logic, which is sufficient

Fig. 13 Waveforms of **a** Three-bit input combinations, carry and the sum of a full adder with **b** A-I **c** A-II **d** A-III

for adiabatic logic families for digital switching circuits as reported in the literature.

5 The layout of the proposed design A-III

The layout of the proposed design A-III has been generated according to the flowchart as given in Fig. 14. The layout of the new design A-III has been simulated to verify

the functionality of our proposed logic of parallel computing. Figure 15 shows the layout of design A-III with an area of $192.68 \mu\text{m}^2$ including a buffer. Post-layout design A-III consumes the power of $0.526 \mu\text{W}$ with a delay of $64.23 \times 10^{-3} \text{ ns}$ with a buffer with 1.8 V supply. This layout has been designed using HSPICE and at $0.18 \mu\text{m}$ technology. This software and technology have been used as at this technology node the leakage currents are less as compared to small technology nodes.

Fig. 14 Flowchart of layout generation

Fig. 15 The layout of design A-III

6 Conclusion

In this article, implementation of parallel computing with adiabatic logic has been demonstrated for full adder designs. The work done in this article has been simulated in 0.18 μm CMOS technology. The proposed approach mitigates the issue of large propagation delay and achieves a signal restoration with a buffer. The presented designs perform better in terms of power dissipation, delay, and the number of transistors used as compared with the existing designs which are reported in the literature. It is evident from the results that the overall power efficiency of the proposed designs is good as compared to existing designs. Implemented new circuits work fairly with varying voltage and temperature conditions. The proposed designs with adiabatic logic also perform better with sufficient output voltage levels. These improvements in performance with high speed make proposed full adders better candidates for

ultra-low-power applications. As a future work, author is working actively toward the implementation of this approach in sequential circuits.

Compliance with ethical standards

Conflict of interest The authors declare that they have no competing interests.

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