A new approach for islanding management in PV system using frequency modulation technique and simple adaptive load shedding algorithm

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Abstract

One of the main challenges in distributed generation is to keep supplying some priority loads when islanding occurs. Unfortunately, most anti-islanding protection (AIP) methods fail in islanding detection if the demand in the islanded loads matches the production in the island. Many active AIP schemes are too slow and cause power quality problems. In this paper, an islanding detection method for inverter-based photovoltaic system (PVS) is presented, operating with a simple adaptive loads shedding algorithm. This method is based on modulating the inverter output voltage at the point of common coupling. This frequency modulation consists in introducing interharmonics as side bands of the inverter voltage. After islanding detection, the adaptive loads shedding algorithm operates so as to keep powered priority loads as possible. AIP scheme and PVSs are implemented in MATLAB/Simulink environment. The effectiveness of the proposed scheme was tested and evaluated under a wide range of operating conditions. These tests determined that the proposed technique does not exhibit any non-detection zone and detects islanding within five electric cycles. No significant effect on power quality is recorded even during islanding detection time. The proposed technique was also robust and more independent of system parameters than some others.

Keywords Frequency modulation · Islanding · Load shedding · Photovoltaic system

1 Introduction

A distributed energy resource disconnected from the power grid forms an island with the loads remained connected. This is a result of an unintentional islanding of this part of the grid. In power systems, accidental islanding scenarios should be avoided mainly because of possible safety issues for maintenance personnel. Specialists consider this phenomenon very dangerous for both users, grid and island's inverters, which are all involved. Islanding concept has evolved in recent years. We distinguished two types of islanding: short islanding (duration less than one second) and unintentional islanding (duration above a

second). It is essential to detect islanding situation as soon as possible in view to organize the protection of users and installations [1, 2].

Islanding detection methods can be divided into passive, active and communication-based methods [3]. Remote techniques are based on the communication between utilities and DGs, such as power line communication, supervisory control and data acquisition. Although they do not have non-detection zone (NDZ), they are expensive to be implemented and need a reliable communication link [3, 4]. NDZs are defined as a loading condition for which an islanding detection method is unable to detect islanding [5]. Local techniques are based on both

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passive and active methods. Passive methods are based on measuring local parameters of the DG and comparing it with the reference values. Common passive methods are over/under frequency protection (OFP/UFP), over/under voltage protections (OVP/UVF) [6], phase jump detection and voltage harmonic monitoring [7]. These techniques have significant NDZ. To overcome NDZ problem, active AIP methods have been adopted. In this case, islanding detection is achieved by grid instability due to disturbance injection into the system operational control. Active methods are permanently improved by reducing the NDZ and the time detection delay. Some active techniques are slip-mode frequency shift (SMS), Sandia frequency [8], voltage shift and negative sequence current injection [9]. Active methods have a negligible NDZ, but false detection is a vital problem due to overlap of injection parameter with non-islanding events, especially when multiple DGs are involved in the system [10]. Active AIP methods, which are based on drifting voltage magnitude or frequency out of the predefined thresholds by deliberate injection of perturbations, are usually characterized by a smaller NDZ in comparison with the passive methods. *However, the better islanding detection performance of active methods comes at the cost of degraded power quality.* Communication-based methods are immune to the NDZ problem, but they tend to be costly.

The detection techniques have been improved by combining active methods with passive methods or their derivatives. These are hybrid methods. We have in this group voltage unbalance and total harmonic distortion of current-based technique [11], Improved Active Frequency Drift Anti-Islanding Detection Method [12], hybrid islanding detection method for inverter-based DGs using Reactive Power Injection and ROCOF [13], just to mention a few. Reactive power variation (RPV)-based AIP methods are favourable in the sense that they do not cause current distortion unlike many other active AIP schemes. Due to economic reasons, controlling the reactive power output of the DG unit is also more reasonable in comparison with manipulation of the active power. The periodically changing frequency is used as a criterion to detect islanding. We often have many problems when calculating or choosing thresholds parameters and the control loop's main coefficient of many active methods [10–14]. We can also mention the negative impact of some techniques on the power quality, particularly those based on the injection of current, of active or reactive power [9, 15–17]. Recent methods use feedback loop to better stabilize the detection operation. The presence of loops slows down the detection process [3, 5], especially when the monitoring variable is the frequency [13]. The time needed for islanding detection can go up to ten electrical cycles [13, 17–19]. The most recent passive method, based on the ripple

spectral content of the voltage at the PCC, detects islanding within 300 ms (18 electrical cycles) [20]. It has many advantages over other passive and even active methods: it is very simple to implement, has no NDZ, high reliability and detects islanding even in zero power mismatch. However, this technique still depends on the size and parameters of the DG system, since ripple content closely relies on the frequency of operation in the inverter (and eventually DC–DC converter). The operation of a powerful inverter in the grid could increase the ripple content in the instantaneous output voltage at the PCC and can cause untimely detections. The fundamental frequency of 12 Hz was selected as an optimal value for computations. On the other hand, it was also proved in the same work [20] that time delay after faults increases when frequency decreases. Thus, detection time can also be reduced if we avoid using large period window in calculations.

In this paper, we propose a new management method of a PVS in islanding situation. Anti-islanding protection method is based on modulating inverter frequency such that the specific frequency components (lateral bands of the modulation) appear at the PCC voltage during islanding. This is achieved by using a specific waveform matching triangle signal to feed pulse-width modulation (PWM) of the inverter. Frequency domain techniques require much real-time computations, thus cannot be easily implemented into a DG protection scheme. Developed in time domain spectral analysis, the proposed active method overcomes the drawbacks of the aforementioned work [20] and becomes better than the latest active techniques in many aspects. In comparison with recent methods, the proposed method is especially advantageous for its fastness and its low impact on power quality. It is also very simple to implement, by monitoring only one parameter without any loop. Moreover, we do not need to add any kind of power to the inverter output such as in the RPV-based methods. Islanding can be detected even in multiple DGs operation, independent of the grid size or parameters. We complete the management system with a simple adaptive loads shedding allowing the PVS to supply in real time the priority loads among the least powerful. Adaptive shedding process uses an algorithm referring to apparent powers needed by different loads when islanding occurs. This algorithm calculates in real time apparent power consumed by each local load and compares them with the maximum power point tracking (MPPT).

Section 2 gives the general functioning of the system and presents the main parts of the PVS. In Sect. 3, anti-islanding detection and adaptive loads shedding methods are developed. Simulation results and discussion showing the effectiveness of the proposed approach are presented in Sect. 4. Finally, Sect. 5 summarizes the paper with concluding remarks.

2 Description of a grid-connected PVS

Figure 1 shows how a PVS can be coupled with the main grid to supply the local loads. The following are found in a PVS scheme:

- A PV array made by assembling panels;
- A DC/DC Boost converter;
- A DC/AC converter based on PWM;
- A Maximum Power Point Tracking (MPPT) block;
- An islanding detection block;
- An adaptive loads shedding block.

The first three points listed make up the 'power circuit' of the system. The last two forms the inverter 'control circuit'. Loads supplied can be nonlinear and linear loads. Thus, the PVS can operate with any type of local load represented by the corresponding device symbols (resistor, diodes, etc.). Section 4 will confirm this. The PVS must also measure the current consumed by each local load. This will be essential for the adaptive loads shedding algorithm developed in Sect. 3.2.

2.1 Presentation of the power circuit

The main grid supply is just a sine source. In Fig. 1, the switches represent possibilities of coupling between blocks. In fact, the inverter is coupled to the utility grid

using a synchronizing algorithm for auto-reclosing. In this paper, the auto-reclosing is considered neither for proposed islanding study nor for adaptive shedding scheme.

Between panels and inverter, we have a DC–DC converter block. This may lead to a major micro-grid challenge during considerable change in solar irradiation. DC–DC converter is an electronics circuit that provides a lossless transfer of energy between different circuits at different DC voltage levels. There are many types of chopper. The most popular is 'Boost' chopper, as shown in Fig. 2. It achieves stable DC voltage across the capacitor (C) for whatever variation may occur in solar irradiation or in panel temperature, for example, when irradiation becomes too low. The Boost converter can increase the input DC voltage (from panels) by changing the duty ratio of the switch. When the duty ratio is less than 1, the output voltage is

Fig. 2 Boost converter

Fig. 1 View of the PVS in the grid

greater than the input voltage (until the process is limited by the device) as in (1)

$$V_{out} = V_{in}/(1 - D) \quad (1)$$

where D is the duty cycle of the converter [21].

2.2 Presentation of the control circuit

Energy produced by photovoltaic panels passes through a DC–DC converter before being converted into alternating form by an inverter. Then the output filter delivers a sine wave voltage to loads.

MPPT algorithm keeps the Boost chopper at its maximum power supply. The maximum power extraction from the PV array is ensured by using incremental conductance algorithm. It is similar to the ‘perturb and observe’ method, but it has a better accuracy. At the maximum power point (MPP), the PV characteristic [power extracted (P_{pv}) vs output voltage (V_{pv})] has a zero slope. That means the ratio dP_{pv}/dV_{pv} is zero. The MPP can be tracked by comparing the instantaneous conductance to the incremental conductance. Towards the left or right (of this MPP), the MPP ratio of P_{pv} to V_{pv} is altered. The chopper output voltage is adjusted in accordance with MPP of PV array [22]. Synchronization operates when the power supply (by the main grid) resumes, after islanding event, reconnecting the PVS to the grid. The inverter’s output power is synchronized with the grid using a phase-locked loop (PLL). In this study, the islanding detection technique is implemented within the inverter and is designed to de-energize the PVS whenever islanding is detected. These two modules of the

control circuit (MPPT and synchronization blocks) are not developed in this paper.

When utility grid is disconnected, our new islanding detection method permits the isolation of the PVS from the grid. Loads adaptive shedding algorithm keeps the local loads connected such that the total apparent power is less than that available on the DC bus.

3 Islanding detection method and loads adaptive shedding method

Simulink model of the proposed grid-connected PVS is given in Fig. 3. During further simulation, a distorted grid will replace the sine wave.

3.1 Islanding detection method

When the main grid and the PVS inverter are supplying an RLC local load type, the equations of the active and reactive powers are given by (2) and (3):

$$(1/R)V_{grid}^2 = P_{inv} + \Delta P = P \quad (2)$$

$$((1/L\omega_{grid}) - C\omega_{grid})V_{grid}^2 = Q_{inv} + \Delta Q = Q \quad (3)$$

Islanding mode cancels ΔP and ΔQ . The PVS producing alone matches the RLC load consumption. Thus, Eqs. (2) and (3) can be rewritten as Eqs. (4) and (5), respectively:

$$(1/R)V_{inv}^2 = P_{inv} \quad (4)$$

Fig. 3 Simulink model of the proposed grid-connected PVS

$$\left(\frac{1}{L\omega_{\text{inv}}} - C\omega_{\text{inv}} \right) V_{\text{inv}}^2 = Q_{\text{inv}} \quad (5)$$

Magnitude and frequency of the voltage at PCC clearly depend on PVS supply during islanding, as it remains the only source present. Dividing Eq. (2) by P_{inv} from Eq. (4), we get Eq. (6).

$$\frac{\Delta P}{P} = \frac{V_{\text{grid}}^2}{V_{\text{inv}}^2} - 1 \quad (6)$$

If $\Delta P \neq 0$, the magnitude of V_{PCC} should vary after islanding. Isolating inductive power and considering capacitive power $Q_C = C\omega_{\text{grid}} V_{\text{grid}}^2$, we have Eqs. (7) and (8).

$$\frac{1}{L\omega_{\text{grid}}} V_{\text{grid}}^2 = Q + \Delta Q + C\omega_{\text{grid}} V_{\text{grid}}^2 \quad (7)$$

$$\frac{1}{L\omega_{\text{inv}}} V_{\text{inv}}^2 = Q + C\omega_{\text{inv}} V_{\text{inv}}^2 \quad (8)$$

Then if $\Delta Q \neq 0$, we can write (9):

$$\frac{\omega_{\text{inv}} V_{\text{grid}}^2}{\omega_{\text{grid}} V_{\text{inv}}^2} = \frac{Q + \Delta Q + Q_C}{Q + Q_C \cdot \frac{\omega_{\text{inv}} V_{\text{inv}}^2}{\omega_{\text{grid}} V_{\text{grid}}^2}} \quad (9)$$

By taking into account (4), we obtain (10):

$$\frac{\omega_{\text{inv}}}{\omega_{\text{grid}}} \frac{\Delta P}{P} - \frac{\Delta Q}{Q} = \left(1 - \frac{\omega_{\text{inv}}^2}{\omega_{\text{grid}}^2} \right) \frac{Q_C}{Q} + 1 - \frac{\omega_{\text{inv}}}{\omega_{\text{grid}}} \quad (10)$$

Equation (10) indicates that there is no change in frequency and magnitude with $\Delta Q = \Delta P = 0$. Thus, the frequency could change after the islanding when there is power mismatch between PVS production and load consumption. $\Delta P \neq 0$ or $\Delta Q \neq 0$ modifies the value of the PVS pulsation ω_{inv} . We can find more details on this development in [1, 5, 7].

No islanding detection should occur in the case of oscillating loads ($\omega_{\text{inv}} = \omega_{\text{grid}} = \frac{1}{\sqrt{LC}}$) when surveying phasors of V_{PCC} . To overcome this, the active method developed here will add a signature in the inverter output voltage.

In the proposed method, the signature added at the inverter output will not appear on V_{PCC} , during normal operation, due to the powerfulness of the main power grid. This signature will become clearer after islanding, since the PVS inverter operates alone with the loads. We then choose to modulate the inverter frequency, adding two interharmonics (25 Hz and 75 Hz) as sidebands of the inverter output voltage. This produces an added 25 Hz ripple on the inverter output frequency. Filters on the grid can not eliminate sidebands, since they are not far from the fundamental frequency.

Assuming interharmonics can cause disturbances [23], these sidebands must have a very low magnitude. We are effectively modulating the frequency of the inverter output voltage using a very low modulation depth. Then V_{PCC} frequency will slightly vary sinusoidally. The frequency variations at the PCC due to fluctuations of active or reactive powers (ΔP or ΔQ) at the islanding time would never fluctuate at 25 Hz for long. Some non-islanding events can falsely trigger islanding detection: short-circuit faults, loss of a parallel feeder, load switching, capacitor switching, nonlinear loads, starting of large induction motors, distorted grid, etc. Any of these events is characterized by a disturbance period, during which the 25 Hz and 75 Hz components increase as much as other frequency components. Then the islanding detection must be confirmed after the largest of those disturbance times. This technique has a very low impact on increasing the total harmonic distortion (THD) when modulation depth is very low and when the fundamental frequency (50 Hz) is a multiple of the one of the modulating signals. We choose 25 Hz frequency for the modulating signal in view of minimizing the period of the signal to be found in islanding situation.

After being modulated, the inverter output voltage can be expressed by (11):

$$V_{\text{inv}}(t) = 220\sqrt{2} \cos \left[\omega_{\text{inv}} t + 2\pi k_f \int_0^t m(u) du \right] \quad (11)$$

where $m(u) = A_m \cos(\omega_m u)$ is the modulating signal of 25 Hz and k_f is the sensibility of the modulator [24]. Instantaneous phase is given by (12):

$$\theta_i(t) = \omega_{\text{inv}} t + 2\pi k_f \int_0^t m(u) du = \omega_{\text{inv}} t + (k_f A_m / f_m) \sin(\omega_m t) \quad (12)$$

$\beta = (k_f A_m / f_m)$ is the modulation depth. Instantaneous frequency is therefore $f_i(t) = f_{\text{inv}} + k_f A_m \cos \frac{\omega_{\text{inv}}}{2} t$. With a low modulation depth ($\beta \ll 1$), we obtain a case of an Armstrong modulator [24]. Inverter output voltage can be expressed as:

$$V_{\text{inv}}(t) \approx 220\sqrt{2} \left[\cos \omega_{\text{inv}} t - \beta \sin \left(\frac{\omega_{\text{inv}}}{2} t \right) \sin(\omega_{\text{inv}} t) \right] \quad (13)$$

$$\approx 220\sqrt{2} \cos \omega_{\text{inv}} t - 110\beta\sqrt{2} \cos \left(\frac{\omega_{\text{inv}}}{2} t \right) + 110\beta\sqrt{2} \cos \left(\frac{3\omega_{\text{inv}}}{2} t \right) \quad (14)$$

Spectral analysis of $V_{\text{inv}}(t)$ shows three components (at 25 Hz, 50 Hz and 75 Hz) for a slight periodic variation of the frequency (from 49.9 Hz to 50.1 Hz, for $\beta = 0.1$) [24]. To obtain $V_{\text{inv}}(t)$, we will produce inverter PWM

signal, matching the reference signal $s(t)$ given as follows with a triangle waveform.

$$s(t) \approx \cos(\omega_{inv}t) - \frac{\beta}{2a} \cos\left(\frac{\omega_{inv}}{2}t\right) + \frac{\beta}{2a} \cos\left(\frac{3\omega_{inv}}{2}t\right) \quad (15)$$

where ' a ' is a constant (assuming the very small values of the two sidebands) representing the effect of the inverter. This constant depends on the type of the inverter. To obtain the desired sidebands at the inverter output, we will amplify the magnitude represented by ' $\frac{\beta}{2a}$ ' until getting ' $110\beta\sqrt{2}$ ' at the output. This sidebands amplitude must correspond to about 0.15% (or less than that value) of the fundamental since IEC recommends having a total distortion ratio (TDR) less or equal to 0.2% [23]. Section 4.2 deeply explains how to set the sidebands value. The PVS inverter is now controlled by three components as shown in (15). We then expect on its output three components of (14) (with eventually their harmonics). Frequency modulation guarantees apparition of harmonics even with small modulation depth. THD will normally change after islanding. Islanding can be confirmed after at least two periods of the 25 Hz sine wave (80 ms), by checking the level of the sidebands (V_0). If this marker exceeds a predefined threshold (V_D), we conclude to an islanding event. Islanding confirmation normally stops the modulation process in the PVS inverter.

The monitoring of 25 Hz and 75 Hz voltage components at PCC (V_L and V_H , respectively) is the aim of the islanding detection block. To choose the frequencies of V_L and V_H , the highest period ($T_1 = 1/f(V_L) = 1/25$ Hz) must be the smallest multiple of the two other periods (1/50 Hz and 1/75 Hz). This in order to compute values over entire period T_1 . After many tests, it appears that other pairs of frequencies (20 Hz and 80 Hz, 35 Hz and 65 Hz, etc.) degrade the power quality and increase the islanding confirmation time delay. We compute the respective mean value V_L and V_H of V_L and V_H (according to each sideband frequency). These signals are small and need to be amplified. We then calculate the square of their average value (called V_0 in volt²). The sidebands are amplified to increase the margin between their level before and after islanding. The detection criterion V_0 is now compared to a threshold. The method is depicted on the flow chart of Fig. 4. The sidebands (V_L and V_H) can also be extracted from V_{PCC} using an adaptive linear neuron (Adaline), for example. We can otherwise proceed by demodulating $V_{inv}(t)$ to get an image of modulating signal $m(t)$. This may be difficult due to much closed values of modulating signal (25 Hz) and carrier (50 Hz).

Fig. 4 Flow chart of proposed islanding detection method

3.2 Loads adaptive shedding method

Uninterrupted power supply of priority loads is considered. After islanding detection, the proposed adaptive algorithm must organize overloads shedding that can affect or even damage the PVS. We consider here apparent power consumed by each local load. To get the value of the current flowing through each local load is the main condition to estimate them, since knowing the voltage at the PCC. We will consider the model of Fig. 3, with three local loads. Our algorithm matches these apparent powers with the one available in the PVS and chooses loads

to disconnect from the inverter output. The matching can take into account the profile or the historical behaviour of each consumption, such as average power after ten electrical cycles and maximum power used on the same period during the last 10 days. In this paper, we just used the power consumed in four electrical cycles (four periods of 50 Hz = 4T) before islanding happens.

Normally, priorities are established for loads elimination. Social considerations usually set these priorities (e.g. shopping centre first, water installation and then hospital, etc.). Therefore, algorithm proceeds at loads shedding, starting with those with less priority. Priority issues are not addressed here. We just subjectively gave priority to the load(s) having lowest consumption. Opening overall loads must automatically stop the PVS production until the recovery of the utility grid. If the island is supplied by many PVS, we needed a coordinated loads adaptive shedding which works on the model described here. In a given island, we consider three loads L_1, L_2, L_3 and their respective apparent powers S_1, S_2, S_3 . The maximal apparent power available on PVS(s) operating is $S_D = S_{PVSmax}(t - 4T)$. As shown in Fig. 5, adaptive loads shedding algorithm is made by the four steps presented as follows (for managing three separated loads without priority consideration).

- Check whether S_D can supply the loads;
- Else, find the biggest sum of two loads S_D can supply;
- Else, find the biggest loads S_D can supply;
- Else, turn off the PVS.

4 Results and discussion

The grid-connected PVS shown on Fig. 3 is realized in MATLAB/Simulink environment (version 9.3.0, R2017b). We used a Simulink model of photovoltaic module *SunPowerSPR-435NE-WHT-D*. This model is made up of ten parallel lines of eight panels each in series that produces about 32 kW, meaning 58A under 550 V, for 1000 W/m² of irradiation and 40 °C of temperature.

4.1 Simulation of the PVS without detection and loads shedding modules

This simulation must reveal the characteristics of the PVS inverter. The PVS output is not yet modulated. All the harmonics and interharmonics normally produced, regardless of the islanding detection method are evaluated. In this section, the inverter output filter is an L - C type, where $L = 10$ mH and $C = 400$ μ F. The PWM is generated by a 4 kHz triangle signal. Load used is a parallel R - L - C dissipating $P = 32$ kW and $Q = 32$ kVAR under 220 V–50 Hz. Lines model

Fig. 5 Flow chart of three loads adaptive shedding

used is R - L ($R = 0.01 \Omega$ in series with $L = 0.1$ mH). Utility grid is an ideal voltage source of 220 V–50 Hz.

Islanding and loads variations are simulated using circuit breakers, to obtain disturbances as large as possible (like in real accidental cases). Figure 6 shows the RMS voltage variations at the PCC. We observe a disturbance period of around 60 ms after islanding due to switches effect. Figure 7 presents the corresponding THD obtained before and after islanding. There we observe that when the PVS becomes the main power supply of the island, all its characteristics appear in the PCC voltage. As islanding confirmation normally stops the modulation process in the PVS inverter, the THD from that moment is 1.4 (Fig. 7b). THD after islanding is systematically evaluated during all

Fig. 6 RMS voltage components at the PCC without detection module

Fig. 7 THD of V_{PCC} without detection module before islanding (a) and after (b)

the simulations of this section (Sect. 4) to show the low impact of the technique on the power quality in the case when the modulation is still going on.

We check the power quality variation by observing voltage THD on two (or any even number) electrical cycles at the PCC before and after islanding (at 40 ms and 400 ms, for example). Two electrical cycles effectively contain a period of 25 Hz and three periods of 75 Hz. We can then evaluate with Eqs. (16) and (17), respectively, the total subharmonic distortion (TSHD) and the total distortion ratio (TDR) obtained.

$$\text{TSHD} = \frac{V_{PCC(25\text{ Hz})}}{V_{PCC(50\text{ Hz})}^3} \quad (16)$$

$$\text{TDR} = \frac{\sqrt{V_{PCC(\text{TRMS})}^2 - V_{PCC(50\text{ Hz})}^2}}{V_{PCC(50\text{ Hz})}} \quad (17)$$

During loads shedding, that happens at 0.3 s in Fig. 6, we notice few effects both on V_{PCC} magnitude and on sidebands magnitude. Larger disturbances are observed during islanding, lasting approximately 60 ms. The two

sidebands reach close to fundamental RMS value and disappear as soon as the disturbance ends.

Figure 7 clearly reveals PVS characteristics. In the next section, this will help us to properly adjust the sidebands for a better detection. After islanding, magnitude of harmonics increases from two to four times. It depends on the penetration of the PVS. Voltage THD increases, taking up from 0.56 to 1.40% in the case presented in this section (from 1.08 to 1.66% with another output filter in the case of single-phase inverter). This explains in the next section why THD changes after islanding. Globally, the PVS induces minimum power quality variation within standards (IEEE1547, Sect. 4.3) [25]. When testing the proposed islanding detection method, we set inverter's switching operation at different frequency values (2 kHz, 5 kHz and 10 kHz).

4.2 Simulation of the PVS with the islanding detection module

We repeat the previous experience, but now using $s(t)$ from Eq. (15) to drive the inverter. Figures 8 and 9 depict the result of that experience and reveal the effect of the

Fig. 8 Comparison of RMS voltage components at the PCC (with detection module and without)

Fig. 9 THD of V_{PCC} with detection module: **a** before islanding and **b** after islanding

frequency modulation on V_{PCC} . The modulation of inverter output frequency causes a ripple of V_{PCC} RMS value. True RMS values of V_{PCC} , V_L and V_H are shown in Fig. 8. Before islanding, V_L and V_H are insignificant, since the PVS power is less than that of the main grid. Islanding disturbance causes increasing of almost all frequency components at PCC for a short period. After that, the main grid is disconnected, and V_L and V_H return to the value fixed into the inverter. Effects of modulation only appear when the main grid is off. Figure 9 shows the spectral analysis of V_{PCC} during simulation. Table 1 summarizes the results with different types of load. To set V_L and V_H values to 0.15% of the fundamental, we increase their effect in normal grid-connected mode until that level. We also notice

relative increasing of harmonics of the modulated PVS signal (made now by three signals). For example, 225 Hz, 250 Hz and 275 Hz components grow up together when islanding happens. Performant filters have no difficulty to cancel these new harmonics. V_{PCC} parameters during islanding could degrade the power quality, though within an acceptable range. Experiences with PWM frequency at 2 kHz, 4 kHz and 5 kHz have been also conducted successfully, by setting the L - C filter at different values (in view to extract maximum power from the Boost converter and reducing harmonics).

Effectively, THD of V_{PCC} reaches 2% when waiting for islanding confirmation, as shown in Fig. 9b. This value is under 5%, which is the standard limit [25]. We use the

Table 1 Simulation results in different scenarios

Type of load	P (kW)	Q (kVAR)	V_L (V)	V_H (V)	After t (ms)
RLC	20	2	5.5	4	88
RLC	20	10	4.5	3	85
RLC	10	10	4.8	3.5	79
RLC	10	20	6	3.3	84
RLC	10	+ 50	3.6	5.7	102
RLC	10	− 50	5.9	2.8	109
RLC: $Q_f = 0.4$	25	+ 10/− 10	3	3.5	102
LC	0	+ 20/− 20	64	33	110
4 D-bridge: $R = 4 \Omega$	5.5	5	71		
4 D-bridge: $R = 4 \Omega$ $L = 1$ mH	8	6.1	76

Fig. 10 V_{PCC} and islanding confirmation signal

same output inverter filter of the experience of Sect. 4.3. Islanding disturbances are more important than inverter pollution (due to modulation effects) and take a very small amount of time. This pollution disappears by cancelling V_L and V_H when islanding is confirmed (to keep a better power quality during loads shedding). Assuming filters would cancel harmonics due to normal inverter operation, we just considered the effects of the interharmonics introduced in power inverter when evaluating the total distortion ratio. We then have a TDR of 0.2% before islanding and 4% after. Then the technique could induce flickers if there is an NDZ (but never in normal operation).

Figure 10 shows an islanding detection followed by opening of inverter switches. The load used here has a unit power factor with $P = 15$ kW, $Q_L = 8$ kVAR and $Q_C = 8$ kVAR. As announced in Sect. 2, we could confirm islanding events after at least four electrical cycles (i.e. two cycles of 25 Hz). Then all protection devices operate and loads shedding starts. For different loads configurations (even power factor unity), V_L and V_H increase after islanding and V_0 still greater than a threshold V_D when disturbances due to breaker operation disappear.

To evaluate performance, many load configurations are tested (resonating RLC, pure Resistor, oscillating LC, high quality factor, etc.) to prove the effectiveness of the method. Islanding detection is ensured without NDZ. In Table 1, for example, when inductive RLC needs $P = 10$ kW and $Q = + 50$ kVAR, it represents 160% the capacity of the PVS (positive mismatch with the main grid). After islanding, V_{PCC} must change, according to (6). Without the OVP/UVF device to stop the PVS operation, modulation approach will still function. Sidebands become quite stable at 102 ms after islanding. Simulation using nonlinear load (4D-bridge: $R = 4 \Omega$) required only 30% of the PVS capacity, and shows stable detection waveforms after only 71 ms.

4.3 Simulation of the PVS with the islanding detection module using IEEE test system

Different types of loads have been tested using IEEE and UL test systems. The first test set is the most interesting. IEEE standards require inverter operations with loads having $1 < Q_f < 2.5$ at resonant frequency [25]. To match 100% of the PVS power (32 kW as mentioned in Sect. 2.1) with a quality factor $Q_f = 1$, for example, we got $R = 1.51 \Omega$, $L = 4.82$ mH and $C = 2104.53 \mu\text{F}$. To be able to produce those 32 kW, the inverter output filter is now set at $L = 0.02$ H and $C = 600 \mu\text{F}$, and it operates at 4 kHz frequency. In this section, TDH obtained after islanding is 2.37%, with a nominal PVS power of 32 kW and a quality factor $Q_f = 2.5$. The corresponding TDR is 3%.

Figure 11 summarizes the results of those simulations. In Fig. 11a, we can observe the effect of quality factor Q_f . Higher values of Q_f mean that loads absorb much reactive power. As established in Eq. (10), islanding would then reduce the amount of frequency oscillations in V_{PCC} waveform. Then quality factor reduces the margin between the islanding and non-islanding levels (V_0 before and after islanding). The same effect is observed in the output

Fig. 11 Resume of IEEE test results, curve of V_0 with a single-phase inverter: **a** effect of different quality factors, **b** effect of real power mismatch, **c** effect of larger real power mismatch, **d** effect of reactive power mismatch

waveform for all other islanding scenarios. Hence, we will set the threshold based on the case $Q_f = 2.5$.

Effect of real power mismatch is depicted in Fig. 11 b, c, while in (d) we have effect of reactive power mismatch. Both positive and negative real power mismatch scenarios ($\Delta P \neq 0$) were simulated for $Q_f = 2.5$, with 1% increments from 1 to 10% followed by 10% increments from 20 to 50%. Reactive mismatch scenarios ($\Delta Q \neq 0$) between $\pm 4\%$ were simulated with $Q_f = 2.5$. The percentages here are with respect to the load nominal real power. Positive real power mismatch indicates that the PVS supplies more power than what the local load consumes (ΔP goes towards the utility grid), while negative real power mismatch indicates that the load requires more power than what the PVS is able to supply. After investigation, the longest perturbation period is the fact of a short-circuit fault (phase and neutral for within 5 ms) during PVS grid

connected operating at nominal power of 32 kW with a load having $Q_f = 2.5$. V_0 spent 78 ms above $5 V^2$. Disturbances do not appear for long as in [20] since the periods used to compute RMS and average values are 1/25 Hz and 1/75 Hz for V_l and V_{lv} , respectively (instead of 1/12 Hz). We changed the PVS nominal power and conducted the tests again (LC filter keeping the same values). Table 2 recaps the results obtained with the worst Q_f case of 2.5. Changing the nominal power of the PVS has very few effects on the technique. Power increases with losses and then reduced V_0 , which remains clearly higher than $5 V^2$.

We implement a three-phase inverter operating under 400 V (between two phases) and a PWM chopping at 4 kHz. Its output filter is now $L = 3$ mH in series with $R = 5$ m Ω . The load supplied in normal operation during this test is an RLC consuming $P = 100$ kW with $Q_f = 2.5$, and the nominal PVS power is 100 kW. In normal operation

(with grid connected), we set the sidebands to obtained a TDR of 0.1% (instead of 0.2% for the other tests with a single-phase inverter). Figure 12 depicts the difference between faults and islanding. Figure 13 shows the influence of a distorted grid on the technique. Frequency variations, unbalance grid and harmonic pollution of the grid do not have a significant effect. However, phase jumps, sags and swells cause serious perturbations. A grid phase jump of 120° and 150% voltage swell have approximatively the same disturbance. But it ends before 80 ms.

Without any incident, maximal value of V_0 is 0.03 V^2 before islanding. After islanding, THD reaches 3.58% and V_0 becomes stable at 128 V^2 (between two phases) or 41 V^2 (between phase and neutral). In this case, we can easily set the threshold. Nevertheless, considering the results of simulations in single phase (with different output inverter filters, different PVS powers, and various linear and non-linear loads) we choose 7 V^2 as the threshold level. It is the medium value of V_0 between the highest value before islanding and the lowest after. The largest disturbance period is 86 ms, caused by capacitor switching (connection of 0.1 F capacitor between each line and neutral). It is shown in Fig. 12. This scenario does not have a negative effect on the technique. THD is kept at 3.58% after islanding instead of 0.74% before, while TDR is 4.2% after and 0.2% before islanding. T_D is closely dependent on the duration of disturbances generated by non-islanding events mentioned above. As a precaution, we will adopt a safety

margin and consider a value. Considering disturbances and the presented results, the best threshold $T_D = 100 \text{ ms}$ (5 electric cycles of 50 Hz). In the single phase, we could set T_D at 80 ms (4 electric cycles) since the largest disturbance period was 78 ms.

Active methods are usually characterized by difficult implementation, particularly due to the closed loops often used to control parameters. Table 3 compares the proposed technique to some recent methods. All of them present no NDZ and have been tested using either IEEE standard or UL standard. The present technique has been tested using both standards. Apart from the speed, the proposed technique does not need OVP/UVP or OFP/UFP [13, 16, 19]. The technique does not affect the power quality as much: in [13], the THD is higher than that obtained with the presented technique. Other techniques do not evaluate this aspect regarding the effect on power quality. The computations are made using 25 Hz and 75 Hz as basic frequencies for V_l and V_h . This explains why disturbance periods are shorter than in [20]. Nevertheless, its implementation is quite simple. It can be the simplest and cheapest active method among the five, at the opposite of [19] which need precise and robust PLL to extract the main criterion of that technique. Moreover, filtering operations can go on, and remote signals transmission or perturbation in the grid could trigger false islanding detection. The technique does not depend on the overall ripple content of V_{PCC} as in [20]. The method is robust: many inverters can operate in the same grid keeping the efficiency of the technique. On the other hand, only successive phase jumps swells and sags within 100 ms could cause false islanding detection. The next section presents this scenario

Table 2 Effect of changing PVS nominal power

PVS nominal power (kW)	$V_{0\text{MAX}}$ before islanding (V^2)	$V_{0\text{MIN}}$ after islanding (V^2)
16	1.46	14.44
32	1.25	20.79
48	1.14	16.32
64	1.04	17.14
96	1.44	10.36

Fig. 12 Tests with a three-phase inverter under faults: curve of V_0 between two phases in red, between phase and neutral in blue

4.3.1 Simulation of operation under multiple PVSs

Figure 14 shows many PVSs operating in the same grid. Table 4 summarizes the obtained results. The variable 'm' is the number of PVSs that operate in the grid when islanding happens. We also investigate the case sidebands tend

Fig. 13 Tests with a three-phase inverter with a distorted grid

to cancel themselves. We consider $\Delta\phi$ the phase difference between modulating signals of two inverters ($m_1(t)$ and $m_2(t)$). We observe these critical cases when the phase difference of inverters forms a balanced system ($\Delta\phi = \pi$ for two inverters, $\Delta\phi = 2\pi/3$ for three inverters, etc.). Lateral band components fall down and tend to cancel themselves. This is normal, considering (15). Equations (18) and (19) give the images of output voltage for two inverters operating (with $\Delta\phi = 0$ or π). The sidebands tend to cancel themselves when operating together, and we get residual values at PCC.

$$s_1(t) \approx \cos(\omega_{inv}t) - \frac{\beta}{2a} \cos\left(\frac{\omega_{inv}}{2}t\right) + \frac{\beta}{2a} \cos\left(\frac{3\omega_{inv}}{2}t\right) \quad (18)$$

$$s_2(t) \approx \cos(\omega_{inv}t) - \frac{\beta}{2a} \cos\left(\frac{\omega_{inv}}{2}t + \pi\right) + \frac{\beta}{2a} \cos\left(\frac{3\omega_{inv}}{2}t + \pi\right) \quad (19)$$

The reference signal $s(t)$ of inverters operating in the grid must get the same phase angle to be well synchronized. Synchronization of inverters with the grid must be achieved by the same modulating signal $m(t)$. Each PVS introduces sidebands at any positive zero cross of PLL responsible of the grid recovery. Therefore, only results obtained with $\Delta\phi = 0$ must be considered. The DGs even if different can use this approach for islanding protection.

Every DG just needs to modulate its inverter output signal as recommended.

4.4 Simulation of PVS with islanding detection and adaptive loads shedding

The goal of the proposed adaptive algorithm presented in Sect. 3.2 is to ensure an uninterrupted supply for priority loads. After islanding detection, overloads shedding operates to avoid destruction of the PVS. One case is presented in Fig. 15. We consider constant sunlight irradiation and temperature that provide a power S_D in the PVS (about 15 kVA). Overloads are disconnected from the PVS, and V_{PCC} recovers its normal characteristics in less than 20 ms after islanding confirmation. This duration depends on the speed of protection devices. The reserve power S_D is then kept above the power required to supply remaining loads. The time frame of the degradation of the power quality is only 0.1 s. We have set T_D at 80 ms since we are using single-phase inverter. During this period, we observe a voltage sag caused by a lack of power in the PVS when supplying the three loads after islanding. A sag must effectively appear in case of great mismatch of power after islanding as explained in (6). It is the case presented. The PVS will stop energizing when remaining loads will need more power than the one on reserve.

Table 3 Comparison of modulation approach with recent similar methods

AIP techniques	Harmonic profile injection	Reactive power disturbance	Reactive power injection and ROCOF	Locking frequency band detection	Ripple voltage content	Proposed approach
Detection time (electrical cycles)	8	4–26	15–25	28–35	18	5
Disturbance applied and effect on power quality	4% voltage harmonic: high degradation (THD=4.94)	4%ΔQ: low degradation, unbalanced system phasors	Repetitive ΔQ with ROCOF: low degradation after faults	Frequency error and bandwidth limit: very low degradation	No degradation since it is a passive method	0.15% Voltage inter-harmonic: very low degradation
Monitoring criterion and resources used	Loop, filter, ROCOF	Depending on loads scenarios, two sets of ΔQ	dQ/df, ROCOF, Q-f load curve, three sets of ΔQ	f, Robust PLL, high	Voltage ripple content at PCC	Voltage sidebands V_L and V_H at PCC
Reliability and multiple DGs effect	Need OVP/UVP, synchronization issues	Need OFF/UFP, synchronization issues	Need OFF/UFP	Need OFF/UFP	Depends on grid and inverter parameter	Depends on inverter parameter only
NDZ	None	None	None	None	None	None

Fig. 14 Multiple PVS scenario

Increased adaptiveness and speed of this loads shedding scheme is under consideration for future scope of this paper in view to reduce, for example, voltage sags described in [25–27]. We would also develop historical database of loads consumption in view to make it also predictive.

5 Conclusion

This paper proposes a new islanding detection strategy based on frequency modulation of a grid-connected PVS output voltage. The technique has been proved better than recent others in terms of speed, simplicity and reliability. It is among the fastest active anti-islanding techniques, with a time detection of 100 ms. The present technique has been tested using IEEE and UL standards. It has very low impact in power quality since it meets the recommended 0.2% interharmonic threshold. Throughout our work, THD values remain very low even during islanding operation (between 2 and 3% during the main tests). In normal operation (before islanding), THD is less than one (depending on the output inverter filter) and the sidebands influence on TDR is at most 0.2. All the values are within the limits of IEEE-519 standards and recommendations [23, 25, 28, 29]. This technique is coupled to a simple adaptive loads shedding algorithm to manage islanding. Adaptive loads shedding allows the quasi-permanent supply of priority loads by the PVS. This is done about 20 ms after the confirmation of the islanding. The continuous supply of priority loads is then made after a transient phase of about 0.1 s characterized by a voltage sag.

Table 4 Multiple PVSs scenario

m	$\Delta\phi$ (rad)	Type of load	P (kW)	Q_L, Q_C (kVAR)	V_0 (V ²) before/after
3	$2\pi/3$	R	25	0	0.41 3.14
		RLC: $Q_f=0.2$	10	+12, -12	1.80 7.82
		4 diodes bridge: $R=4\ \Omega$			1.18 7.56
	0	RLC: $Q_f=1$	15	+15, -15	3.87 182
	0	RLC: $Q_f=2.5$	32	+80, -80	4.23 20.5
2	π	R	25	0	0.11 0.12
	0				3.6 100
	0	RLC: $Q_f=2.5$	32	+80, -80	4.6 23

Fig. 15 Apparent powers flowing through the island when islanding happens

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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