Research Article

Recital analysis of multilevel cascade H-bridge based active power filter under load variation

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Abstract
This paper investigates a 13-level cascaded H-bridge (CHB) converter for shunt active power filter (SAPF) application to minimize the total harmonic distortion (THD) of source current under load variation. The converter configuration comprises of six H-Bridge cells per leg. Carrier-based phase disposition PWM is used as a modulation strategy to control the switches of 13-level CHB topology. An instantaneous real and reactive power technique based harmonic current extraction method is implemented to extract the reference currents. The proportional-integral controller is implemented to control the DC voltage of the SAPF. The proposed 13-level CHB SAPF performance is compared with two-level voltage source SAPF, three-level CHB SAPF, five-level CHB SAPF and nine-level CHB SAPF. The proposed work is implemented using Matlab/Simulink. The comparative performance analysis of THD, harmonics, active power, reactive power and power factor are presented.

Keywords Cascade H-bridge · Phase disposition · Power factor · Instantaneous real and reactive power technique (IPQT) · Reactive power compensation (RPC) · Total harmonic distortion (THD)

1 Introduction

Recently multilevel active power filters are very attractive due to modularity structure for medium voltage and high power application under non-linear load conditions. Conventionally, voltage source inverter for SAPF application is reported in literature, but they produce more harmonics due to square wave output [1, 2]. Later, the combination of VSI and passive filter based SAPF are reported in literature for power quality improvement [3–7]. A hybrid compensator with 3-level and the 5-level CHB are presented to reduce reactive power and harmonics for the railway traction system [8]. The predictive current control method is adopted for 5-level CHB using phase shifted space vector modulation [9] for power quality improvement. Various SAPF configurations; three-leg-inverter-based SAPF, single CHB SAPF, two CHB SAPF and four CHB SAPF are presented its comparative performance of harmonic reduction for an aircraft electric application [10]. The five-level CHB based SAPF with low carrier frequency pulse width modulation is presented to mitigate harmonics in aerospace applications [11]. Single phase five-level CHB with the model based controller is presented to reduce the current distortions under non-linear loads [12]. The level shift carrier based phase disposition (PD) method is proposed and presented in [13–17]. In this paper, thirteen-level CHB based SAPF is proposed to reduce source current THD. The detailed configuration of proposed SAPF is presented in Sect. 2. The multilevel inverter concept for SAPF application, the reference current generation method and the modulation scheme is explained in Sect. 2. The performance of proposed SAPF is discussed and compared with the conventional system using simulation results in Sect. 3. Finally, the conclusions were made in Sect. 4. The configurations of one CHB, two CHB, four-CHB, and six CHB are

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represented with HB1, HB2, HB4, and HB6 respectively for simplicity in this paper. The suffix '*a*', '*b*', and '*c*' represents the phase '*a*', phase '*b*', and phase '*c*' respectively.

2 Shunt active power filter

The CHB SAPF can compensate the reactive power and mitigate the harmonics in the power system. The single line block diagram of proposed SAPF is shown in Fig. 1. It consists of a 3-phase supply, non-linear (NL) load and SAPF. A three phase uncontrolled bridge with the RL load is used as NL load. The symbol V_s, V_m, V_{dc}, L_f, i_L, i_s, and i_c is the source voltage, peak voltage, capacitor voltage, filter inductance of SAPF, load current, source current, and filter current respectively. The 3-phase supply, NL and SAPF are connected at the point of common coupling (PCC) as shown in Fig. 1.

The instantaneous source voltage is written as

$$V_{Sa}(t) = V_m \sin \omega t \tag{1a}$$

$$V_{Sb}(t) = V_m \sin (wt - 120^\circ) \tag{1b}$$

$$V_{Sc}(t) = V_m \sin (wt - 240^\circ) \tag{1c}$$

The NL load current is calculated using (2) which include both fundamental and harmonic currents.

$$i_L(t) = I_1 \sin \left(n\omega t + \emptyset_1\right) + \sum_{k=2}^{\infty} \sin \left(k\omega t + \emptyset_k\right) \tag{2}$$

From Fig. 1, the load current in terms of source current and compensator current is given in (3).

$$i_L(t) = i_s(t) + i_c(t) \tag{3}$$

2.1 Multilevel inverter

An inverter, which is having more than 2-levels in output voltage, is called multilevel inverter (MLI). The harmonic content in both voltage and current can be mitigated with a higher voltage levels. The MLIs are very attractive in the application of SAPF due to this advantage. Three types of MLIs include diode clamped (DC), capacitor clamped (CC),

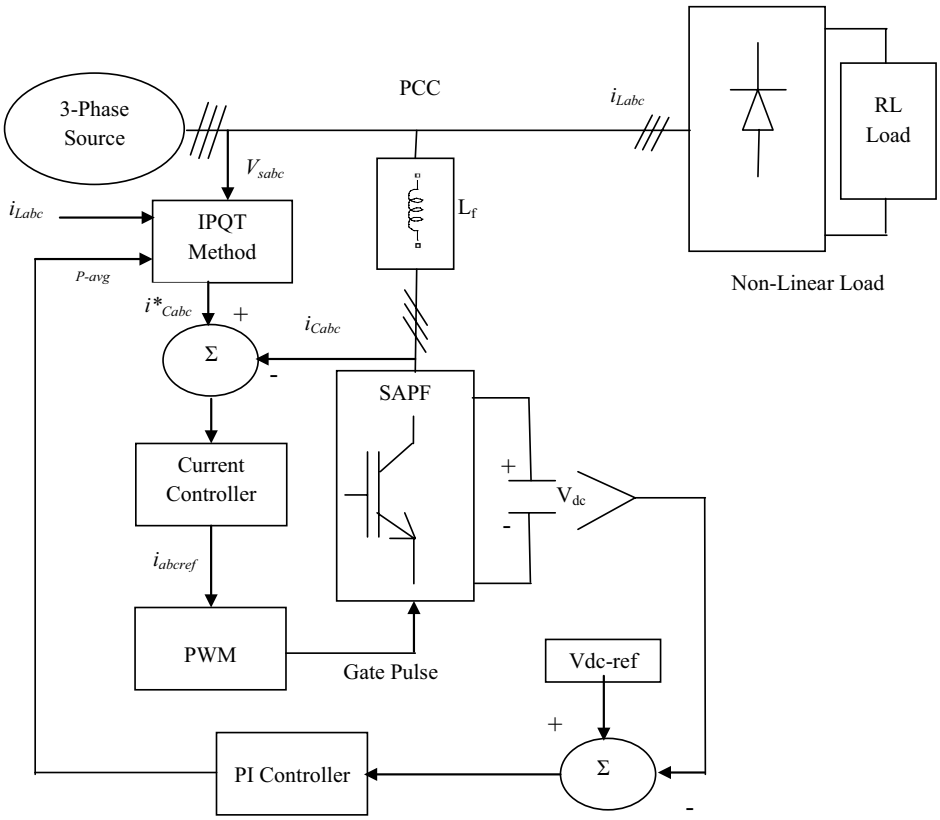
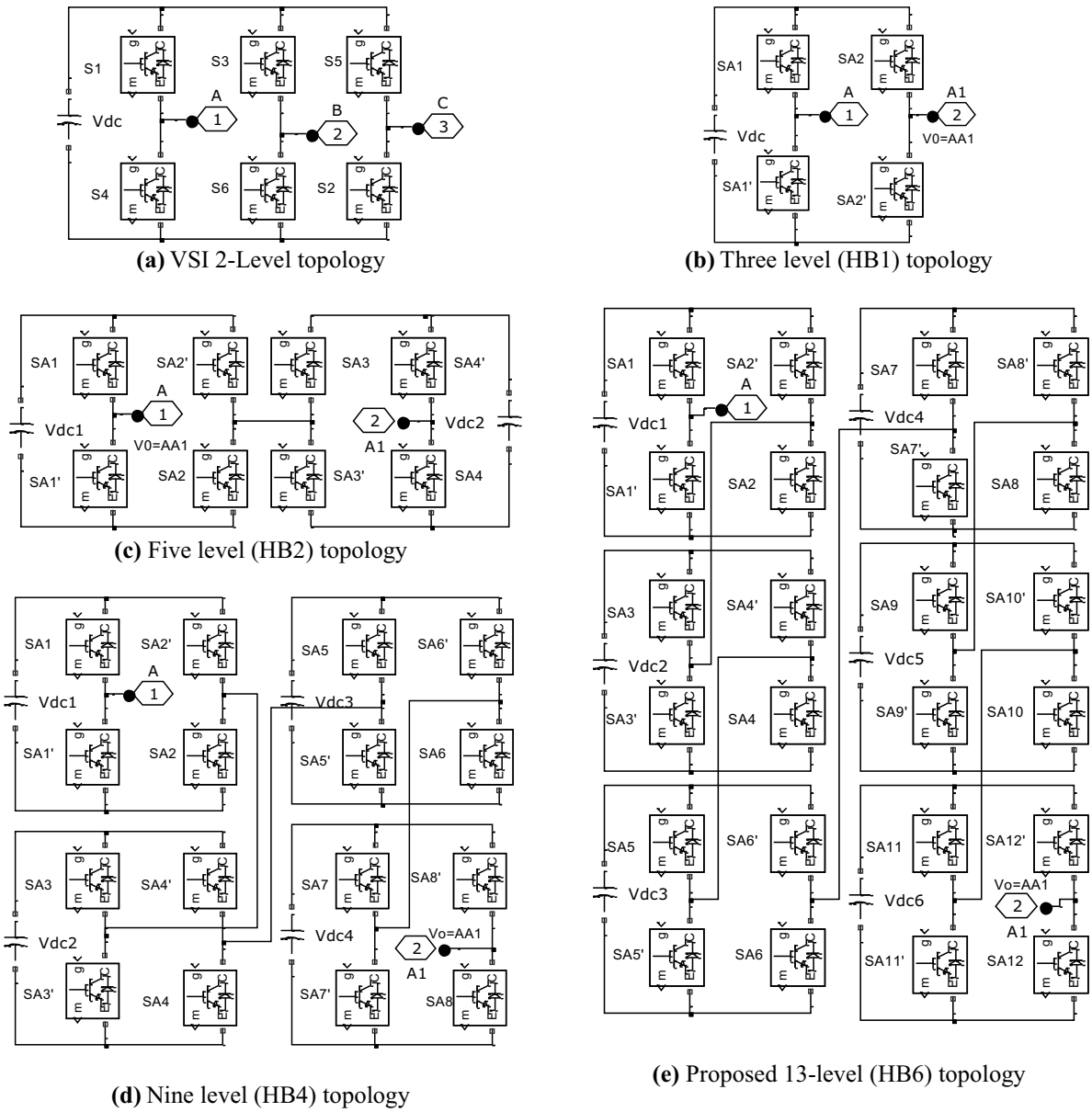


Fig. 1 Single line block diagram of SAPF configuration

and the cascaded H-bridge (CHB) configurations are suitable for an application of SAPF [18]. CHB MLI based SAPF configuration is proposed due to its superior merits such as component reduction, no clamping diodes, no clamping capacitors and modularity in structure compared to other two configurations. The schematic diagram of VSI 2-level is shown in Fig. 2a [19]. The different topologies includes HB1, HB2, HB4, and HB6 per leg is shown in Fig. 2b–e. HB6 inverter consists of six capacitors at the DC bus and produces thirteen-levels on the phase. For a DC bus voltage (V_{dc}), an individual capacitor voltage is calculated using Vdc/(m – 1). The thirteen-levels of output voltages are $6V_{dc}$, $5V_{dc}$, $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, −2Vdc, $-3V_{dc}$, $-4V_{dc}$, $-5V_{dc}$ and $-6V_{dc}$ respectively. An output voltage is produced with switch 'ON' of S_{A1}, S_{A2}, S_{A3}, S_{A4}, S_{A5}, S_{A6}, S_{A7}, S_{A8}, S_{A9}, S_{A10}, S_{A11}, S_{A12} and its complementary switches with different combination. Thus, the minimum of twelve switches will be turned 'ON' per phase for producing thirteen-level output voltage. The possible switching states for one leg thirteen-level CHB inverter is presented in Table 1.



(a) VSI 2-Level topology

(b) Three level (HB1) topology

(c) Five level (HB2) topology

(d) Nine level (HB4) topology

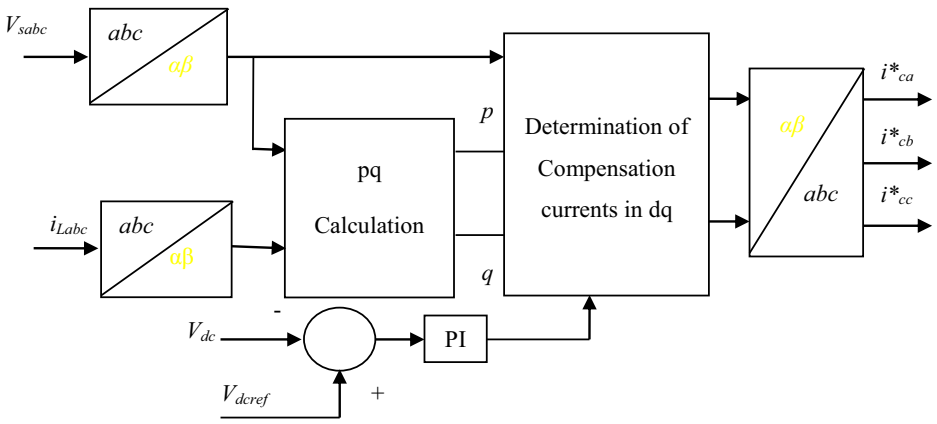
(e) Proposed 13-level (HB6) topology

Fig. 2 Diagram of CHB topologies per leg

Table 1 13-level CHB inverter switching states (for Fig. 2e)

V_0	6Vdc	5Vdc	4Vdc	3Vdc	2Vdc	Vdc	0	−Vdc	−2Vdc	−3Vdc	−4Vdc	−5Vdc	−6Vdc
SA1	1	0	0	0	0	0	0	0	0	0	0	0	0
SA2	1	1	0	0	0	0	0	0	0	0	0	0	0
SA3	1	1	1	0	0	0	0	0	0	0	0	0	0
SA4	1	1	1	1	0	0	0	0	0	0	0	0	0
SA5	1	1	1	1	1	0	0	0	0	0	0	0	0
SA6	1	1	1	1	1	1	0	0	0	0	0	0	0
SA7	1	1	1	1	1	1	1	0	0	0	0	0	0
SA8	1	1	1	1	1	1	1	1	0	0	0	0	0
SA9	1	1	1	1	1	1	1	1	1	0	0	0	0
SA10	1	1	1	1	1	1	1	1	1	1	0	0	0
SA11	1	1	1	1	1	1	1	1	1	1	1	0	0
SA12	1	1	1	1	1	1	1	1	1	1	1	1	0
SA1′	0	1	1	1	1	1	1	1	1	1	1	1	1
SA2′	0	0	1	1	1	1	1	1	1	1	1	1	1
SA3′	0	0	0	1	1	1	1	1	1	1	1	1	1
SA4′	0	0	0	0	1	1	1	1	1	1	1	1	1
SA5′	0	0	0	0	0	1	1	1	1	1	1	1	1
SA6′	0	0	0	0	0	0	1	1	1	1	1	1	1
SA7′	0	0	0	0	0	0	0	1	1	1	1	1	1
SA8′	0	0	0	0	0	0	0	0	1	1	1	1	1
SA9′	0	0	0	0	0	0	0	0	0	1	1	1	1
SA10′	0	0	0	0	0	0	0	0	0	0	1	1	1
SA11′	0	0	0	0	0	0	0	0	0	0	0	1	1
SA12′	0	0	0	0	0	0	0	0	0	0	0	0	1

Fig. 3 IPQT METHOD



2.2 Reference current generation

Time domain based reference current extraction method of an instantaneous real and reactive power technique (IPQT) is implemented for computation of reference currents [14, 20] as shown in Fig. 3.

abc to αβ conversion of source voltage is given by (4)

$$\begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = [0.8165] \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (4)$$

abc to αβ conversion of load current is given by (5)

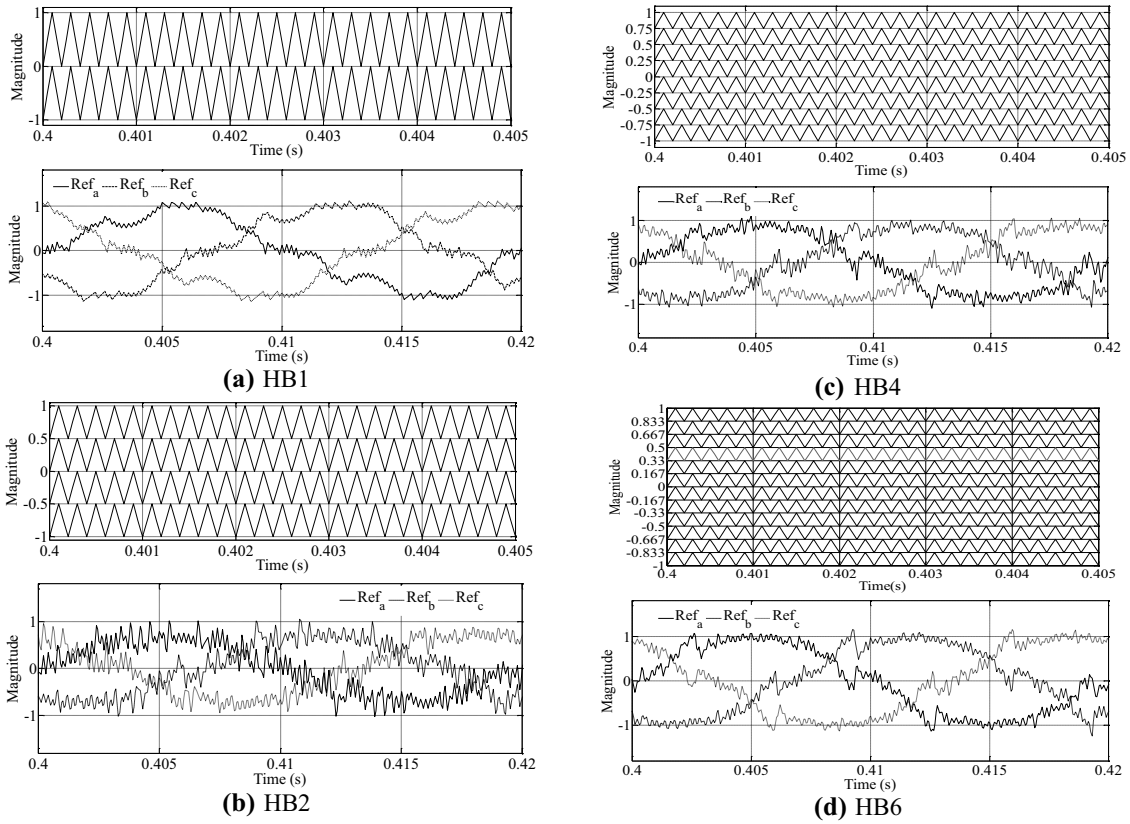


Fig. 4 Carrier signal and generated reference signal

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = [0.8165] \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{5}$$

The real and reactive power (pq) computation is as follows:

Table 2 Simulation parameters

S. no.	Description	Value
1.	3-Phase supply voltage	440 V (rms)
2.	L_s and R_s	2e−5H, 0.01 Ω
3.	Non-linear load	Three phase diode bridge with RL load
4.	R_{L1}	50 Ω
5.	L_{L1}	110 mH
6.	R_{L2}	37.5 Ω
7.	L_{L2}	82.5 mH
8.	Switching frequency	5000 Hz
9.	V_{dcref}	720 V
10.	Capacitor, C_{dc}	3300 μF
11.	PI controller	$k_p = 10$, $k_i = 0.5$

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} V_{s\alpha} & V_{s\beta} \\ -V_{s\beta} & V_{s\alpha} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{6}$$

The controlled real and reactive power is calculated using (7)

$$p_c = p + p_{loss}, \text{ and } q_c = -q \tag{7}$$

The compensation current in αβ quantities is calculated using (8)

$$i_{c\alpha} = \frac{p_c * v_{s\alpha} + q_c * V_{s\beta}}{V_{s\alpha}^2 + V_{s\beta}^2}, \quad i_{c\beta} = \frac{p_c * v_{s\beta} - q_c * V_{s\alpha}}{V_{s\alpha}^2 + V_{s\beta}^2} \tag{8}$$

The reference currents are converted from αβ components to abc using (9)

$$\begin{bmatrix} i_{ca}^* \\ i_{cb}^* \\ i_{cc}^* \end{bmatrix} = [0.8165] \begin{bmatrix} 1 & 0 \\ -0.5 & 0.866 \\ -0.5 & -0.866 \end{bmatrix} \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \tag{9}$$

2.3 Modulation method

The level shift (LS) PWM is used to control the switches. PD triangular carriers and generated reference signals is illustrated in Fig. 4 and is implemented for control of switches in proposed SAPF configuration.

The pulse is generated using Fig. 4. The terms Ref_a, Ref_b, and Ref_c are the reference signals for pulse generation in phase-a, phase-b, and phase-c respectively. The pulse is generated based on condition that the pulse is available if reference signal is greater than carrier signals otherwise it is zero. The triangular carriers are selected using (10)

$$m - 1 \tag{10}$$

where '*m*' is the number of levels.

2.4 DC link voltage balancing method

The minimum values of parameters for PI technique to balance dc voltage can be determined by

$$K_p \geq 2C\xi\omega \tag{11}$$

$$K_i \geq C\omega \tag{12}$$

where k_p, k_i, C, ξ and ω are proportional constant, integral constant, capacitance of active power filter, damping coefficient (0.707) and system frequency respectively.

3 Simulation result and discussion

In this section, the simulation result analysis is carried out for SHB SAPF compensation. The proposed compensation method using Fig. 1 is validated with simulation results. The simulation parameters and its values are listed in the Table 2.

Waveforms for uncompensated system are shown in Fig. 5. The source current has produced square wave due to non-linearity in the load as shown in Fig. 5a. The PF of the system is 0.7462, and the reactive power is 2637 Var. Source current has produced its THD of 24.39% due to more harmonics presented in 5th, 7th, 11th and 13th, as shown in Fig. 5f.

The two-level voltage source inverter based SAPF response curves are presented in Fig. 6. It is observed that, the PF is improved to 0.9876, the real power (*P*) and reactive power (*Q*) is also improved. The THD is reduced from 24.39 to 11.94%. Various levels of cascade H-bridge inverter based SAPF is simulated and the response curves are presented in Figs. 7, 8, 9, and 10

The simulation results of HB1, HB2, HB4 and HB6 based SAPF using an IPQT, and PIC is presented in Figs. 7, 8, 9, and 10. The proposed HB6 SAPF has good performance compared to traditional configurations. From Fig. 10, it is observed that the PF and the reactive power of the system are improved. The harmonics presented in

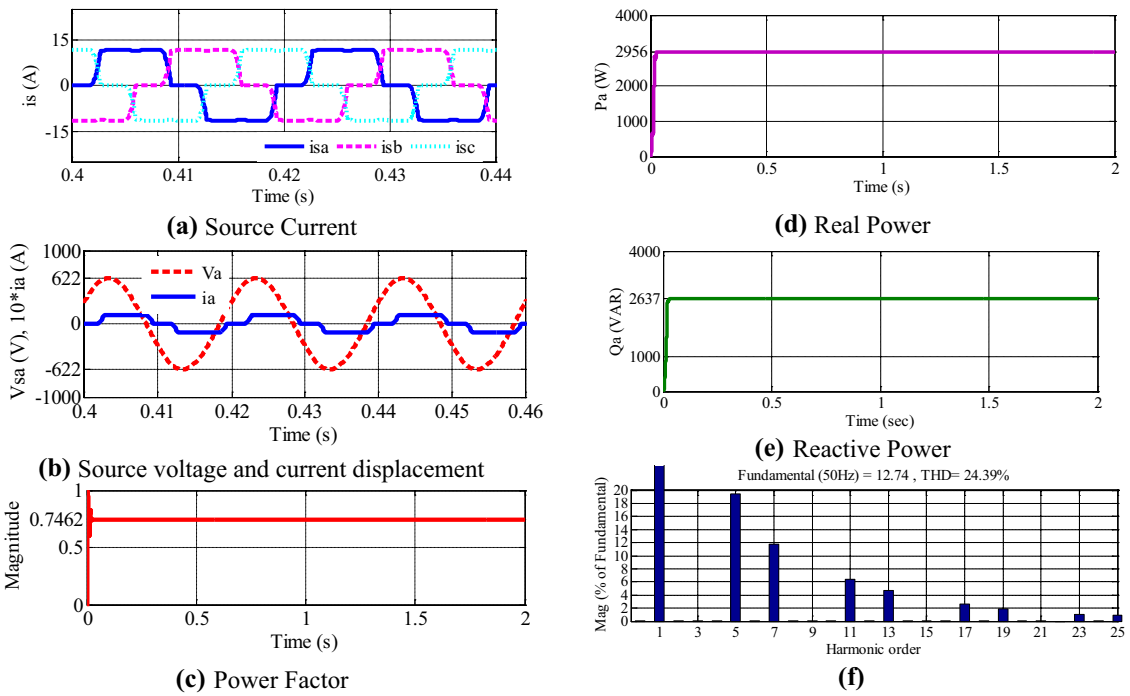


Fig. 5 Response curves of uncompensated system

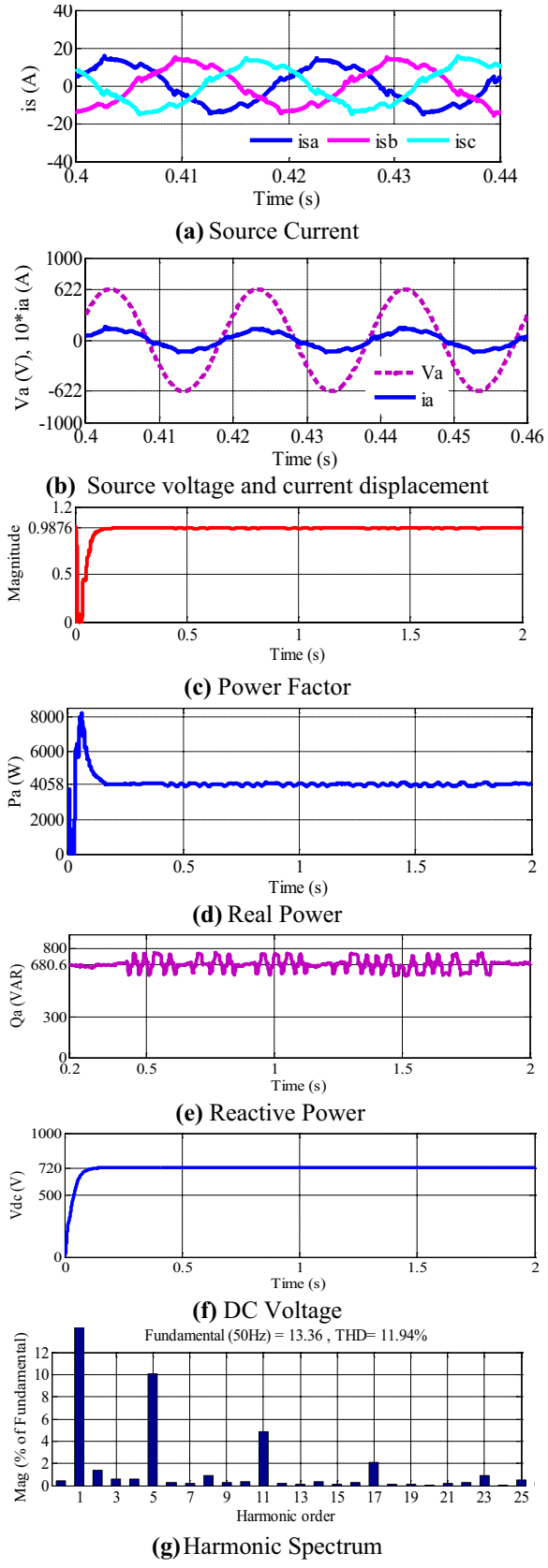


Fig. 6 Response curves using two-level VSI topology

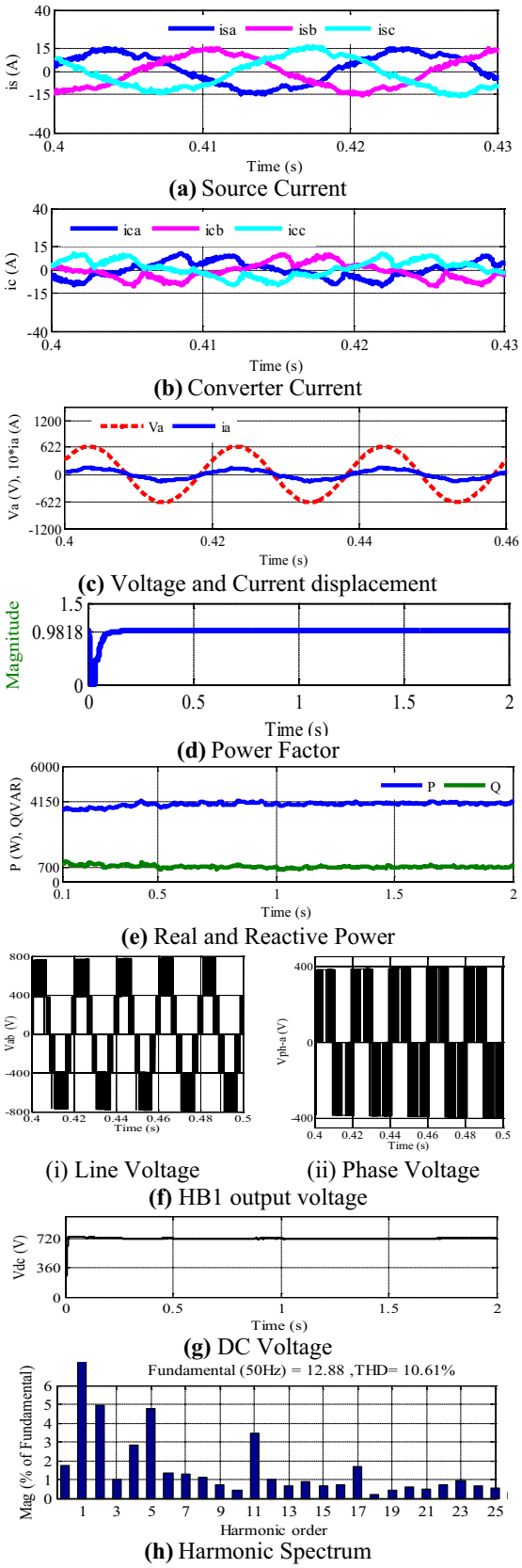


Fig. 7 Response curves using HB1 topology

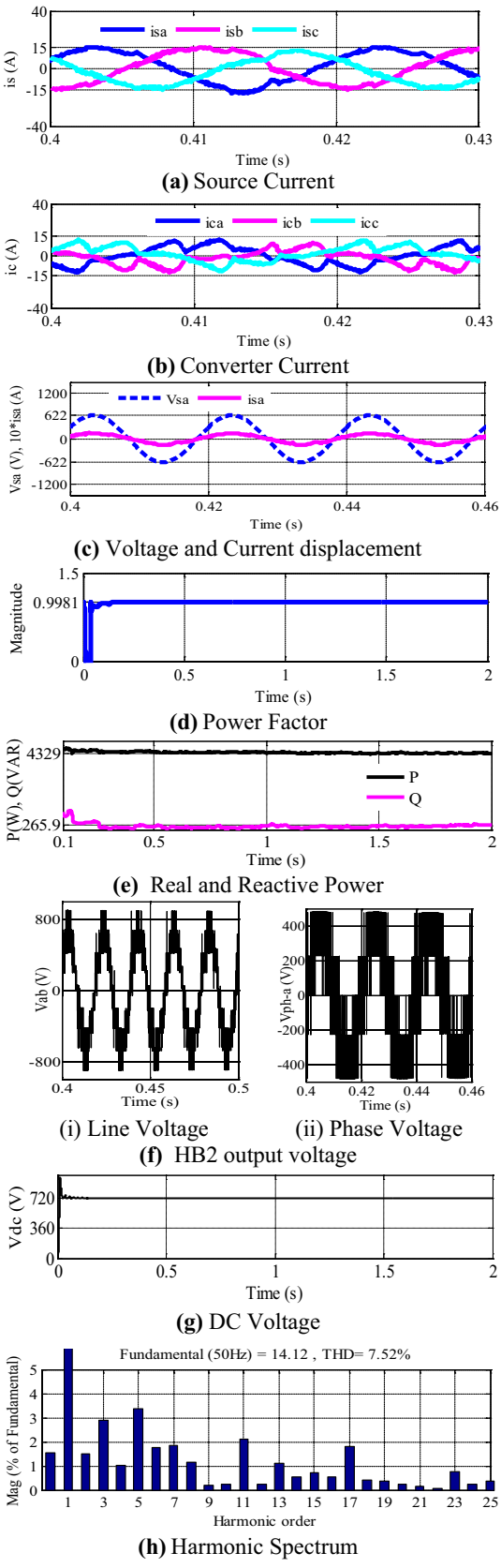


Fig. 8 Response curves using HB2 topology

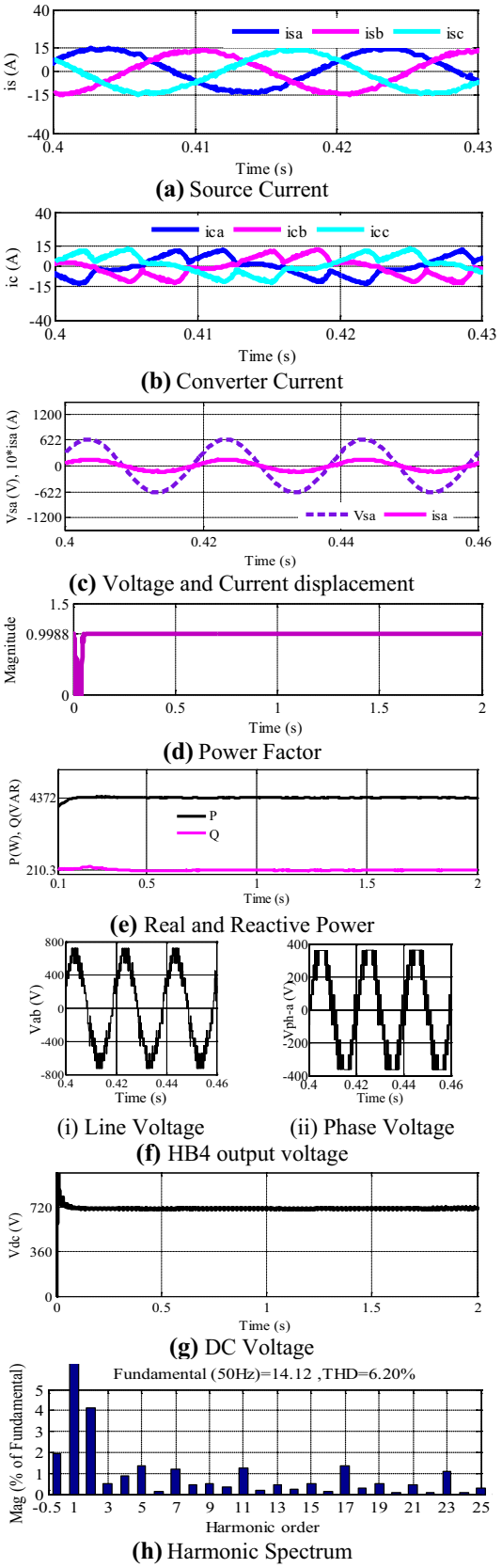
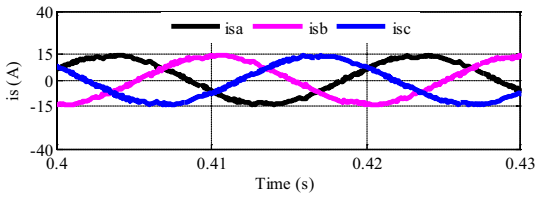
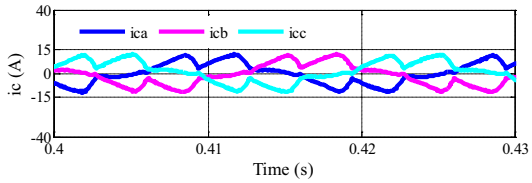


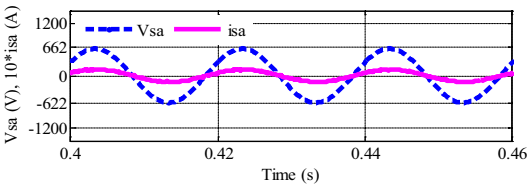
Fig. 9 Response curves using HB4 topology



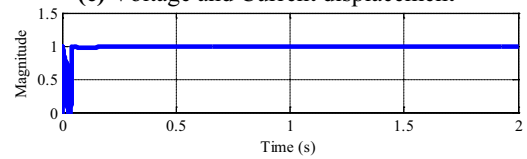
(a) Source Current



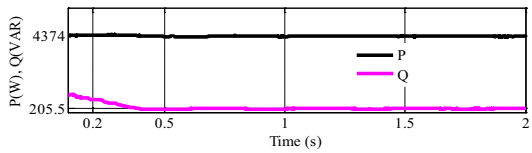
(b) Converter Current



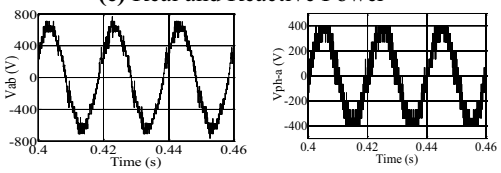
(c) Voltage and Current displacement



(d) Power Factor

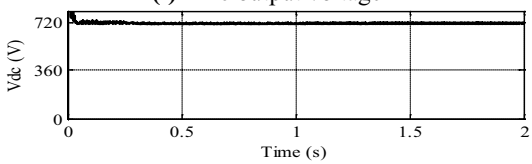


(e) Real and Reactive Power

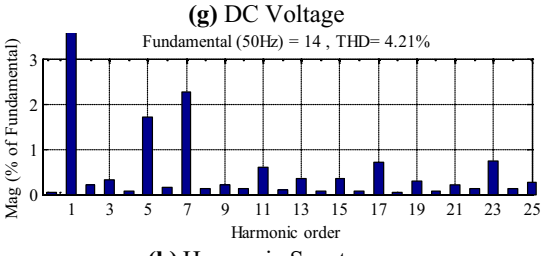


(i) Line Voltage (ii) Phase Voltage

(f) HB6 output voltage



(g) DC Voltage



(h) Harmonic Spectrum

Fig. 10 Response curves using HB6 topology

Table 3 Simulation result comparison

Parameter	Before compensation (BC)	VSI 2-Level SAPF	HB1	HB2	HB4	HB6
Pa (W)	2956	4058	4150	4329	4372	4374
Qa (VAR)	2637	680.6	700	265.9	210.3	205.5
PFa	0.7462	0.9876	0.9818	0.9981	0.9988	0.9989
i_{sa} (A)	12.74	13.36	12.88	14.12	14.12	14.00
Source current Harmonics in percentage values						
I_{h5}	19.4	10.10	4.74	3.37	1.34	1.70
I_{h7}	11.81	0.22	1.27	1.85	1.22	2.28
I_{h11}	6.45	4.84	3.47	2.10	1.25	0.6
I_{h13}	4.69	0.10	0.67	1.13	0.46	0.35
THD	24.39	11.94	10.61	7.52	6.20	4.21

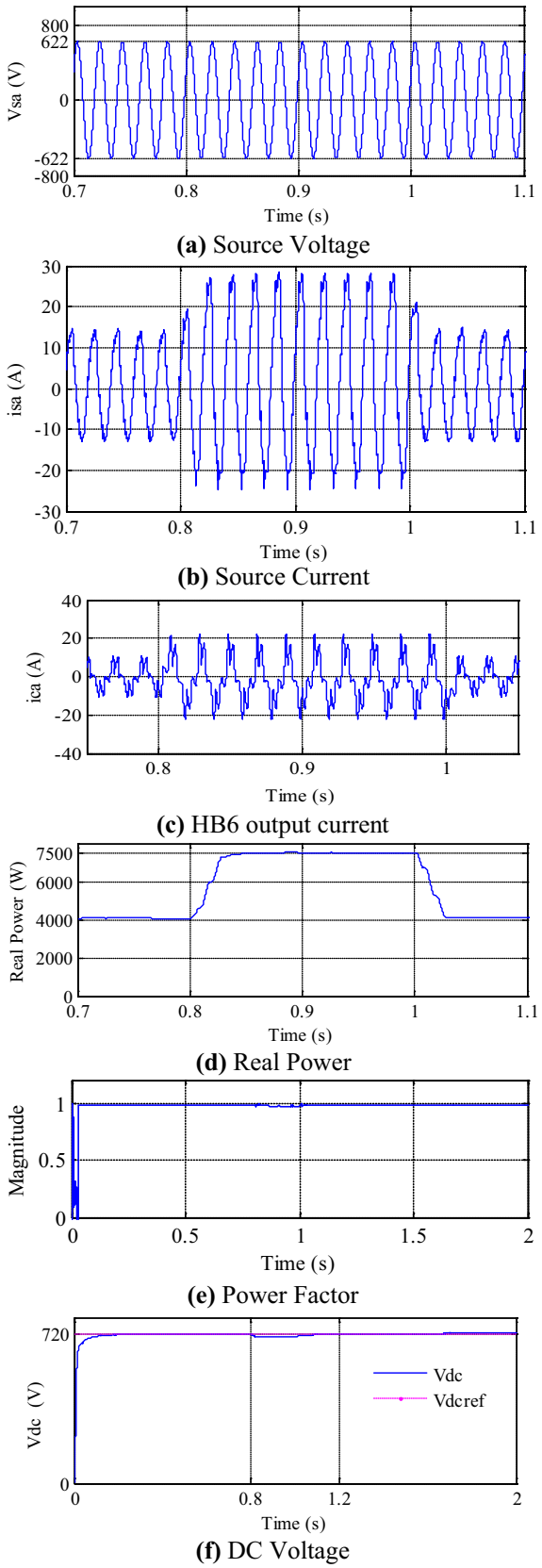


Fig. 11 Response curves using HB6 under load variation

5th, 7th, 11th and 13th are reduced with the proposed CHB topology. The reduction of harmonics in source current is satisfying the IEEE standards. The total DC link voltage is also balanced using proposed control method as shown in Figs. 7g, 8g, 9g, and 10g. The complete simulation result comparison is presented in the Table 3.

Further the simulation work is extended to load variation to validate the performance of proposed HB6 SAPF configuration and its response curves are shown in Fig. 11. Proposed HB6 configuration is simulated under load variation to validate its performance in SAPF application. Another load is connected at t = 0.8 s and disconnected at t = 1 s. The performance of proposed HB6 SAPF has well under load variation and its response curves are shown in Fig. 11.

4 Conclusions

The proposed CHB SAPF is simulated and the results are discussed clearly. THD in Source current is reduced from 24.39 to 4.21%. The PF is improved from 0.7462 to 0.9989 and reactive power is reduced from 2637 to 205.5 Var. The harmonic mitigation and reactive power compensation is achieved with proposed CHB SAPF.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflicts of interest.

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