Low power device design application by magnetic tunnel junctions in Magnetoresistive Random Access Memory (MRAM)

S. Hamsa¹ · N. Thangadurai¹ · A. G. Ananth²

© Springer Nature Switzerland AG 2019

Abstract

The spintronics techniques combines the spin degree and charge which gives rise to state of the art devices like magnetic tunnel junctions which are ultra-low power devices. It is proposed in the paper to evaluate magnetic tunnel junctions (MTJ) at the device level. The paper present an overview of fabrication process, while considering different aspects of the characteristics of MTJs, performance, challenges and a wide range of applications which are different from conventional CMOS technology. The MTJ devices are CMOS compatible for non-volatility, high stability and reliability. The MTJ device is a promising candidate for building non-volatile circuits for ultra- low power operation and fast switching speeds. The current approaches to design logic functionalities and memory devices with MTJs w include hybrid CMOS and MTJ circuits are also discussed in the paper. The results on the most robust magnetic tunnel junction with Resistance Area = $8 \Omega\text{-}\mu\text{m}^2$ demonstrates that it satisfies the statistical requirements in parallel with high magnetic tunnel resistance greater than $15\sigma(R_p)$, breakdown-of voltage to edge more than 0.5 V, read-induced rate beneath 10^{-9} , and with adequate write endurance, free of undesirable write endurance magnetic inversion. Also this paper demonstrates on the most vigorous MTJ with Resistance Area = $8 \Omega\text{-}\mu\text{m}^2$ that satisfies the statistical requirements in parallel with high magnetic tunnel resistance greater than $15\sigma(R_p)$, breakdown-of voltage to edge more than 0.5 V, read-induced rate less than 10^{-9} , and with adequate write endurance, and is free of undesirable write endurance magnetic inversion.

Keywords Magnetic tunnel junction · MRAM · Spin valve · Spin polarization · Ferromagnetic resistance area · Write endurance

1 Introduction to MTJs and MRAMs

1.1 Magnetic tunnel junction (MTJs)

Due to the advancement in the micro chip engineering, one of the limiting factors in making the circuit smaller with shrinking transistor today is generation of heat. So shrinking the transistor though is manageable but the functionality cannot be ensured due to this factor. As the channel length is shrunk below 45 nm, the leakage currents increases finally resulting in increased power consumption. The power consumption is one of the major challenges in VLSI design and in order to address this issue a novel

approach that is derived from spintronics has been evolved in which the CMOS technology is replaced by Magnetic Tunnel Junction (MTJ) that supports continuous scaling.

There are two foremost characteristics of an electron namely 'charge' and 'spin' and the magnetism is due to the spin character of the electron. Spins in semiconductors offer a new approach towards integration of information storage and processing in a single material. Such devices in which both the electronic charge and as well as its magnetic moment (spin) are studied together are called as spintronic devices or spin electronics devices [1].

Tunneling is a nano-scale phenomenon where under the right conditions, electrons can tunnel to very thin

✉ N. Thangadurai, mrgoldjain2015@gmail.com | ¹Electronics and Communication Engineering Department, JAIN (Deemed-to-be University), Bangalore, India. ²Electronics and Communication Engineering Department, NMAMIT, Nitte, Udupi, India.

Fig. 1 Cross section of magnetic tunnel junction [5]

insulating materials causing load resistance, such structures are called Magnetic Tunnel Junction (MTJ) or Tunneling Magneto Resistance (TMR). MTJ is a spin based device showing non volatile characteristics working with principle of Magnetoresistance (MR). Magnetoresistance is a phenomenon in which the property of the material will change its electrical resistance when an external magnetic field is applied to it. MR effect is basically the property of materials causing resistance change due to magnetic field and it occurs in materials like magnetic, semiconducting and insulating materials. MR operates without any physical contact and can be used in sensors, hard disk drives and measuring electric current [2–4].

1.2 MTJ device structure

The MTJ material stack comprises layers of ferromagnets divided by an ultra-thin dielectric layer. The dielectric layer between the ferromagnets is in nanometer range leading the junctions into thin vertical nanostructures. Figure 1 shows the cross section of magnetic tunnel junction, the upper layer is called as free layer in which the magnetic orientation in this layer can be changed freely. While the lower layer is called pinned or reference layer, the spin orientation is fixed in the layer while the device is manufactured. The barrier between the pinned and free layer is thin enough, that electrons can tunnel through and offers some resistance even if the layer is insulating.

The pinned layer is much thicker compared to free layer, large exchange Bias energies and high blocking temperature are required as the layer have fixed magnetic orientation with reference to free layer. The pinned layer consists of two sub layers separated by Ruthenium (Ru) film to form anti ferromagnet structure. This stack structure helps to eradicate the magnetostatic field in the free layer [6, 7].

1.3 Types of MTJs

MTJ comprises of two nano magnets separated by a thin insulator layer. The two layers actually behave like magnets particularly. The fixed nano magnet in which the configuration (magnetic orientation) is fixed and the other is free nano magnet in which the configuration of the magnet

Fig. 2 Types of MTJs [5]

can be changed. There are two configurations namely parallel and anti-parallel configurations, the confirmation of the free layer with respect to pinned layer can be of two ways that defines two variations of MTJs namely in-plane MTJ and perpendicular MTJ as shown in Fig. 2.

These two types of MTJs differ in properties offering diverse Tunnelling Magnetoresistance Ratio (TMR). The TMR ratio depends on the configurations of the two magnets and the conduction varies drastically depending on the in-plane and perpendicular MTJ. There are other properties of MTJ as well like stability factor (D), switching current. TMR ratio also depends on the materials used for the barrier, earlier amorphous barriers had low TMR ratio but recent developments have high TMR ratio with crystalline junction with MgO barrier. High TMR ratio gives best results for change of states.

1.4 MTJ operation

MTJ works on the basic principle of Tunnel Magnetoresistance (TMR) which is due to spin based tunneling. TMR effect occurs when two ferromagnetic layers are separated by an insulator layer made of oxide. The two ferromagnetic layers have magnetic orientation within them, the orientation in free layer is free to change and hence the name free layer while the orientation of magnetic field in reference is fixed. The magnetic orientation in the layers depends on the conductance of the resistance in the layer [8–10]. In an MTJ there exist two states of conduction namely parallel and anti-parallel states. In parallel state the magnetic field orientation in free and reference layer are in the same direction, while in anti-parallel the magnetic field orientation in free layer is opposite to that of reference layer. The resistance offered by MTJ in its parallel state is lesser when compared to the resistance offered by the MTJ in its anti-parallel state of operation [2]. The lower resistance i.e. parallel state electrical resistance (R_p) is considered as state “1”, while the higher resistance i.e. Anti-parallel state electrical

Fig. 3 TMR effect

Fig. 4 Parallel and anti-parallel switching

resistance (R_{ap}) is considered as state “0”. The corresponding TMR ratio is defined as:

$$TMR = \frac{R_{ap} - R_p}{R_p} \quad (1)$$

Fig. 5 a MRAM operation window. b Voltage division to access transistor and MTJ. c VI characteristics of MTJ

The electrical resistance and the state of MTJ is shown in Fig. 3

Using the STT scheme, writing on to the MTJ can be used in circuit design as a current or bias voltage controlled inconsistent resistance [11–13]. In Fig. 4 one can observe how the tunneling probability will be different in the parallel configuration or in the anti-parallel:

- Parallel configuration.
- Anti-parallel configuration.

In the case of a parallel configuration as shown in Fig. 5a the spins down (blue arrows) are minority spins in both Ferromagnets and, according to the second assumption have a low tunneling probability, while the spins up -majority on both Ferromagnets, red arrows- have a high tunneling probability. In the case of the Anti-parallel configuration Fig. 5b spins up and down are majority in one ferromagnet and minority in the other; therefore, the tunneling probabilities for both are normal. This means that in a parallel configuration tunneling are more common than in the anti-parallel configuration, resulting in the lower resistance in the parallel state encountered in Fig. 4. This difference in the resistance, depending on the magnetization of two Ferromagnets is being used in many commercial hard drives and solid state memories to store information. Basically, the parallel/anti-parallel states constitute a ‘bit’ of information (1/0) which can be read due to the difference in resistance.

2 Design properties of MTJ

The thickness of MTJ-RAM [14] compared to that of DRAM is more aggressive. MTJ MRAM consumes less power and is also very adaptable compared to regular field-MRAM [3]. The designed MTJ-MRAM gives adequate measurable limits compared with existing FLASH memory and fulfills the intersection long haul unwavering quality necessities.

Fig. 6 MRAM cell

There are five key design properties for STT MTJs [15]:

1. Voltage edge isolating read, write, and breakdown conditions shown in Fig. 5,
2. An adequateness of vitality obstruction for information maintenance,
3. TMR for an adequate amount of read flag,
4. Dependability since breakdown, and
5. MTJ being much more capable compared to CMOS transistor.

A 1T-1MTJ MRAM schematic diagram and its equivalent circuit are shown in Fig. 6 and write threshold offering about 300 mV is shown in Fig. 7.

At a compose batch rate of 10^{-9} , the compose voltage V_w is around two fold the edge voltage, and the dependence on V_w is relatively Gaussian. With extending compose heartbeat widths, the compose batch rate gets off faster and the edge voltage is cut down, as shown in Fig. 8.

The essentialness obstacle of the MTJ is 40 kBT. The assortment among $70 \times 210 \text{ nm}^2$ MTJs is Gaussian. For 100 ns compose, $\sigma(V_w) < V_w \geq 8.7\%$. In the midst of making, bothersome attractive reversal may happen close or over the compose limit. Such MTJs were recognized to be the ones that show low attractive security and can be discarded by changing cell structure. There are satisfactory edges between read and compose voltages.

The characteristic convergence breakdown voltage, V_{bd} , is evaluated to be more noticeable than 1.35 V, and shows an unforeseen I-V at V_{bd} . This is suggested as hard breakdown (hBD). Be that as it may, rare events of

Fig. 7 Write error rate versus write voltage V_w

deformation provoked delicate breakdown (sBD) are seen at voltages somewhat lower than hBD. Such sBD events will happen simply more as frequently as conceivable as the thickness of the section limit is diminished, a potential issue for future CMOS innovation hubs. Quantifiably, the Rp regards for MTJs with sBD and hBD are unclear. Be that as it may, after voltage extend, the Rp of hBD MTJs remains unaltered, in any case, Rp of sBD MTJs shifts toward cut down characteristics. MTJs proceed $> 7 \cdot 10^9$ compose cycles. There is sufficient edge between the VW and V_{bd} ,

Fig. 8 Write voltage against Write bit error rate of $8 \Omega\text{-}\mu\text{m}^2$ MTJs

Fig. 9 Memory cell-size in F^2 against write current

> 0.5 V. For future CMOS hubs, RA will scale back further, the control of sBD remains an innovation challenge [16].

3 Design of array of memory cells

As to likeness of these MTJs with CMOS design runs, a single piece line cell can be as meager as $\sim 9F^2$ in the 90-nm center point, if create current is under $50 \mu\text{A}$ [15] as shown in Fig. 9.

For the focused on MTJ working point at $\sim 4 \times 10^6 \text{ A/cm}^2$, the cell measure is $30F^2$. Bi-directional composes current amongst select line and bit line is sent into compose information as shown in Fig. 10.

When MTJs are composed from parallel to anti-parallel state, the access FET is bootstrapped [17, 18]. In order to the dispose of stray current that could influence read and compose activity, different Bit lines of the cluster are released before cell select line is activated [15]. Research are going on in the area to reduce the switching speed

Fig. 10 Description of bit line cells

[19], also implementing MRAM on SOI and DGSOI structures but have faced some failures [20, 21]

4 Results

Using the design flow in cadence virtuoso schematic tool, the MTJ one transistor and one MTJ element design was done. Also Flash and SRAM circuits were designed using cadence virtuoso schematic editor and finally the analysis was done in various aspects for all the designed circuits. The waveforms for bit line, word line and output for MTJ-MRAM, NOR-Flash and SRAM are shown in Figs. 11, 12 and 13. It is observed from the output waveforms that when word line (access transistor) is powered the output follows the data i.e. bit line for MTJ-MRAM and for NOR-Flash circuits showing Non-volatile feature. While when the access transistor is powered in SRAM, the output follows the data only when word line is high else when word line is low the output follows the previous output only.

The circuits are designed in 90 nm Technology and power and delay are estimated. For the designed MTJ-MRAM circuit on 90 nm and 45 nm Technology, the power and delay are estimated. The power consumption is found to be $\sim 19.97 \text{ nW}$ and Time Delay is found to be $\sim 15.14 \text{ fs}$ for 90 nm. While the power consumption is found to be $\sim 11.73 \text{ nW}$ and Time Delay is found to be $\sim 71.85 \text{ fs}$ for 45 nm. The power consumption, circuit delay time and its prominent feature in comparison with existing volatile and non-volatile memory circuits are recorded in Table 1.

From Fig. 13 it is observed that the data is stored only when wordline is high and when wordline is low the data is not stored in memory cell. This behavioral characteristic of SRAM makes it volatile and hence the data is not retained in SRAM on poweroff. Whereas the the behavioral characteristic of Flash memory shown in

Fig. 11 Behavioral characteristics of MTJ-MRAM

Fig. 12 Behavioral characteristics of nor flash

Fig. 13 Behavioral characteristics of SRAM

Table 1 Comparison of SRAM, FLASH and MRAM circuits

Memory	Delay (s)	Power (nW)	Feature
SRAM	64.11×10^{-9}	151.3	Volatile
NOR-Flash	4.568×10^{-12}	5.4	Non-volatile
MTJ-MRAM			
90 nm Technology	15.14×10^{-15}	19.97	Non-volatile
45 nm Technology	70.85×10^{-15}	11.73	Non-volatile

Fig. 12, which is present non volatile memory in market shows that data is retained even when word line is low. This characteristic of Flash memory makes it non volatile that stores data even when powered off. It is observed that in the designed resistive MTJ-MRAM memory cell, it offers a similar behavioral characteristics of that of Flash memory showing non-volatility. Also the attributes like power dissipation and delay are measured for designed

MRAM circuit and it is observed that MTJ-MRAM offers better performance than the Flash memory. A detailed comparison between different SRAM, NOR-Flash and MTJ-MRAM memories designed in 90 nm and 45 nm technology is shown in Table 1. The observation shows that MTJ-MRAM exhibits Non-Volatile feature offering good speed and low power consumption.

5 Conclusion

From the behavioral analysis of circuits and the timing analysis of the simulations carried out in the paper the following conclusions can be made.

1. An $8\ \Omega\text{-}\mu\text{m}^2$ MTJ demonstrates adequate R/W limits, warm steadiness, and compose continuance. With reiteration, as the channel shrinks, there is decrease in resistance area, delicate breakdown and compose current will require further change.
2. The VLSI design of MTJ-MRAM shows that there is a significant delay reduction of about 3 times i.e. the speed is increased by 3 times (both in 45 nm and 90 nm) compared to Flash Non-Volatile memory. The VLSI design of MTJ-MRAM of 45 nm shows power consumption is reduced to half of that required in 90 nm design.
3. The design of MTJ-MRAM also shows significant power and delay reduction of about 6 times compared to volatile SRAM circuit designed in 90 nm technology. The design of 45 nm MTJ-MRAM also shows a bottleneck of delay in the circuit which is increased ~ 55 fs compared to 90 nm design.
4. The design of MTJ-MRAM also offers Non-Volatility feature. By designing MTJ-MRAM in 90 nm technology for FPGA architecture, the configuration time of FPGA decreases and speed up overall FPGA process with added advantage of minimized power consumption compared to SRAM based FPGA.

Compliance with ethical standards

Conflict of interest The author declares that there is no conflict of interests regarding the publication of this paper.

References

1. Hamsa S, Ananth AG, Thangadurai N (2018) A study of semiconductor memory technology by comparing volatile and non-volatile memories. *J Adv Res Dyn Control Syst* 10(4):1252–1258
2. Islam A, Rajan NS, Dwivedi AK (2018) Compact design of an MTJ-based non-volatile CAM cell with read/write operations. *Microsyst Technol* 1:1–12
3. Worledge DC et al (2017) Theory of spin torque switching current for the double magnetic tunnel junction. *IEEE Magn Lett* 8:1
4. Huet G et al (2017) Low-current spin transfer torque MRAM. *Nat Nanotechnol* 10(3):187–191
5. Hu G et al (2015) MRAM with double magnetic tunnel junctions. In: *IEEE International Electron Devices Meeting*, pp 668–671
6. Peng S et al (2014) Magnetic tunnel junctions for spintronics: principles and applications. *J Wiley Encycl Electr Electron Eng* 1:1–16
7. Kim K, Yoo C (2016) Macro-model of magnetic tunnel junction for STT-MRAM including dynamic behavior. *J Semicond Technol Sci* 14(6):728–732
8. Chakraverty M et al (2013) First principle simulations of various magnetic tunnel junctions for applications in magnetoresistive random access memories. *IEEE Trans Nanotechnol* 12(6):971–977
9. Nowak JJ et al (2011) Demonstration of ultralow bit error rates for spin-torque magnetic random-access memory with perpendicular magnetic anisotropy. *IEEE Magn Lett* 2:3000204
10. Ikeda S et al (2010) A perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction. *Nat Mater* 9(9):721–724
11. Madec M, Kammerer J, Hébrard L (2008) Compact modeling of a magnetic tunnel junction Part II: tunneling current model. *IEEE Trans Electron Devices* 57(6):1416–1424
12. Chen Q et al (2008) Study of dielectric breakdown distributions in magnetic tunneling junction with MgO barrier. In: *Dig of MMM 2008*, DB-02
13. Min T et al (2008) Back-hopping after spin torque transfer induced magnetization switching in magnetic tunneling junction cells. In: *Dig of MMM*
14. Hosomi M (2005) A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram. In: *IEEE international electron devices meeting, IEDM technical digest*, pp 459–462
15. Kim H-J et al (2005) Development of magnetic tunnel junction for toggle MRAM. *IEEE Trans Magn* 41(10):2661–2663
16. Beach R (2008) A statistical study of magnetic tunnel junctions for high-density spin torque transfer-MRAM (STT-MRAM). In: *IEEE international electron devices meeting*
17. Mitchell BS et al (2004) An introduction to materials engineering and science: for chemical and materials engineers. Wiley, London
18. De Brosse J et al (2004) In: *Symposium on VLSI Circuits*, pp 454–457
19. Sverdlov V, Makarov A, Selberherr S (2018) Switching current reduction in advanced spin-orbit torque MRAM. In: *Joint international EUROSOL workshop and international conference on ultimate integration on silicon (EUROSOL-ULIS)*, Granada, pp 1–4
20. Cai H et al (2018) MRAM-on-FDSOI integration: a bit-cell perspective. In: *IEEE computer society annual symposium on VLSI (ISVLSI)*, Hong Kong, pp 263–268
21. Cai H et al (2018) Addressing failure and aging degradation in MRAM/MeRAM-on-FDSOI integration. *IEEE Trans Circuits Syst I Regul Pap* 66(1):239–250

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.