Research Article

Signal amplification with patterned conducting polymer electrodes based organic thin film transistor circuit

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Abstract

Organic thin film transistors (OTFTs) fabricated with non-destructive patterning techniques are the building blocks in realizing flexible electronic interface for sensing applications. In this study, a single stage differential amplifier is demonstrated with flexible OTFTs. The OTFTs were fabricated with thermally evaporated Pentacene as the semiconducting layer. The electrodes of the OTFTs were realized using a conductive polymer composite, poyaniline:polystyrene sulphonic acid (PANi-PSS), patterned by a modified Parylene lift-off process. Electrical characteristics of bottom contact TFTs with polymeric PANi-PSS electrodes is superior to those with conventional metal electrodes due to a lower charge injection barrier and resultant lower contact resistance. The measurement of the transistor characteristics and the amplifier response reported has been carried out with a wafer probing test jig set up. The differential amplifier realized with *p*-type Pentacene transistors with mobility, 0.5 cm^2/Vs, exhibited a voltage gain of 10 dB in a frequency bandwidth of 1 kHz.

Keywords Amplifier · Patterning · Conducting polymer · Organic thin film transistor · Parylene lift-off · Wafer probing test jig

1 Introduction

Over the last decade, the field of organic electronics has grown from discrete single unit fabrication to circuit level integration, due to the development of high–performance organic semiconductors (OSCs), large scale fabrication techniques and understanding of operation mechanism [1]. Complementary circuits, wireless systems, memory and processing units were successfully demonstrated, leading to their potential implementation in different kind of sensors [2, 3]. OTFTs are the primary building blocks of numerous devices such as low-cost radio-frequency identification tags [4], flexible displays [5, 6], wearable sensors [7–9], medical devices [10], digital and analog circuits [11, 12]. Sensing and signal processing of various signals using conformable flexible organic integrated circuits have been actively researched to enable real time sensing on curvilinear surfaces [13, 14]. In the analog regime,

from a fundamental viewpoint, signal amplification is the simplest form of signal processing. Organic amplifiers find application in devices which need monolithic integration of any flexible sensor and the amplifying circuit. OTFTs being the functional units of organic amplifiers, their performance have to be optimized with respect to the materials employed such as the OSCs, insulators, conducting and passivating materials. Within this scope, ultrathin flexible organic amplifier is the most important building block for large-area signal recording and stabilization in close proximity to the site of interest.

Organic amplifiers have been developed in different layouts on flexible substrates to achieve good frequency response and high gain. To harvest the response of certain materials to pressure/force/strain or temperature stimuli, the sensors often are coupled to thin film transistors (TFTs) that convert the response generated by the material to an amplified voltage signal, suitable for

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subsequent interfacing with readout electronics [15–19]. Due to the limitations of the inherent mobility of organic semiconductors, the achievable gain and gain bandwidth are comparatively lower than the inorganic counterparts. Many amplifier topologies, from simple buffers to more complex differential amplifiers have been shown using unipolar p-channel OTFTs [20–22]. Marien et al. demonstrated differential amplifier with Pentacene based transistors, optimizing basic differential pairs by following four different techniques. Their circuit showed a gain of 18 dB. It was demonstrated that Pentacene based analog circuits could deliver satisfactory and acceptable performance, even after repeated use for four months and different applied stress conditions [23]. Recently, Reuveny et al. demonstrated organic amplifiers based on small organic semiconductor, dinaphtho [2,3-b:2',3'-f] thieno [3,2-b] thiophene (DNTT). They achieved voltage amplification of 13 dB with cut-off frequency 2.5 kHz. A high uniformity in the gain, among six amplifier circuits, 13.0 ± 1.2 dB over 4×4 cm^2 was also demonstrated. The open loop design gave gain bandwidth product of 45 kHz with operating voltage of 7 V [22]. The highest open-loop gain and the highest gain-bandwidth, reported with organic amplifiers is 36 dB [24] and 18 kHz [25], respectively, which are but, adequate for application that do not demand very high speed and very high frequencies.

For real time sensing on curvilinear surfaces, the amplifier circuit has to be integrated in close proximity to the sensor and should also be flexible. For such applications, the basic building blocks of the amplifier, the flexible OTFTs should have all the layers, including the dielectric and conducting, preferably fabricated out of organic materials. This study was undertaken to fabricate an all organic flexible OTFT, as it is the prerequisite for the realization of a high performance flexible amplifier. There are not many literature available for flexible amplifier realized from OTFTs, in which patterned conducting polymer electrodes have been employed. Conducting polymer electrodes have shown to have lower charge injection barrier and hence lower contact resistance than metal electrodes, in OTFTs [26, 27]. The present study aims at fabrication of flexible OTFT based single stage amplifier that can amplify differential input signals on any curved surface. The electrodes of the transistors are fabricated from solution processable, conductive polymer composite, poyaniline:polystyrene sulphonic acid (PANi-PSS), that are patterned by a modified Parylene lift-off process. The conducting polymer electrode ensured lower charge injection barrier in the OTFTs [28] and hence better performance of the flexible amplifier.

For fabrication of such a flexible amplifier that can be an integral part of an acoustic sensing system, optimized materials and processes have been utilized that yielded optimum performance for the OTFTs. An effective passivation of OTFTs with a compatible material such as Parylene C ensured consistent and reliable performance of the flexible amplifier. A flexible amplifier fabricated with all organic materials, demonstrated in this study, can be integrated in close proximity to the output signal from any sensor. The proximity between sensor and electronics minimizes signal loss by avoiding large lengths of cable used for signal transfer. The signal amplification of acoustic signal from a polymeric piezoelectric sensor was also demonstrated in this study. Additional circuit techniques such as cascading and gain boosting can be applied to further maximize the gain.

2 Experimental details

2.1 Thin film transistor fabrication

A clean silicon wafer was laminated with polyethylene naphthalate (PEN) film. Prior to device processing, the PEN was preshrunk at 165 °C in an oven to improve its dimensional stability. The mask design with 37 numbers of TFT was designed so as to realize devices with different aspect ratio, to be suitably employed as load or input devices in the amplifier (Fig. 1a). To define the gate, a 70 nm thick palladium metal layer was defined using photolithography and lift-off process. For the gate dielectric layer, poly(4-vinyl phenol) (PVP) solution was prepared by dissolving PVP (12 wt% of solvent) and methylated poly (melamine-co-formaldehyde) (3 wt% of solvent) as cross-linking agent in propylene glycol methyl ether acetate solvent. The spin coated PVP insulator layer was patterned using photolithography and O$_2$ plasma etching. A modified Parylene lift-off method was then adopted for patterning the solution processable electrodes of PANi-PSS as previously reported by our group in [29].

The length of all the devices was 5 μm and widths of 1700, 1000 and 300 μm were used. For comparing the results of the conducting polymer electrode based OTFT with conventional OTFT, devices with Pd source and drain electrode were also fabricated and patterned by lift-off process. Parylene C was employed for simultaneous passivation and patterning of Pentacene [30], as previously reported by our group. The schematic of the fabricated OTFT for studies on effect of electrodes is shown in Fig. 1b. The yield of the devices fabricated was ~85%, with almost equal number of TFTs with different aspect ratio. For the convenience of testing, the support wafer beneath the flexible substrate was removed only after the characterization of all the devices and the amplifier circuit.

Fig. 1 a Mask design of OTFTs employed as load or input devices in the amplifier and **b** Schematic of the fabricated OTFT
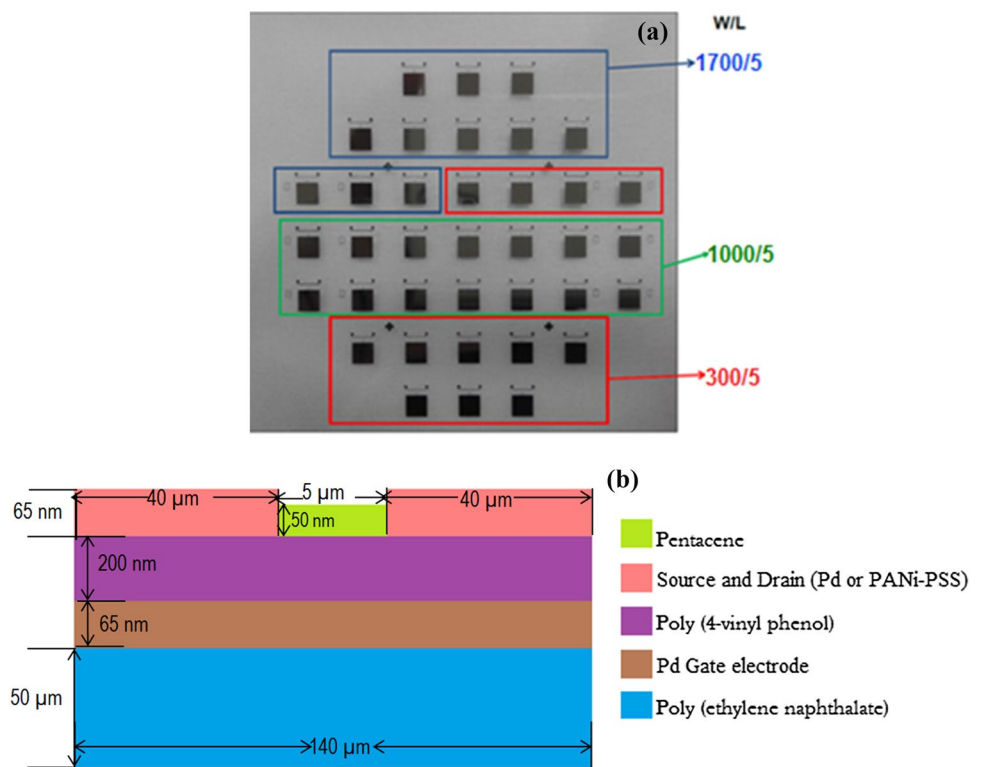
2.2 Design and fabrication of wafer probing test jig for testing of OTFT amplifier

The wafer probing test jig was designed and fabricated to meet two main objectives. First was to probe all 37 device terminals simultaneously on the 3" substrate (PEN film supported on wafer). Second objective was to test the devices in an amplifier configuration by connecting the TFTs to a matrix of configurable jumpers. The batch fabrication of OTFT was done on a 3" flexible substrate as described in Sect. 2.1. The design consisted of 37 number of OTFT (different W/L ratio) with the source, drain and gate of the devices connected to metal contact pad of dimension 500×500 μm. To avoid the complications involved in taking connections from each contact pad, the wafer probing test jig was in-house designed and fabricated for the purpose of testing the devices and configuring them as amplifier. The wafer probing assembly could probe the 500×500 μm metal pad terminals of all the devices on a wafer and connect to configurable matrix of switchable jumpers. The jig could work with maximum of 100 V DC voltage, hence the components used in this test jig had sufficient voltage rating. It was designed to have scalability to accommodate different aspect ratios for different devices, in a totally independent manner by shunting multiple devices together.

The performance of the amplifier topology could be checked for multiple wafers by just inserting the wafer on

the jig. To account for a low noise amplifier design realization on the test jig, shielded BNC connectors (Keithley) were used for feeding the input signal to the input devices of amplifier. Similarly the output of the amplifier was also routed though BNC connectors. Shielded coaxial cables were provided for monitoring the signal. A guide card with through holes was fabricated as per the mask design of contact pads and lay out of OTFTs, which could guide all the probe pins of test jig to correctly align and connect to the metal pads on the substrate. Pins used in the jig were special type of spring loaded POGO pins. The electrical connections were not permanent, but could be replaced with ease. Five stages of amplifier design were also included in the jig for application in future, with each single stage utilizing five TFTs. Through the matrix of configurable jumpers, each TFT could be connected in place of any other TFT location in any amplifier stage. The fabricated wafer probing test jig is shown in Fig. 2.

A very straight forward design of a single stage differential amplifier was adopted for testing the achievable gain with the fabricated TFT based amplifier. The gate terminal of the load of p-type OTFT was connected to the drain terminal. This resulted in a diode load with the load OTFT biased in saturation region. For higher bandwidth (BW), the diode-connected load performs better and is relatively less sensitive to shift in threshold voltage (V_T) over time. The schematic of the design of single stage differential amplifier used in the study is shown in Fig. 3.

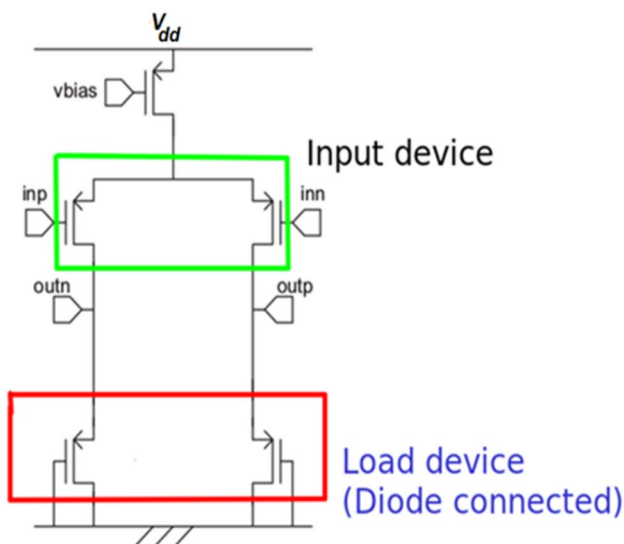**Fig. 2** Photograph of the wafer probing test jig

Fig. 3 Schematic of the design of single stage differential amplifier used in the study

In amplifier with diode connected loads, the voltage gain is represented by Eq. (1) [31].

$$\text{Voltage gain} = g_{mI}/\left\{g_{mL} + g_{dsI} + g_{dsL}\right\} \quad (1)$$

where, g_m is the transconductance and g_{ds} is the conductance parameter, defined by Eqs. (2) and (3).

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (2)$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \quad (3)$$

the suffix 'I' and 'L', represent the input and load, respectively.

The transconductance, g_m is proportional to mobility (μ) and V_T of the transistors. For the voltage gain to have less dependence on μ and V_T, the g_m factor of the devices should be much larger than the g_{ds}. In such cases, voltage gain being a ratio of two g_m factors, will be a weak function of μ and V_T of the TFTs. The voltage gain then simply will be the ratio of transconductance of input pair of transistors and that of the transistors acting as load devices.

2.3 Testing of TFTs on test jig

2.3.1 Placement and alignment of TFTs on test jig

For positioning the wafer with fabricated 37 devices on the test jig, the split microscope and micropositioners of mask aligner (ABM 6, USA) stage was utilized. The contact pads on the wafer were aligned with the guide card with through-holes (designed as per the TFT layout in the wafer). The wafer was temporarily stuck with a double side tape to the guide card after alignment. The wafer along with guide card was then placed over the test jig with POGO pins touching the contact pads of the wafer through the through-holes. The photographs of the process of aligning the TFT contact pads with the holes on the guide card using the mask aligner is shown in Fig. 4a–c. Figure 4a shows the wafer and guide card mounted on the wafer stage and mask stage, respectively. Figure 4b shows the process of alignment with the split microscope and Fig. 4c is the electrode pads aligned with the holes on the guide card, as seen by the split microscope. After the alignment, the wafer along with guide card was mounted on the wafer probing test jig for the electrical characterization. The schematic of side and top view of the wafer aligned on test jig is shown in Fig. 5a, b.

2.3.2 Connectivity test for wafer probing test jig

The test is aimed to ensure that all the probe pins make electrical contact with the pad locations on the TFTs (gate, source and drain terminals). For this purpose, only the contact pads of the TFTs were fabricated on a dummy wafer, with positions exactly similar to the pad terminals of OTFTs. All the three pads of each structure were shorted during fabrication. Test was aimed at feeding a voltage to gate terminal with respect to the ground. Since the drain and source pad terminals were shorted to gate pad, voltage would be available at the source
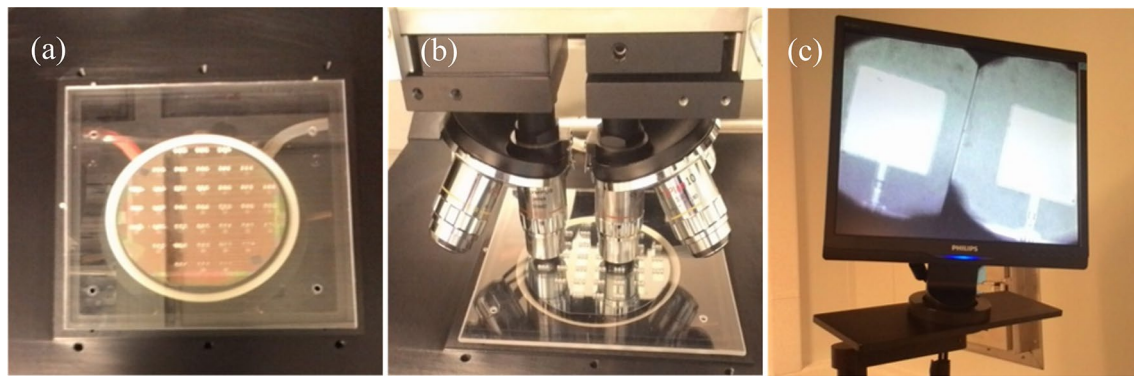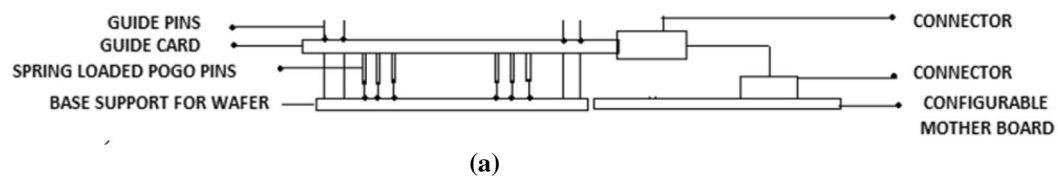
Fig. 4 Photographs of the process of aligning the TFT contact pads with the holes on the guide card using the mask aligner **a** wafer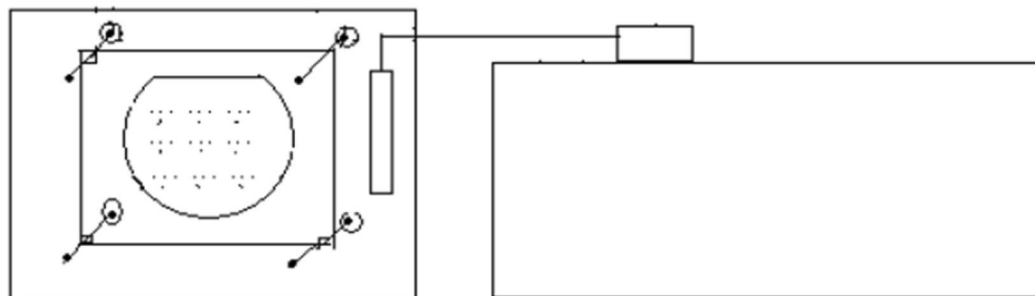 and guide card mounted on the wafer stage and mask stage, respectively, **b** process of alignment with the split microscope and **c** electrode pads aligned with the holes on the guide card, as seen by the split microscope

Fig. 5 Schematic of side and top view of the test wafer aligned on test jig

and drain terminals also, which could be confirmed by the glowing of a LED connected to the source and drain. For the purpose of testing, all the gate terminals of 37 devices were shorted to a common point. A voltage of − 5 V was applied to the common terminal. Since the source and drain terminals were shorted with the gate and connected to LEDs, on probing all the terminals with the test jig, all the 37 LEDs were glowing. The test proved that all the 37 contact pads were probed with the test jig. The test is important to confirm the availability and probing of all 37 devices with the test jig, during the process of configuring the amplifier. The schematic of the connectivity test with the test jig is shown in Fig. 6a and

the corresponding photograph of the testing is shown in Fig. 6b. An Elnova Model E-DC power supply was used to give the voltage and Keysight 34450A digital multimeter was used to measure the voltages.

2.3.3 Testing of OTFTs as switches

For simultaneously checking the 'on' condition of all the 37 TFTs fabricated on the 3″ substrate, all the gate terminals of devices were connected to a single pin, V_{gconn}. Jumper positions were as shown by coloured locations in Fig. 7. V_{dd} of 5 V was applied, with V_{gs} sufficiently low than V_T, enabling the devices to turn on. Since, for each TFT there
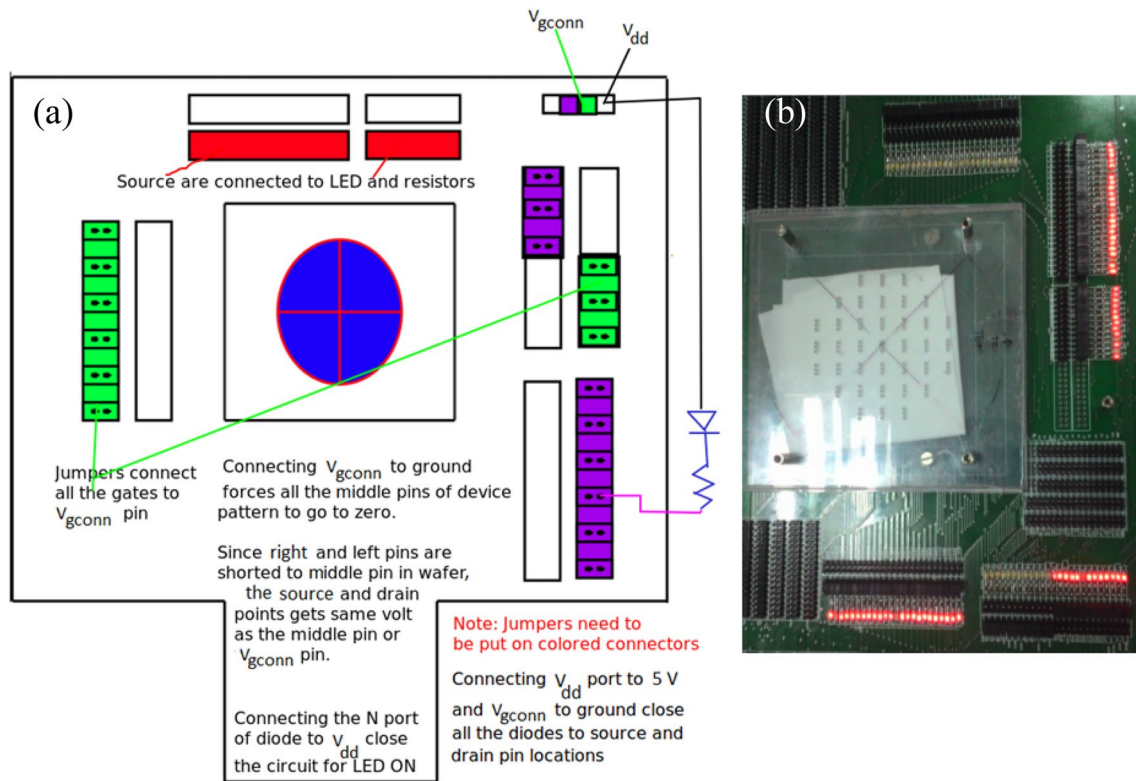
Fig. 6 **a** Schematic representing the connectivity test with the wafer probing test jig for the 37 devices in a 3" substrate and **b** photograph showing the devices tested for connectivity on the wafer probing test jig, indicated by the glowing of LED for the properly connected OTFTs
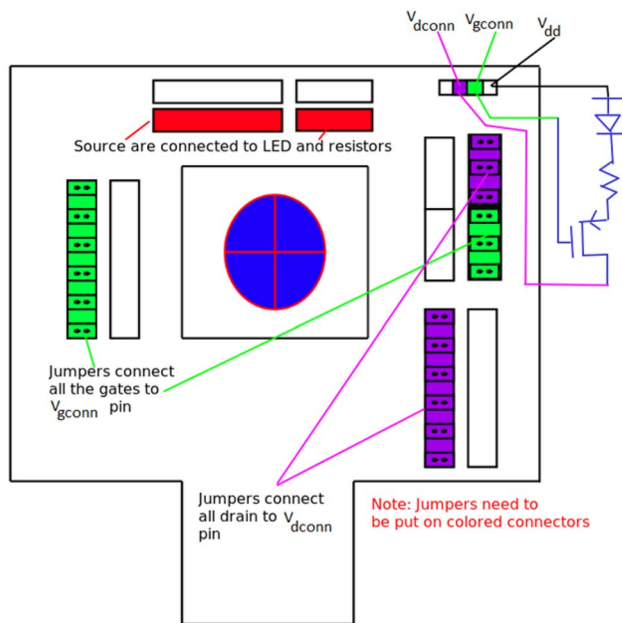

Fig. 7 Schematic representing the testing of 37 OTFTs in a 3" substrate as switches, with the wafer probing test jig

is a separate diode string, all the 37 TFTs turn on, which is indicated by the glowing of LEDs. For the testing of the 'off' condition of the TFTs, $V_{gs} > 0\,V$ was applied, the condition in which all the devices are expected to be 'off'. In the test on different sample wafers, an average of 3 devices did not turn off, indicating a low I_{on}/I_{off} ratio. Such TFTs were marked and not used for configuring the amplifier.

2.4 Configuring and testing of TFTs as amplifier for acoustic sensor

To determine the achievable gain and bandwidth with the organic transistor based amplifier circuit, simulated signal from a function generator was used. AC signal was generated using Tektronix AFG 3102 dual channel function generator. The output was recorded using Tektronix TPS 2024 four channel digital storage oscilloscope (DSO). The gate electrodes of the TFTs were protected with transorbs externally, to avoid damage to the circuit due to voltage spike from any other source. Connections were established using the wafer probing test jig as per the schematic shown in Fig. 3. Negative input terminal of the amplifier was set to a DC voltage bias. A sinusoid signal of programmable amplitude was added to the DC voltage and given to the positive input terminal. Being a
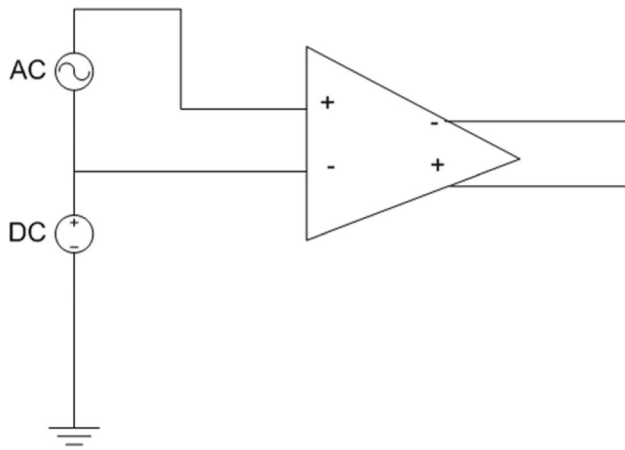
Fig. 8 The schematic for testing the amplifier configured using OTFTs on 3" wafer, mounted on the wafer probing test jig

differential amplifier, the sinusoid signal only got amplified and the constant DC voltage bias was discarded by virtue of common mode rejection. Few input transistors were connected in parallel to emulate the effect of multiple fingers. Various load configurations for gain enhancement were also implemented through the jig to achieve the required gain. The schematic of circuit for testing the amplifier is shown in Fig. 8. The amplifier was characterized

for different input voltages. Five numbers of single stage amplifiers were tested and checked for the voltage gain. The experimental set up used for measuring the amplification of the signal using OTFT based differential amplifier is shown in Fig. 9. The amplification of the signal was tested from 100 to 2 kHz.

The amplification of the acoustic signal was tested with a 10 cm × 10 cm electroded piezoelectric sensor. The schematic of the test set up is shown in Fig. 10a. A tone burst was fed to a projector (speaker) through an audio power amplifier. The sensor placed in front of the projector senses the acoustic signal. The schematic of circuit representing the amplification of signal from the acoustic sensor is shown in Fig. 10b. The top plate of sensor electrode was connected to a constant DC bias voltage. A resistor of 100 kohm was connected across the electrodes of sensor. The charge in the piezoelectric sensor, upon receiving the acoustic signal varies and flows through the resistor and created a voltage. This voltage is the equivalent of the sensor generated voltage. The bottom plate of the piezoelectric sensor would be at a voltage equal to fixed DC bias ± the sensor generated voltage. The amplifier amplified the difference in voltage between the input terminals (fixed DC bias being common in both the nodes, gets cancelled) and only the voltage generated by the sensor is amplified. The output voltage from the sensor and the
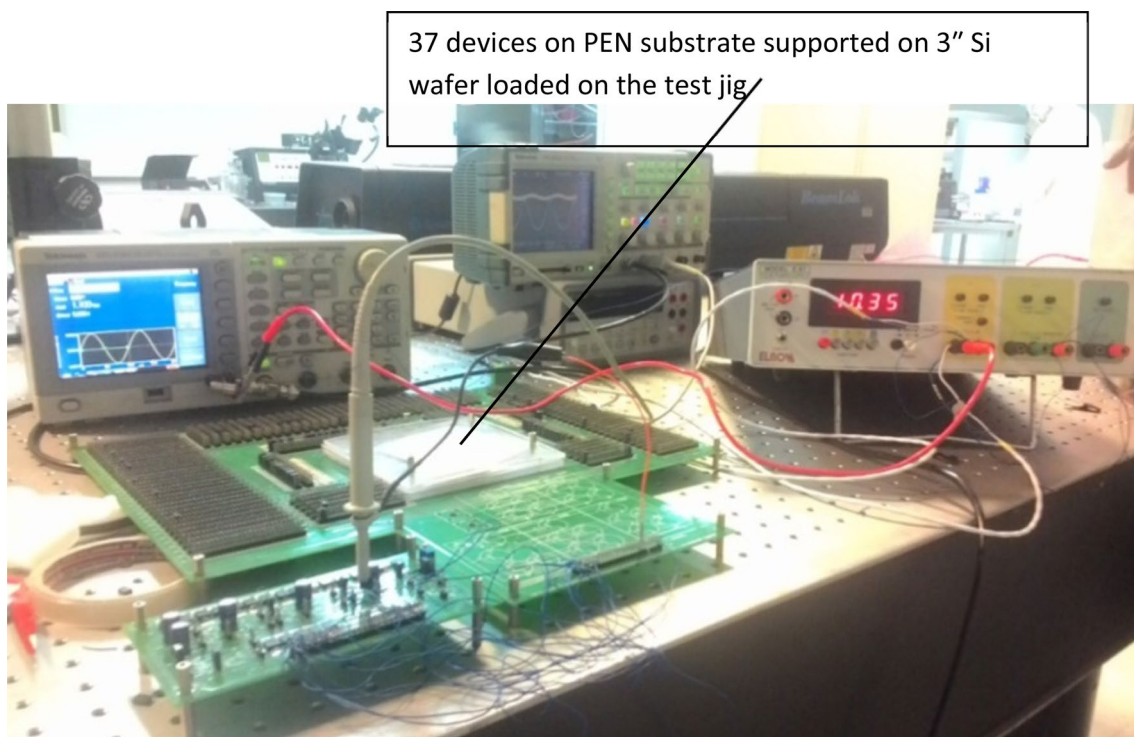

37 devices on PEN substrate supported on 3" Si wafer loaded on the test jig

Fig. 9 Experimental set up used for measuring the amplification of the signal using OTFT based differential amplifier
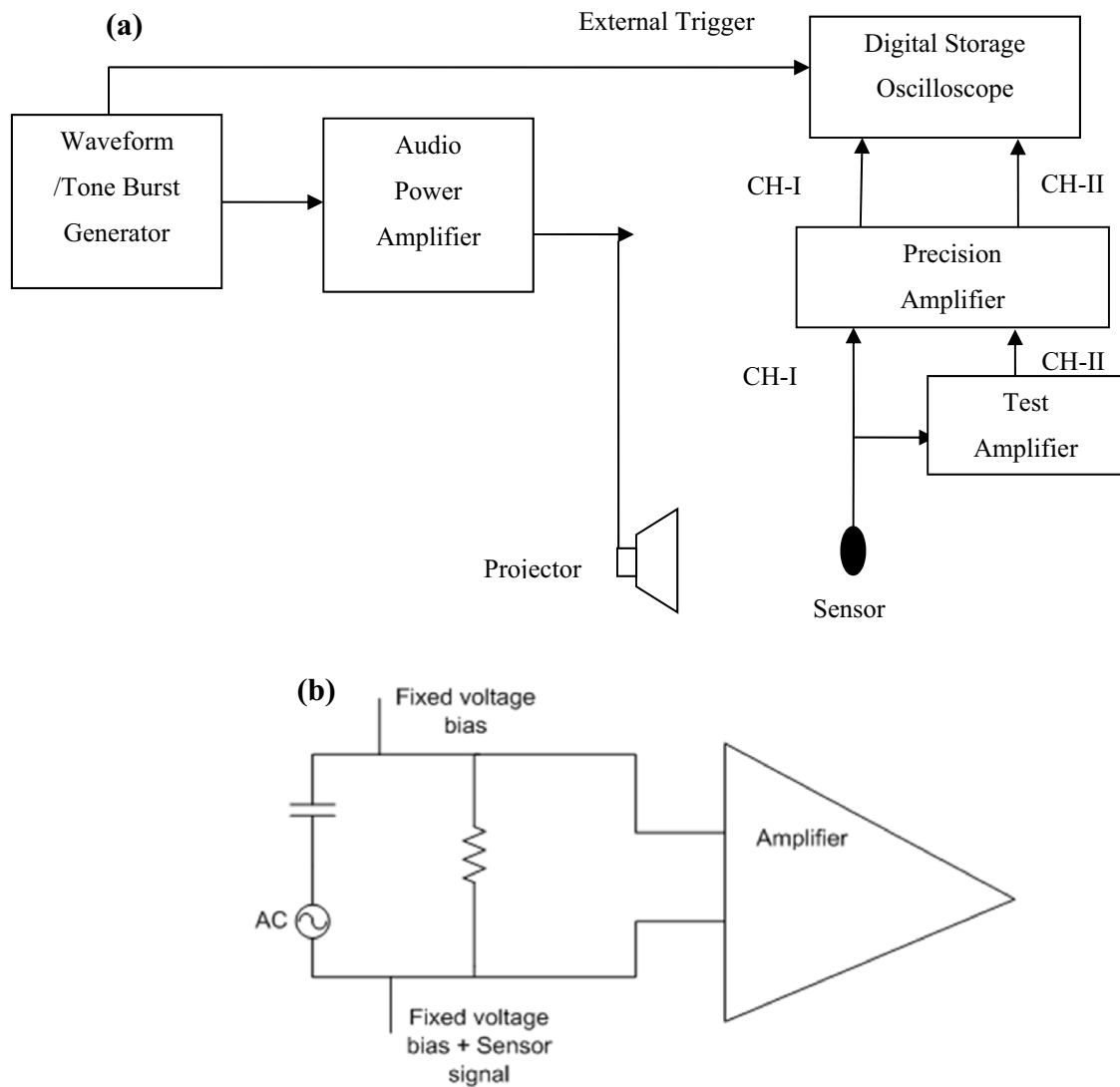
Fig. 10 Schematic of **a** the test set up used for the testing of amplification of acoustic signal generated from a piezoelectric sensor and **b** circuit representing the amplification of signal from the acoustic sensor

voltage amplified by the OTFT based test amplifier were received at two different channels of the digital storage oscilloscope, through a precision conditioning amplifier (Fig. 10a). The ratio of the voltage at channel-II to voltage at channel-I gave the gain of the OTFT amplifier.

3 Discussion on the results

3.1 OTFT characteristics

The OTFTs fabricated for realizing the flexible amplifiers in this study were passivated with Parylene C. The process

of passivation also simultaneously patterned the semi-conductor layer, which reduced the leakage current and increased the I_{on}/I_{off} ratio. The results of effect of passivation have been discussed in detail in [30]. The mobility of the Pentacene OTFT passivated with Parylene C remained constant during the period of study of four months. The mobility values were not affected even after six months. The electrical characteristics of unpassivated and unpatterned TFT were beyond the measurable ranges even after 60 days. However, the pin hole free photolithographically patterned and Parylene C passivated Pentacene TFT is quite stable and does not affect the characteristics of the
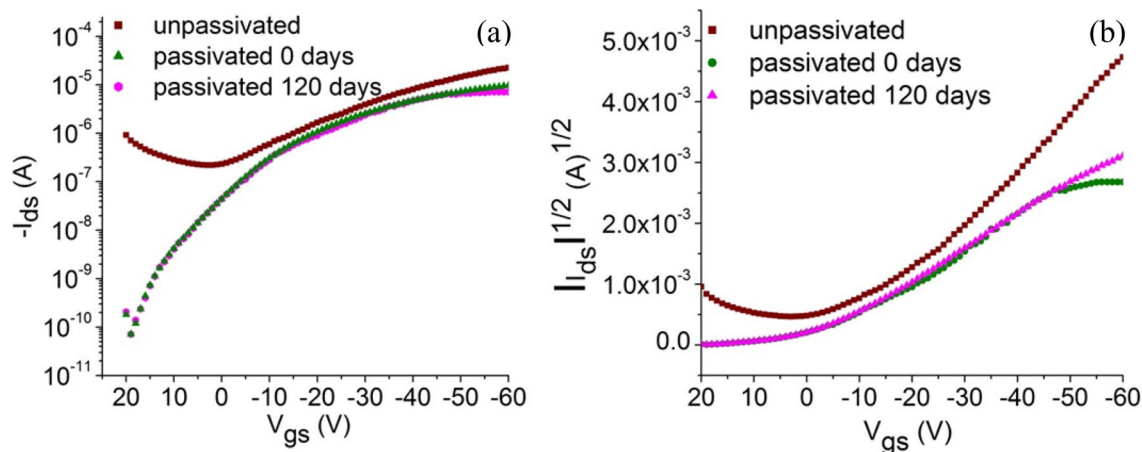
Fig. 11 Time dependent **a** I_{ds}–V_{gs} transfer and **b** $|I_{ds}|^{1/2}$–V_{gs} curves of bottom contact, unpassivated and Parylene passivated OTFT (20 μm channel length) in ambient air
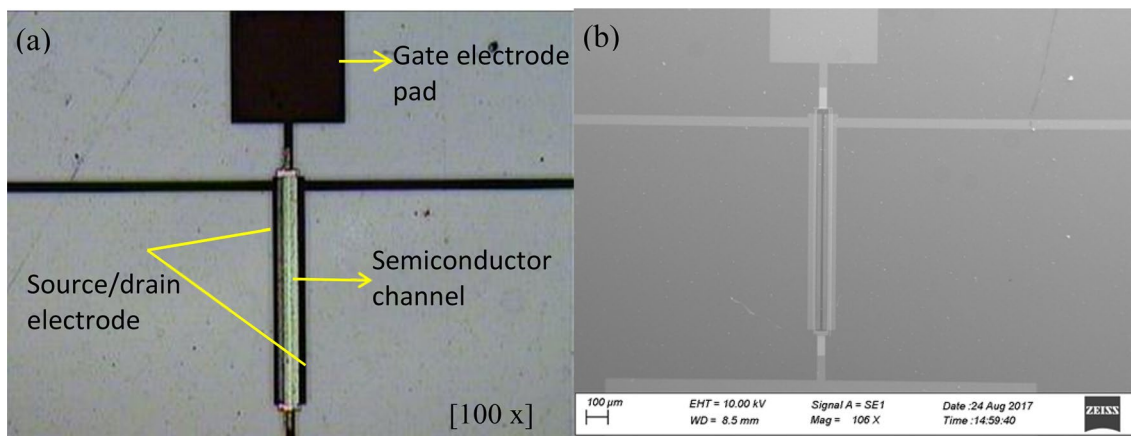

Fig. 12 **a** Microscopic image and **b** SEM image of fabricated Pentacene OTFT with PANi-PSS electrode
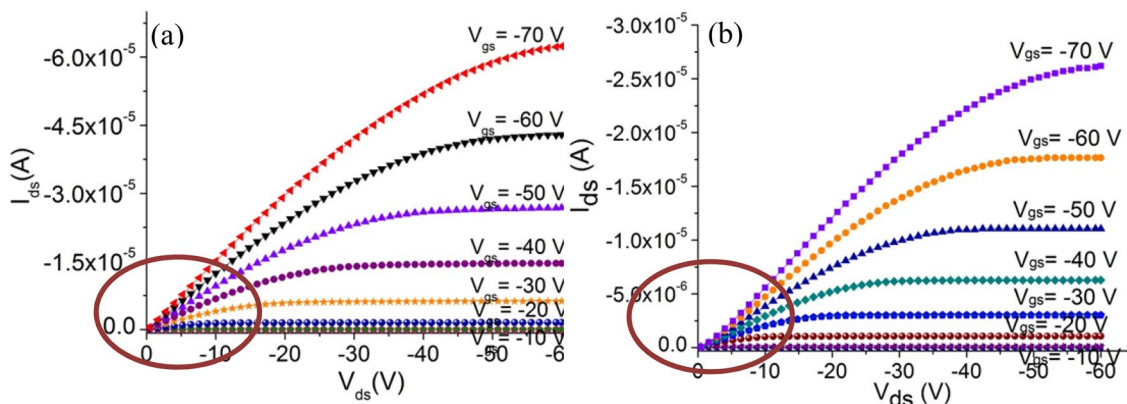

Fig. 13 I_{ds}–V_{ds} characteristics of OTFT fabricated with **a** PANi-PSS as source and drain electrode, **b** Pd as source and drain electrode
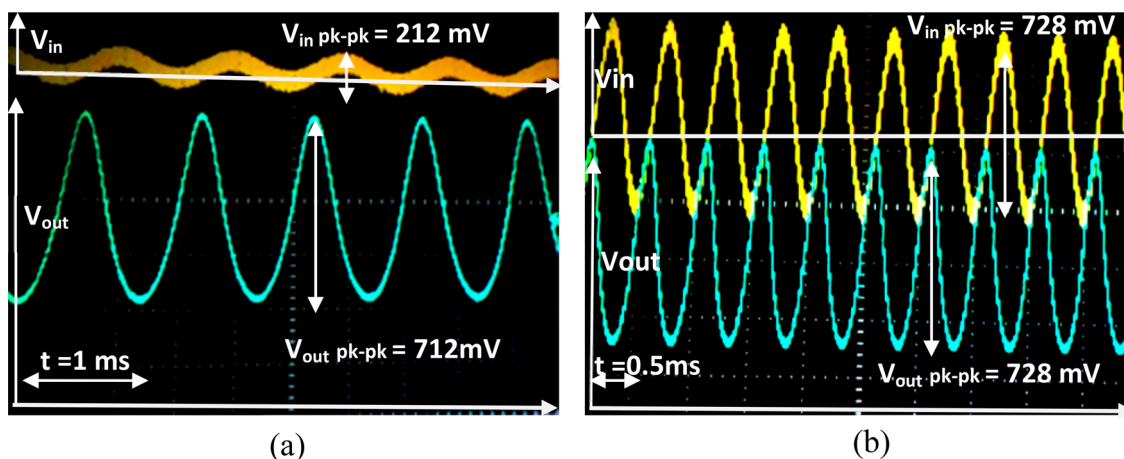
Fig. 14 Photograph of the input and output signals, observed on a DSO, revealing the amplification of signal at **a** 1 kHz and **b** 2 kHz (V_{in} and V_{out} represent the input and output voltage, respectively)

OTFT with time. The transfer characteristics of unpatterned and Parylene C passivated OTFT are shown in Fig. 11a, b.

The microscopic image and the Scanning Electron Microscopy (SEM) image of a discrete OTFT with PANi-PSS patterned by Parylene lift-off method, as source and drain electrode are shown in Fig. 12a, b, respectively. The devices exhibited lower charge injection barrier when compared to the ones with metal, Pd electrode. The I_{ds}–V_{ds} characteristics of the OTFTs fabricated with PANi-PSS and Pd electrode as the source and drain electrodes are shown in Fig. 13a, b, respectively. The non-linearity usually observed with metal electrodes, such as palladium and nickel [32, 33] in the I_{ds}–V_{ds} characteristics, at lower V_{ds} (circled portion in Fig. 13a) values is nearly absent in Fig. 13a. The non-linearity is a direct consequence of the higher contact resistance due to metal electrodes used in OTFTs. The non-linearity at low V_{ds} values in OTFT with Pd electrode is evident in Fig. 13b. The results are also discussed in detail in [29]. The conducting polymer electrode, PANi-PSS, with lower charge injection barrier, due to lower contact resistance and an effective passivation with Parylene C, aided in the realization of amplifier circuit with these OTFTs.

3.2 Amplifier characteristics

In this study an in–house designed wafer probing test jig was employed to select the required OTFTs from a group of 37 discrete transistors and connect them to form a single stage differential amplifier. The connection between the test jig and the OTFT was established using POGO pins provided on the jig. Screening of the OTFTs as switch and for their functioning at the start of the experiment, enabled to discard the devices that were non-functional or had low I_{on}/I_{off} ratio. Such devices were not included in

the amplifier circuit. As independent jumpers were provided on the test jig to connect to any of the OTFTs on the 3" wafer, they could be selected irrespective of their position on the wafer. The conventional method of taking connections from such circuits is through wire bonding. Wire bonding is a permanent process and hence, there is no possibility of discarding any non–functional TFT from a circuit. In such cases, due to the improper functioning of any one device, a whole set of 5 or more OTFTs, configured as an amplifier, would have to be discarded.

Measuring the circuit characteristics using a test jig is easier when a new set of materials have to be proven for their utility in analog or digital circuits. Establishing electrical connection through manual wire bonding is tedious and also a time consuming process. Noise characteristics of the circuit will essentially be higher when using a test jig, as the connections are established externally and the discrete OTFTs are placed far apart (≈ 1 cm) on the wafer. But, after proving the feasibility of realizing functional circuits, complete design can be made on wafer itself with connections established by wire bonding, thus minimizing the noise levels, improving the amplifier gain and bandwidth.

The photographs of real time measurement of amplification of signal by the OTFT amplifier, recorded with a DSO, at 1 kHz and 2 kHz are shown in Fig. 14a, b, respectively. The X-axis and Y-axis represent time and amplitude of voltage, respectively. The single stage amplifier realized with the organic TFTs exhibited a constant gain of 10 dB up to 1 kHz, which is the frequency band of interest for large area flexible acoustic sensors. The cut off frequency (f_c) was 1.2 kHz, where the gain dropped by 30%. Bode plot representing the voltage gain of the amplifier as a function of frequency is shown in Fig. 15. Similar output was observed
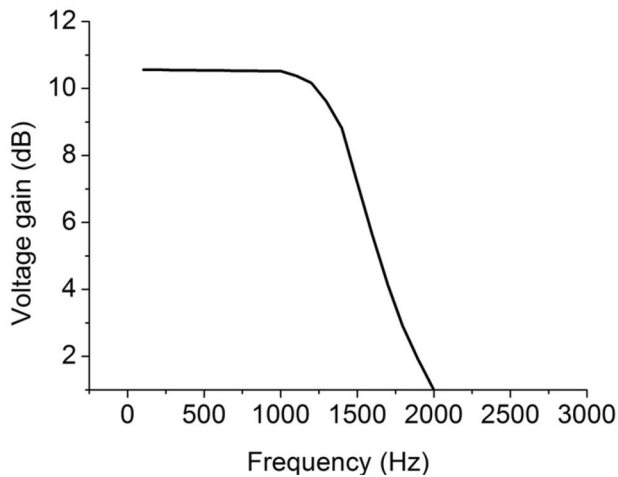
Fig. 15 Bode plot showing the voltage gain of the flexible OTFT amplifier as a function of frequency

on feeding differential input from a piezoelectric sensor to the organic TFT based front end electronics. A flexible amplifier realized on PEN substrate, consisting of OTFTs with solution processable conducting polymer electrode, patterned by the novel Parylene lift-off method is reported for the first time. The OTFTs configured as the amplifier showed good repeatability and gave reproducible results during the period of study of 4 months, under various bias conditions. This could be achieved only due to the effective passivation with photopatterned Parylene C.

For the flexible amplifier, single stage voltage gain of 10 dB and frequency bandwidth of 1 kHz has been achieved as a result of employing conducting polymer electrode, PANi-PSS with lower contact resistance and an effective passivation technique with photopatterned Parylene C. PANi-PSS electrode aided in reducing the charge injection barrier in TFTs and Parylene passivation protected the active semiconductor layer, Pentacene from degrading and in giving a consistent amplifier response. The frequency response and the voltage gain of the amplifier remained almost constant for a period of four months, the period for which the response was monitored. The conventional OTFTs, with metal electrodes have also been tested for the amplifier response, the gain of which was found to be 6 dB in a frequency bandwidth of 800 Hz. The biasing circuit and interconnections have been realized in the present study with the help of an external jig. The observed voltage gain is comparatively lower than that reported with novel semiconducting materials. However, the gain and bandwidth can further be increased by miniaturizing the circuit design at wafer level, fabricating the interconnections on the wafer and applying additional circuit techniques such as cascading the transistors. Reducing the size of the crossing lines thereby decreasing the

parasitic capacitances and noise within the circuit can also improve the achievable single stage gain. By applying techniques to reduce the overlap capacitances between gate and drain & gate and source, the frequency response of the amplifier can be improved. The amplifiers optimized for high gain and minimum chip area are important step towards the realization of flexible electronic systems. Sensor signal amplification and analog-to-digital conversion on a flexible substrate, coupled to a flexible sensor such as acoustic sensor is highly essential for flexible electronic applications. Fabrication of flexible acoustic sensor in close proximity to the amplification circuit, enabling monolithic integration can reduce parasitics to a great extent for large area flexible sensors.

4 Conclusions

The method adopted for configuring the discrete TFTs fabricated on a 3″ flexible substrate as a single stage differential amplifier has been discussed. Feasibility of real time sensing of acoustic signal generated by a standard piezoelectric sensor was tested with a fabricated single stage flexible differential amplifier. The flexible amplifier consisting of OTFTs with solution processable conducting polymer electrode, patterned by the novel Parylene lift-off method exhibited a gain of 10 dB in a frequency bandwidth of 1 kHz. It is proposed that the gain can be further increased by miniaturizing the circuit design at wafer level and applying additional circuit techniques, including cascading the transistors.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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