Reliability experimentation of 1200 V SiC power *n*-MOSFETs by accelerated thermal aging and bias temperature instability

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Abstract

This paper describes reliability experiments on 1200 V SiC power *n*-MOSFETs manufactured by three different manufacturers utilizing two different mechanisms: accelerated thermal aging and bias temperature instability. Each of the devices was electrically tested for evaluating variation of pre- and post-stress I–V characteristics. Pre-stress evaluation of threshold voltage (V_{th}) for 25 cycles showed transient behavior and a saturation toward an average value. For thermal aging reliability test, devices were stressed at 120 °C for 200 h and 3.33% of the devices showed significant shift in threshold voltage (V_{th}). For bias temperature instability measurement, devices were stressed at 120 °C for 200 h and a bias voltage of 20 V was applied across the gate–source terminals. For 96.7% device, V_{th} demonstrated an increment with stressing time and a movement toward saturation.

Keywords Power MOSFETs · Reliability study · SiC power *n*-MOSFET · Bias temperature instability testing

1 Introduction

Wide bandgap (WBG) power switching devices promise significantly more efficient operation of power electronic switching converters at higher junction temperatures and at higher switching frequencies compared to silicon power devices [1]. Among the available commercial WBG power devices in the market today, SiC power MOSFETs rated at 1200 V have been used for applications in motor drives, electric vehicles and power supplies as a replacement for silicon power MOSFETs and silicon IGBTs. However, SiC power MOSFETs have reliability issues due to excessive gate oxide, interface state charge and residual defects in the epitaxial region [2]. For instance, gate MOS threshold voltage shifts ($\Delta V_{GS(th)}$) due to DC positive (+ 15 V, + 20 V) and DC negative gate bias (– 10 V, – 15 V) at 150 °C are well-known [3].

In recent reliability study on 1200 V SiC-MOSFETs, weaker short-circuit capabilities compared to Si IGBT power devices, and two most prevalent failure mechanisms caused by gate oxide breakdown and thermal

runaway [4] were mentioned. Murakami et al. showed a positive shift in threshold voltage for SiC-MOSFETs during positive bias temperature instability test [5]. Hu et al. demonstrated that non-uniformities in the electrothermal characteristics of parallelly connected 1200 V SiC-MOSFETs reduce overall reliability compared to discrete device since power is not equally dissipated between the devices [6]. Liu et al. performed a systemic reliability study of bias temperature instability on 1200 V SiC-MOSFETs and observed a saturation of threshold voltage with the stressing time [7].

In this work, we have presented the reliability study of 1200 V SiC power MOSFETs from three different manufacturers. Accelerated thermal aging and bias temperature instability procedures were utilized to perform the reliability study. A measurement setup was developed to test multiple power devices by accelerated bias temperature instability testing method. The gradual degradation of static properties [e.g., threshold voltage (V_{th})] due to bias temperature instability testing was also measured. A total number of 60 devices were tested, and statistical data

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analysis was used to estimate the trends and spreads in key device parameters such as V_{th} .

2 Experimental details

In this study, a total number of 60 devices were tested from three different manufacturers (termed as A, B and C). The device specifications are summarized in Table 1.

The reliability study of the power devices that were performed here could be divided into two main categories:

1. Accelerated life test by temperature acceleration.
2. Bias temperature instability test.

Before and after stressing the devices, the devices were tested to measure static electrical characteristics using Agilent 1505A power semiconductor parameter analyzer. In this test, the gate–source voltage, V_{gs} , was varied from 0 to 20 V, at the same time drain–source voltage, V_{ds} , was varied from 0 to 20 V ($V_{ds} = V_{gs}$) and corresponding drain–source current, I_{ds} , was measured. The V_{th} of each device was measured from V_{gs} – I_{ds} graphs using linear approximation method. The variation of first derivative of the V_{gs} – I_{ds} graph was also measured. Each I–V characterization was performed for five times, and average threshold voltage was reported. For one of the SiC power MOSFETs, the V_{th} voltage measurement was performed for 25 times to understand transient behavior of the measurements and distinguish them from stress-related variations.

During accelerated thermal aging test, a set of ten devices from each manufacturers (total 30) were stressed at a 120 °C for 200 h inside a muffle furnace. Each device was then tested for 100 h to identify the degradation of static behavior.

An experimental setup was built to perform bias temperature instability measurement for multiple power MOSFETs (10 at a time) at the same time as shown in Fig. 1. In this setup, temperature was set at 120 °C, and an Omega benchtop PID controller was used to maintain the desired temperature. At the same time, an EL302RT Triple Power Supply was used to apply a constant gate–source bias voltage, V_{gs} , of +20 V across each devices simultaneously.

Table 1 SiC power *n*-MOSFETs specification

Manufacturer	Voltage rating, V_{ds} (V)	Current rating, I_{ds} (A)
A	1200	24
B	1200	20
C	1200	22

Fig. 1 Characterization tool to perform bias temperature instability measurement of SiC power MOSFETs

3 Results and discussion

The variation of V_{th} of a SiC power *n*-MOSFET before applying stress is shown in Fig. 2, and the I–V measurements were run for 25 times. V_{th} showed a transient behavior throughout the measurements, due to the uneven distribution of dopant atoms in the channel and oxide thickness throughout channel length [8]. It is a good indicator that a slight increment or decrement of V_{th} , before and after electrical or thermal stress, does not dictate any gate oxide degradation. However, repetitive cycling can help to erase the history of the device by resetting transient charges, and therefore provides a more accurate measure of irreversible failure.

Variation of V_{th} accumulated around 4.7–4.8 V range, while the average is not fixed. I_{ds} is a function of V_{th} ; I_{ds} followed Lorentzian fluctuation, which was due to the

Fig. 2 Pre-stress variation of threshold voltage for a SiC power MOSFET manufactured by B

presence of $1/f$ noise which reflected capture and emission of charge carriers by active traps [9]. An increase in the V_{th} (from 4.7 to 4.8 V range) reflected an increase in negative trap density (NMOS) on the channel near the source end. On the other hand, Ashraf et al. [10] mentioned that a decrease in the V_{th} (from 4.8 to 4.7 V range) reflected an increase in negative trap density (NMOS) on the channel near the drain end. This testing allows us to see movement of active traps along the channel during measurement. As observed here, the trap density and total number of impurities distribute evenly across the channel as V_{th} moves toward the average value.

Figure 3 demonstrates the $V_{gs}-I_d$ behavior of a device (device # 4 from manufacturer A) before and after accelerated thermal stress. It should be mentioned that this device showed the highest amount of variation in the V_{th} (~ 9.6%) after 100 h of thermal stress, while other 29 devices from manufacturers A, B and C did not show such significant variation even after 200 h of thermal stress at 120 °C. As mentioned earlier, for current fluctuation at the strong inversion region, the channel part closer to the source region plays an important role, which means that thermal stress significantly increases number of active trap centers near the source region.

Figure 4 shows the variation of dI_d/dV_{gs} for the same device (device # 4 from A) with V_{gs} . It could be observed

Fig. 3 $V_{gs}-I_d$ variation before (a) and after (b) thermal stress for device #4 from A

Fig. 4 Variation of dI_d/dV_{gs} with respect to V_{gs} for device #4 from A

here that the first derivative of drain current fluctuates significantly at inversion region. The peak position of dI_d/dV_{gs} dictates the value of V_{th} . Therefore, this fluctuation reflects the change of V_{th} due to accelerated thermal stress.

Out of 30 devices, only one device (3.33%) showed a significant variation of V_{th} after 100 h of thermal stress, while no other device showed such a high deviation even after 200 h of thermal stress. If this significant change (9.5%) of V_{th} is count as a failure, relatively higher rate of failures at the beginning dictates higher infant mortality of the device, which follows Weibull distribution. On the contrary, zero or lower rate of failure at 200 h dictates lower random failure happenings at the later stage of stress, which also follows Weibull distribution. However, more points and longer duration of stress are required to understand complete aging profile and Weibull distribution for the SiC power MOSFETs.

The variation of V_{th} for the SiC power MOSFETs which were stressed during bias temperature instability measurements, is shown in Fig. 5. The measurements were performed immediately after the devices were removed from stress set-up. It was observed that with the stress time, the threshold voltage shifted gradually and it demonstrated a trend of saturation at higher stress time (except A12). The change in V_{th} reflects the activation of near-interfacial oxide traps in the channel region as mentioned in [3]. The positive change in V_{th} increases the ON-state resistance of the device and eventually decreases device efficiency. The negative change in V_{th} (device #A12) causes drain leakage current during OFF-state which eventually leads to device-failure [3]. Out of total 30 power devices tested, only one showed a negative change in V_{th} .

The trend line of V_{th} over stress time for devices from manufacturer B and manufacturer C is shown in Figs. 6 and 7. From Fig. 6, it was observed that V_{th} increased initially with the thermal and electrical stress, and eventually saturated toward an average V_{th} value with further stress.

Fig. 5 Variation of threshold voltage with respect to stress time during bias temperature instability measurements (devices from A)

Fig. 7 Variation of threshold voltage with respect to stress time during bias temperature instability measurements (devices from C)

Fig. 6 Variation of threshold voltage with respect to stress time during bias temperature instability measurements (devices from B)

From Fig. 7, it was observed that V_{th} increased with the stress time expect devices C2 and C6. For devices C2 and C6, V_{th} fluctuated and eventually moved toward a saturated value. Regardless of the fluctuations, for every devices V_{th} moved toward an average value.

The research is focus toward device operation under harsh environment. One of the key environmental

stressors for harsh environment is neutron radiation. The reliability testing under neutron irradiation for 1200 V SiC MOSFET showed low failure rate (0.1 device failure per 1 billion hours) at sea-level radiation exposure operated at rated 1200 V. The failure rate increases exponentially with the operating voltage above the rated voltage [11].

4 Conclusion

1200 V SiC power *n*-MOSFETs from three different manufacturers were tested for reliability by accelerated thermal aging and bias temperature instability mechanisms. SiC power MOSFETs demonstrated very low failure rate during accelerated thermal aging and bias temperature instability testing which demonstrated their reliability for high-temperature operations.

Funding This work was funded by Department of Energy—Power-America (Grant PA100215CFP51). Part of this work is also supported by U S Department of Energy (DoE), Office of Science, Office of Basic Energy Sciences, under DoE contract number DE-AC02-06CH11357.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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