Capacitor-within-capacitor

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Abstract

Capacitors are typically connected together in one of two configurations: either in series, or in parallel. Here we study a capacitor-within-capacitor configuration. Simulations and experiments indicate that the overall capacitance of the structured cell may be made larger than an ordinary two-plate counterpart by at least 50%. Simulations also indicate that the cell's capacitance may be controlled by the gate voltage. Overall, this concept is deemed suitable for microfluidic sensing and possibly for energy storage elements.

Keywords Capacitors · Capacitor-within-capacitor · Energy storage · Electronic circuits · Electronic sensors

1 Introduction

In equivalent circuit terms, capacitors may be connected in series (the overall capacitance becomes smaller than either capacitors), or in parallel (the overall capacitance is the sum of individual capacitors) [1]. Here we consider a third possibility, a capacitor-within-capacitor (CWC) configuration. Specifically, one capacitor, the gate capacitor is placed either within (inner gate construction) or outside (outer gate construction) a cell capacitor. Such concept is general and may be applied to dielectric capacitors (body of the manuscript) and super-capacitors (Supplementary Information, SI section). Simulations on the control of such structure by the gate voltage are provided in the SI section, as well. One may argue that if a cell capacitor is maintained at, or limited to a constant voltage, then more energy may be stored by this design.

In a nutshell, nesting a capacitor within another (Fig. 1) alters the cell's capacitance because of the mutual capacitance that appears between every pair of electrodes. For a large parallel plate capacitor, the mutual capacitance is mainly between the two adjacent electrodes (nearest neighbor electrodes); the next nearest electrode are

effectively masked away. Thus, the structure in Fig. 1b is made of 3 such capacitors connected in series. For simplicity, let us assume that all three capacitors have the same capacitance, C . Then, the overall cell capacitance is $C/3$. If the inner capacitor is short, then, the overall cell capacitance is now $C/2$ since we now have only two capacitors in series. A more attractive example is when the cell is nested within the gate capacitor. In this case, the cell's capacitance is increased by 50%; from C to $3C/2$ (see the Discussion section, Fig. 7). Equivalent circuit arguments above are limited to thin electrodes. Thicker electrodes have self-capacitance and more importantly, introduce polarization across them. Similarly to giant molecules, such polarization may be viewed as effectively increasing the permittivity within the capacitor and leading to substantial capacitance change.

Simulations of the structure under a short and open inner gate are provided in Sect. 2, with more simulations provided in the SI section. Experiments in Section III reveal that one can affect the cell's capacitance by simply connecting the gate electrodes with a variable resistor. Equivalent circuits are provided in Sect. 4. It is worth noting that equivalent circuits do not take the thickness of the

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Fig. 1 **a** An ordinary parallel plate dielectric capacitor is made with two metal electrodes, separated by a dielectric material. **(b)** A capacitor-within-a-capacitor can be made by nesting another capacitor within the ordinary structure

electrodes into account; thin gate electrodes do not fully mask the polarization effect of the cell. By replacing the dielectric in the capacitor with ionic liquid, a much larger effect is obtained. Both simulations and experiments demonstrate that the overall cell's capacitance increases upon introducing a gate structure, either outside or inside the cell. It is, therefore, suggested that one can accumulate more charges on a low voltage capacitors, realizing a better energy storage.

2 Simulations

Dielectric capacitor—inner gate electrodes The dielectric capacitor is shown in Fig. 1. The outer capacitor (C_{cell}) is polarized by a potential difference V_0 between the cell's electrodes. A finite-element code (Comsol) was used for the simulations. The cell's capacitance is simply the simulated terminal charge divided by the cell's voltage ($V_0 = 1$ V in our case). As discussed in Sect. 4.1. Energy Considerations, limiting our attention to the cell's capacitance does not violate any energy conservation law since the energy used for charge separation at the gate is reflected through

a change in charge at the cell's electrodes. The structure was assumed to be immersed in a liquid dielectric with a relative dielectric constant of $\epsilon_r = 100$.

Let us consider two cases where the gate electrode are floated (namely, not grounded): in case 1 (Fig. 2a) the gate is open whereas in case 2 (Fig. 2b) the gate is short. A short gate case was mimicked by connecting its edges with a floated line. As can be seen from Fig. 2b, the potential distribution within the gate region is constant (as it should be). The cell's capacitance of the open gate was assessed as 1.44 nF whereas the cell's capacitance with a short gate was 1.86 nF; an increase of 29%.

More simulations on the control of a CWC by a gate bias and numerical assessment applicable to (super)capacitors are provided in the SI section.

3 Experiments

Methodology: the 4×4 cm² electrodes were made out of 25 micron copper foil, with a protruding notch in each plate, left for contact. This way, the thickness of the electrode has not been altered by a wire contact. The dielectric material was a 110 micron thick plastic transparency film and the entire structure was held between two glass plates by two paper clips. A 90 micron soaked lens tissue with ionic liquid (1-*n*-Butyl-3-methylimidazolium hexafluorophosphate, Thermo-Fisher) served as an electrolyte as well. A hand held multi-meter (BK Precision) and LCR bridge (QuadTech) were used for the capacitance measurements. The simulations were DC calculations whereas a typical capacitance measurement employs a small AC signal. Under small AC signal approximation any independent DC voltage source is treated as a short due to its small internal impedance. Indeed, the measured cell capacitance, with a gate battery in place, was exactly the same as for the case where the two gate plates were short. In order to observe the effect of the gate bias on the cell capacitance at AC

Fig. 2 **a** Potential distribution for a floated and open gate (the gate is formed by the two inner electrodes). **b** Potential distribution when the inner gate electrodes are connected (namely, the gate is short)

frequencies, one needs to synchronize it with the cell's measurements or dope the dielectric layers.

For the AC measurements, an external trigger (not shown) drove the scope and Ground was provided by the function-generator. Since the system may have its own capacitance, a reference trace of only the signal is provided below (Fig. 7). The system capacitance was smaller than the cell's capacitance when including the open gate structure.

3.1 Cell capacitance with inner gate construction

Inner gate configuration is depicted in Fig. 3a. Results were obtained with a hand-held unit.

Fig. 3 **a** Experiment: when the inner gate electrodes are open. The measured cell's capacitance is 0.111 nF. **b** Experiment: the inner gate electrodes are connected by a yellow jumper (short). The cell's capacitance is 0.159 nF. Red wire: positive cell's contact; black wire: negative cell's contact; the yellow jumper provides contact between the inner (gate) electrodes. The reading for an ordinary cell without the gate structure exhibited results similar to those obtained for an open gate structure

Fig. 4 **a** Reversing the roles of CWC: the cell capacitor is defined by the inner electrodes set whereas the gate capacitor is constructed by the outer electrode set. **b** Experiment: the outer gate electrodes are open. The cell's capacitance is 0.313 nF. **c** Experiment: the

3.2 Cell capacitance with outer gate construction

A complementary design and its related experimental data are provided in Fig. 4.

Since the cell's capacitance increases when the gate capacitor is short, then one may ask what happens if a variable resistor is placed across the gate structure (shunt resistor). One expects that for very large resistors the gate capacitor is effectively open and hence the cell's capacitance is the smallest. On the other hand, when the shunt resistor is very small, the gate capacitor is effectively short and the cell's capacitance would be the largest. The variable resistor was simply a resistor bank; each resistor defined within 1% resolution. The shunt resistance could be varied without removing its leads from the gate electrodes.

From circuit point of view, adding a shunt resistor in parallel to the gate capacitor would affect the gate impedance (both real and imaginary components) and hence, will affect the cell's capacitance. The cell's capacitance as a function of the gate's shunt resistance is expected to be semi-linear as shown in Fig. 5. As the shunt resistance increases, the cell's capacitance decreases, as also expected.

The scalability of the design is demonstrated by replacing the 'ordinary' plastic dielectric layer with ionic liquid. A 90 micron thick lens-tissue was soaked with the ionic liquid for 30 min. The results are summarized in Table 1. The cell's capacitance has increased when the gate is short. Note the factor of ca 100,000 when the ionic liquid replaces the 'ordinary' dielectric.

3.3 AC measurements

The overall capacitance of the cell may be assessed through the rise, or decay time of a 10 kHz square wave.

outer gate electrodes are connected by a yellow jumper (short). The capacitance is 0.446 nF. Red wire: positive cell's contact; black wire: negative cell's contact; the yellow jumper provides contact between the outer (gate) electrodes

Fig. 5 The experimental configuration for an inner control (a) and an outer control (b). c Cell's capacitance as a function of shunt resistance; inner gate control. d Cell's capacitance as a function of shunt resistance; outer gate control. $C = 0.29$ nF is the limiting cell's capacitance when the gate cap is open (when the shunt resistance approaches infinity)

Table 1 Electrolytic CWC with ionic liquid

Gate control	Gate status	Cell's capacitance (μF)
Inner	Open	23.6
Inner	Short	34.5
Outer	Open	66.4
Outer	Short	93.2

The signal was applied to the outer terminals (Figs. 6a–d) using a function-generator. A 1 KΩ resistor was connected in series between the function-generator and the positive outer terminal leads. The output resistance of the functional generator was 600 Ohms. The reference circuitry is shown in Fig. 6a. Results for the gated experiments are shown in Fig. 6b–d. A floating gate is shown in Fig. 6b. If the polarity of the gate counters the polarity of the cell capacitor (Fig. 6c), then, the time constant and hence the overall cell's capacitance increases. If the polarity of the gate capacitor is in same the direction as the cell's polarity, then, the overall cell's capacitance decreases (Fig. 6d). The redrawn curves from the oscilloscope are plotted in Fig. 6e with a B-Spline fitting function.

4 Discussion

Let us consider a circuit approach to an inner gate configuration with floating electrodes (Fig. 7a). As mentioned earlier, this approach ignores the developed polarity across each electrode. The cell capacitor is made of three capacitors in series—the mutual capacitance between every

nearest plates. We ignore the effect from next-nearest plates because they are masked by the nearest parallel plates. Let us further assume that each capacitor, formed between every two adjacent electrodes is of value C . Then, the total cell's capacitance is made of three capacitors in series whose overall value is $C_{\text{cell}} = C/3$. This value is the same as the value for a single capacitor whose electrode spacing is 3 times larger than the spacing that constituted capacitor C . On its face, we have no advantage in stuffing an inner gate capacitor within a larger one other than complicating the simpler structure. Yet, along with Fig. 7b, if the inner gate is short, then the cell capacitance is now $C_{\text{cell}} = C/2$. This is 50% larger than either the ordinary or the structured configuration.

Outer gate construction (Fig. 7c) also results in a 50% capacitance increase when the outer gate is short. In this case, the capacitor of value C is in parallel to two other capacitors, each of value C , which are connected together in series. Overall, $C_{\text{cell}} = (C + (1/C + 1/C)^{-1}) = C + C/2 = 3C/2$.

If we ground one electrode instead of a mid-short in Fig. 7b, then, the cell capacitance is made of a capacitor C in parallel to two capacitors in series (Fig. 7d): $C_{\text{cell}} = C + (1/C + 1/C)^{-1} = 3C/2$. Such construction also enables charging the mid-capacitor by another voltage source, V_g (see SI section).

In electric field terms, the increase in the cell's capacitance is attributed to the polarity of the gate structure, either for inner or outer construction. The gate dictates the polarity of the electrolyte filling the cell (the dielectric constant, so to speak). The larger this polarity is, the larger would be the cell's capacitance. Such induced capacitance is similar to artificial dielectrics [2–4]—dielectrics that are filled with floating metallic or semi-conductive objects to affect their permittivity values. Put it differently; the gate

Fig. 6 **a** The circuit used as a reference. **b–d** The circuits used with the structured gates. **e** Redrawn traces of Voltage vs Time for the corresponding circuits. B-spline function was used to fit the extracted points

Fig. 7 **a** The equivalent circuit for inner gate construction results in a total capacitance of $C/3$, similar to an ordinary parallel plate capacitor. **b** Short inner gate with a floating potential diagram exhibits a total capacitance of $C/2$ compared with $C/3$ of the ordinary or 50% capacitance increase. **c** Outer gate construction result in a capacitance increase of 50%, as well. **d** Instead of a short in **b** one grounds one junction, and the overall cell capacitance is $C + (1/C + 1/C)^{-1} = 3C/2$

capacitor draws counter charges to its electrodes resulting in more electronic charges drawn to the cell's electrodes.

Unlike what may be deduced from equivalent circuitry, field simulations indicate that the particularities of the gate permittivity only marginally affect the overall cell's capacitance. For example, varying the permittivity value for an inner gate structure by three orders of magnitudes, from 1 to 10^3 changes the overall cell's capacitance by less

than 1%. That means that the larger effect is related to the induced surface charges across the gate electrodes and not to its capacitance.

The advantage of such multiple-electrode structure is clearer when placing the cell capacitor within an outer gate (see the SI section for more details). There, one takes a full advantage of the smallest spacing possible for the cell capacitor and increases it further by encapsulating it with

an outer gate structure (Table 1). The equivalent circuit is again made of two capacitors in series, which are connected in parallel to the third; therefore, there is an overall capacitance increase (50% in our case) when comparing it with a single capacitive element.

Application to pulse shaping is also described in the SI section. There, one is adding a nonlinear element, such as a diode to the input signal to affect either the rise or decay times (but not both) of a pulse.

4.1 Energy considerations

The broader question is: what do we gain by complicating the simple parallel capacitor's design? This is a linear system after all; in the absence of heating loss, all energies invested in charge separation are added up. In general, and if the electrodes are kept at a given potential, V_i , the energy stored in an array of conductors is written as [1],

$$U = 1/2 \sum_{ij} C_{ij} V_i V_j = 1/2 \sum_i Q_i V_i.$$

Here, C_{ii} , C_{ij} , V_i and Q_i are the coefficient of self-capacitance, the coefficient of inductance between conductors i, j , the potential on the i th conductor and the charge on conductor i , respectively. In our case, $U = 1/2(Q_{\text{cell}}V_0 + Q_gV_g)$ with Q_{cell} and V_0 , respectively, the charge and potential on the cell's electrode and Q_g and V_g are, respectively, the charge and potential on the gate electrodes. These two quantities are not arbitrarily determined and there is a linear relationship between them.

Let us consider the case where the two gate electrodes are connected together by a wire (namely, are short). The total charge on the gate is zero. Yet, the polarization by the cell displaces the gate charge and creates a charge separation across the gate. Let us denote the induced charge on the gate electrode as q . The charge on a stand-alone

cell's electrode, Q_0 , will be modified as a result of this induced charge: $Q_{\text{cell}} = Q_0 + q$. The total stored energy has therefore increased by qV_0 . Likewise, the cell's capacitance has increased: $C_{\text{cell}} = C_0 + q/V_{\text{cell}}$. Typically, $V_{\text{cell}} = V_0$ is kept constant. The energy increase is supplied by the external source at potential V_0 , and we note that an ideal voltage source is defined as a source that can provide any required current or, charge for that matter while keeping the voltage constant.

5 Conclusions

Adding gate electrodes to a cell capacitor may be designed to increase the overall cell capacitance. This is beneficial when the cell capacitor has a bias limit to its potential, e.g., in the case of many (super)capacitors. Interfacing this structure with nonlinear elements (such as diodes, transistors, or even light activated materials) is an exciting possibility.

Compliance with ethical standards

Conflict of interest The author declares that have no conflict of interest.

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