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REVIEW PAPERS

Promising Lithography Techniques for Next-Generation Logic Devices

Rashed Md. Murad Hasan[1] · Xichun Luo[1]

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Abstract
Continuous rapid shrinking of feature size made the authorities to seek alternative patterning methods as the conventional photolithography comes with its intrinsic resolution limit. In this regard, some promising techniques have been proposed as next-generation lithography (NGL) that has the potentials to achieve both high-volume production and very high resolution. This article reviews the promising NGL techniques and introduces the challenges and a perspective on future directions of the NGL techniques. Extreme ultraviolet lithography (EUVL) is considered as the main candidate for sub-10-nm manufacturing, and it could potentially meet the current requirements of the industry. Remarkable progress in EUVL has been made and the tools will be available for commercial operation soon. Maskless lithography techniques are used for patterning in R&D, mask/mold fabrication and low-volume chip design. Directed self-assembly has already been realized in laboratory and further effort will be needed to make it as NGL solution. Nanoimprint lithography has emerged attractively due to its simple process steps, high throughput, high resolution and low cost and become one of the commercial platforms for nanofabrication. However, a number of challenging issues are waiting ahead, and further technological progresses are required to make the techniques significant and reliable to meet the current demand. Finally, a comparative study is presented among these techniques.

Keywords Nanolithography · Throughput · Resolution · Defect density · Overlay

Abbreviations

AIMS^{TM}	Aerial image measurement system^{TM}
BCP	Block copolymer
CAR	Chemically amplified resist
CD	Critical dimension
CDU	Critical dimension uniformity
CHIPS	Chemo-epitaxy induced by pillar structures
CMG	Chemically modified graphene
CoO	Cost of ownership
COOL	Coordinated line epitaxy
DPP	Discharge produced plasma
DRAM	Dynamic random access memory
DSA	Directed self-assembly
EBL	Electron-beam lithography
EPE	Edge placement error
EUV	Extreme ultraviolet
EUVL	Extreme ultraviolet lithography
FEL	Free-electron laser
FIBL	Focused ion beam lithography
HIM	Helium ion microscope
HP	Half pitch
HSQ	Hydrogen silsesquioxane
HVM	High-volume manufacturing
IC	Integrated circuit
ITRS	International technology roadmap for semiconductors
LADI	Laser-assisted direct imprint
LAN	Laser-assisted nanoimprint
LELE	Litho-etch-litho-etch
LER	Line edge roughness
LiNe	Liu–Nealey chemo-epitaxy
LPP	Laser produced plasma
LWR	Line width roughness
MEBDW	Multiple E-beam direct write
NA	Numerical aperture
NDM	Nano-defect management
NGL	Next-generation lithography
NIL	Nanoimprint lithography
NPGS	Nanometer pattern generation system
OAI	Off-axis illumination

✉ Xichun Luo
xichun.luo@strath.ac.uk

[1] Centre for Precision Manufacturing, Department of Design, Manufacture and Engineering Management, University of Strathclyde, Glasgow, UK

OPC	Optical proximity correction
PMMA	Poly(methyl methacrylate)
PS-*b*-PDMS	Polystyrene-block-poly(dimethylsiloxane)
P2VP-*b*-PDMS	Poly(2-vinylpyridine)-block-poly(dimethylsiloxane)
RESCAN	Reflective-mode EUV mask scanning lensless imaging microscope
RET	Resolution enhancement technologies
RLS	Resolution LER sensitivity
RTP	Roll-to-plate
RTR	Roll-to-roll
R&D	Research and development
SADP	Self-aligned double patterning
SAQP	Self-aligned quadruple patterning
SEM	Scanning electron microscope
SMART™	Surface modification for advanced resolution technology™
SMO	Source-mask optimization
SPIE	Society of Photographic Instrumentation Engineers
STEM	Scanning transmission electron microscope
S-FIL	Step-and-flash imprint lithography
193i	193-nm Immersion lithography

1 Introduction

In the last few decades, the semiconductor industries had followed the Moore's law; the number of transistors per chip had been doubling each process generation. Figure 1 shows the logic transistor density over the last decade and the future trend using a quantity density metric. The linear scale implies a doubling of density every 2 years. Intel has announced the new 10-nm process that achieves 100.8 million transistors per square millimeter. This provides notable 2.7 times transistor density improvement over its predecessor and suggests that Moore's law is likely not slowing down. This enhancement of transistor density has been done by shrinking the sizes of the transistors. However, the industries have demanded sub-10-nm nodes patterning to meet the growing requirements. As reported by the International Technology Roadmap for Semiconductors 2015 (ITRS2015), new type of logic devices (Gate-all-around structures) have already been introduced [1]. These new devices will replace the fin structures soon. This report also demonstrates the development of many new types of memory devices that can be the possible alternatives in the future.

These new devices will also push patterning to manufacture even smaller nanostructures. Although this rapid shrinking of feature size permits for faster processing with more power efficiency at a lower cost, it intensely enhances the design complexity and introduces various manufacturing challenges. Table 1 shows the ITRS roadmap requirements for the lithography techniques. Consequently, lithography must accomplish the stringent industrial requirements with excellent capability to meet the future challenges.

Photolithography has been the dominant method of patterning nanoscale features for the microelectronics industries since the commencement of the ICs. Resolution enhancement technologies (RET) and immersion method enables the photolithography with patterning beyond its intrinsic resolution limit. RET improves the quality of an image. It generally includes phase shift mask, optical proximity correction (OPC), modified or off-axis illumination (OAI) and multiple patterning. Although they have extended the capability of the lithography process, these methods experience some restrictions as well. Phase shift method has some limitations on implementation of mask due to phase termination problems and mask fabrication difficulties. The OPC technique introduces layout restrictions and prohibitive costs to make the corrected masks, while OAI presents complexity to the illumination source in the wafer stepper and to the mask design.

Multiple patterning is the main technique for current sub-20-nm volume manufacturing, which enables to print the patterns that are smaller than the single exposure lithographic resolution limit using multiple process steps. There are many different techniques to implement multiple patterning including litho-etch-litho-etch (LELE), self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP). However, more and more masks will be required for finer process nodes, resulting in prohibitively expensive manufacturing cost and it requires much tighter overlay control than single patterning [4]. 193-nm immersion lithography (193i) has given influential boost to the further development of microelectronics, and the 22- and 14-nm nodes are currently manufactured with multi-patterning immersion ArF lithography [5]. However, this technique brings enormous process challenges like leaching, immersion defects and the filling methods of a purified medium. Despite the challenges, it has been the mainstream lithographic technique used in manufacturing industries since last decade. Now it is reaching its intrinsic limits.

Despite the high-resolution capabilities, X-ray lithography (utilizes X-rays wavelength of 0.4–4 nm) techniques were proved unsuccessful to provide an economically attractive lithographic process due to some difficulties. One of them was to find the right combination of materials and

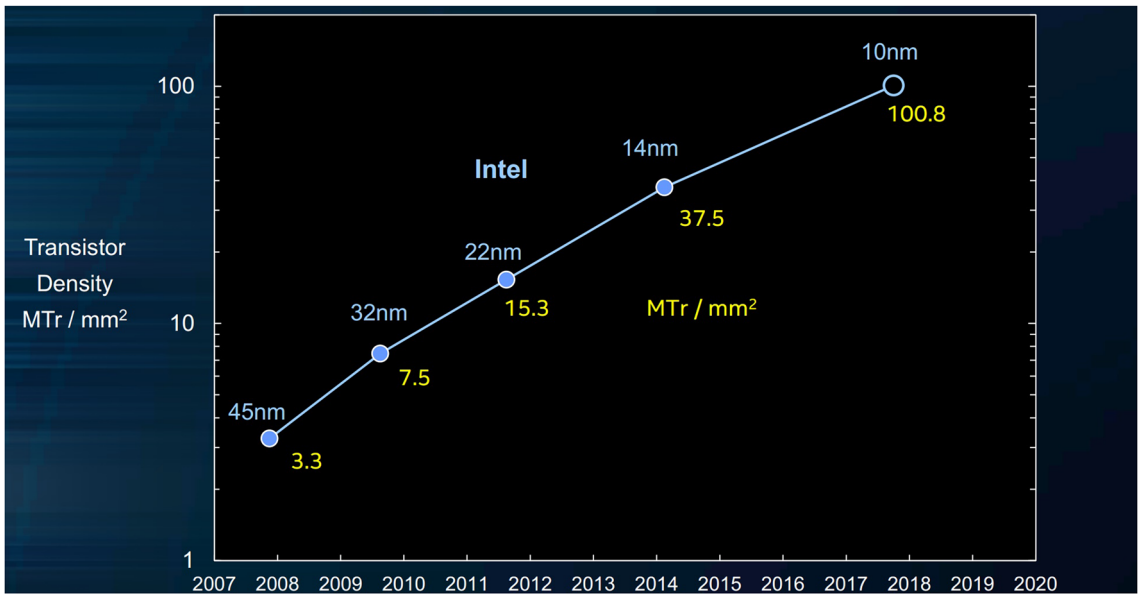

Fig. 1 Logic transistor density [2]

Table 1 ITRS roadmap requirements [3]

Specification (mm)	2017	2018	2019	2020	2021	2022
Minimum critical level Half Pitch (HP)	13	12	11	10	9	8
Minimum hole dimension	18	16	14	13	11	10
Line width roughness (LWR)	1.4	1.3	1.1	1.0	0.9	0.8
Minimum pattern defect size	10	10	10	10	10	10
Overlay	3.4	3.0	2.7	2.4	2.1	1.9
Minimum hole critical dimension uniformity (CDU)	0.5	0.4	0.4	0.3	0.3	0.3

wavelength. Wrapping of absorber material due to internal stresses is an issue to mitigate. Furthermore, the most critical point is the failure to furnish suitable masks as these masks had to be unity magnification and the requirement of creating the mask from adequately X-ray absorbing materials. Again, the requirement of thick absorber layers and membranous nature of the substrate made X-ray lithography unpopular in nanofabrication arena.

As the conventional photolithography has approached its ultimate limits, considerable efforts have been devoted to NGL techniques by various research laboratories and industries around the globe. These techniques are extreme ultraviolet lithography (EUVL), electron-beam lithography (EBL), focused ion beam lithography (FIBL), nanoimprint lithography (NIL) and directed self-assembly (DSA). They have the potentials as the replacement to conventional photolithography.

With the increasing in patterning resolution, resist is one of the key challenges for the adoption of the patterning techniques in HVM industries. The next-generation potential techniques drive the need for resist materials with high resolution, high sensitivity and low LWR. However, it is difficult to achieve high resolution, low line edge roughness (LER) and low sensitivity simultaneously due to an inherent trade-off relationship between each other (RLS trade-off). Therefore, the development of advanced resist materials will be required to break the RLS trade-off relationship. In addition, the next-generation resists must have the ability to mitigate the stochastic barrier. The advancement of new resist materials is entering a new age with the accompanied challenges and opportunities to fulfill the stringent requirements for the future patterning techniques. In this review report, we will discuss the mechanism, overall status and the challenging issues for the NGL techniques as well as the general issues related to resist materials.

2 Extreme Ultraviolet Lithography

2.1 Mechanism

Due to wavelength limitations, current attentions are directed toward developing EUVL which uses extreme

ultraviolet radiation to increase efficiency, reduces manufacturing cost and supports the development of processing power. In the last decade, researchers put extensive interest in EUVL as a 'next wavelength' replacement for 193-nm dense-UV lithography [6]. EUVL utilizes 13.5-nm photons that are obtained typically from a plasma source. EUV light is then collected by an optical element called a 'collector.' Light from the collector is focused into the illuminator (formed of multilayer-coated normal incidence mirrors as well as grazing incidence mirrors) through an intermediate focus. The illuminator illuminates the right amount of light and guides it onto the reticle stage (i.e., a mask). The reflected image of the reticle arrives into the projection optics (consist of six or more multilayer mirrors) with a demagnification. Finally, the image is focused onto the wafer stage to form a pattern into a substrate coated with a photoresist. Every step is operated in a low-hydrocarbon, high-vacuum environment. Figure 2 shows a schematic of a EUVL exposure system [7].

2.2 Status and Challenges

Over the last few years, considerable progress has been made to move EUVL toward increased high-volume manufacturing (HVM) viability. Most remarkably, there have been substantial developments to exposure throughput, reliability, variance control and patterning materials for the high resolution required [8, 9]. Currently, EUVL is projected to use in manufacturing at the 7-nm node or beyond [10]. ASML, a leading company involved in the development of EUVL tools, revealed that more than 1000 wafers per day had been exposed on its NXE:3300B EUV system over multiple weeks' duration [8]. They have also claimed that the throughput specification of 125–150 wafers per hour has been achieved on TWINSCAN NXE:3400B lithography system [11]. Although, the targeted 4-week average availability (80%) has been achieved by 2016, it needs to continue to improve further [8].

In terms of production timescales, ASML predicts it will go into production in 2018 [1]. The source power, masks and resist materials still have critical issues for mass production. For the future technology at the 5-nm node and beyond, sources powers of 500–1000 W at a reduced operational cost per wafer may be required [12]. Laser produced plasma (LPP) and discharge produced plasma (DPP) are two main techniques to produce EUV sources. The source power has been improved ten times in last 5 years [13]. Mizoguchi et al. [14] reported that more than 250 W LPP-EUV powers could be generated by using plasma generation schemes. Another approach by using FEL (free-electron laser), many tens of kilowatts power can be produced [15]. Mitsubishi electric has successfully explored a higher average power CO_2 laser more than 20 kW at output power [16]. Now they are developing new high-power HVM LPP-EUV source with more than 25 kW CO_2 driver laser system. Although EUV source technology is very close to the requirements, some cost of ownership issues need to be investigated before the insertion of EUVL

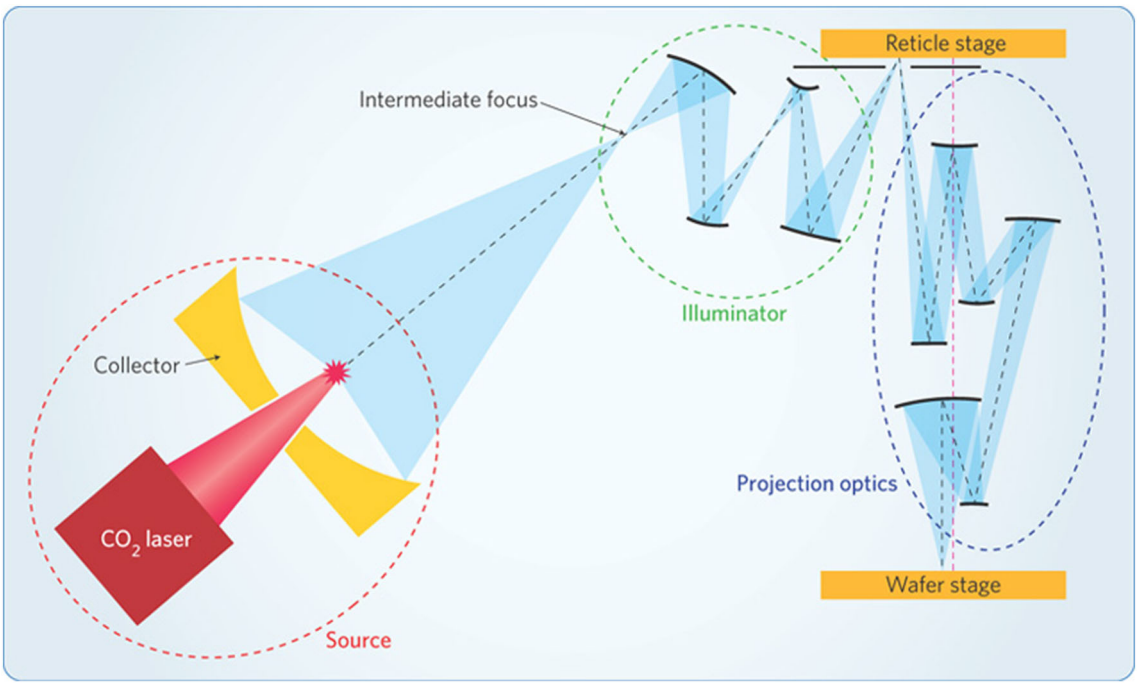

Fig. 2 Schematic of a EUVL system [7]

into HVM. For further improvement, novel approaches for power sources are being still investigated [17, 18].

A key factor for adoption of EUVL in HVM is the choice of EUV resist with high sensitivity, high resolution, low LER, low LWR and better contact hole CDU. Chemically amplified resists (CARs) have effectively achieved the scaling requirements of the semiconductor industry [19]. RLS performance and stochastic variations are the key issues for the CARs as well as for other resist materials. High-sensitivity (< 20 mJ/cm^2) resist materials are required to reduce the development cost of high-power exposure sources that in turn leads to large LER values. Acid diffusion in CARs influences these performances. Vesters et al. [20] have reported that by selecting an appropriate ratio of quencher to PAG (photo-acid generator), an EUV dose reduction of up to 12% can be achieved with 240 s PEB (post-exposure bake) time, while keeping LWR and resolution constant.

For better optimization of these parameters, some other resist materials and approaches have been studied. Non-chemically amplified resists (non-CARs) show high-resolution capability, high sensitivity and low LER as they have no acid diffusion issues. Some researchers have reported the development of the metal containing photoresist that has high sensitivity performance, which will be very helpful for the low-energy power source to realize EUVL [21, 22]. Some other new techniques including nanoparticle photoresists with high sensitivity have been reported [23–26]. Lately at the 2016 SPIE Advanced Lithography conference, a good amount of papers was presented demonstrating the substantial research on Photosensitized CARs [27–31]. Moreover, some approaches have been introduced to improve sensitivity, LWR and local CDU from many directions [32, 33].

However, it is urgent need to mitigate the stochastic failures such as broken line, nano-bridge, merging holes and closing holes. These nano-failures are influenced by many factors including aerial image quality, photon absorption, acid shot noise and acid diffusion. The probable solutions lie with the co-optimization of variety of different aspects (materials used, hardware, metrology etc.). Exposure dose can be an effective knob to drive down the failures. Higher dose absorber materials can reduce the stochastics. Moreover, the substrate underneath the resist influences the exposure dose and the LWR, and therefore, optimization of the substrates could be a potential improvement knob to the exposure dose and LWR reduction [34].

Pattern collapse is another challenging issue faced by the resists patterned at high resolution. Several strategies have been proposed to mitigate this problem. Since the capillary forces are one of the reasons for pattern collapse, eradicating any process steps where liquid–air interface reaches the resist surface can be an effective way to avoid this problem. Moreover, mechanically strong resists are less susceptible to the damage due to the capillary forces [35]. Another way could be controlling the thickness of the resist film properly as thin film can avoid pattern collapse during development and rinse. Some other processes were studied to decrease pattern collapse with increased resolution [36, 37]. However, traditional resolution enhancement techniques are used to extend the EUVL including OPC and source-mask optimization (SMO). By using SMO method, edge placement error (EPE) can be reduced significantly [38]. Over the last few years some organization like CNSE of SUNY Polytech associated with SUNY Polytech SEMATECH have supported the investigation of EUV resist materials and various EUV resists evaluation.

Mask blank defects and yield limit the applicability of EUVL. They are continuing to improve. However, extensive researches are still needed to improve mask materials, fabrication processes, defect inspection and disposition metrology and mask protection. To specify, pellicle and mask inspection are two critical matters to improve overall process defectivity. Highly transmitted and long-lasting pellicles are desirable. The interaction between the oblique incident EUV light and the patterned absorber may cause the mask 3D effects at wafer level. Philipsen et al. [39] have suggested some alternate absorber materials (nickel and cobalt) to reduce the mask 3D effects and improving the overall imaging window. For the defect-free mask manufacturing, an EUV aerial image metrology system, the AIMS^{TM} EUV, has been developed by ZEISS and the SUNY POLY SEMATECH EUVL Mask Infrastructure consortium to actinic review of EUV mask [40]. These actinic tools are very useful for blank inspection, pattern mask inspection, and defect repair verification.

However, Mochi et al. [41] have developed a reflective-mode EUV mask scanning lensless imaging microscope (RESCAN) which has the capability of actinic patterned mask inspection for defects and patterns with high resolution and high throughput. In support of EUVL roadmap, micro-field exposure tools (13.5 nm, 0.5 NA R&D) have been developed by Zygo Corporation [42]. According to ITRS2015 report, ASML is going to produce a 0.55 NA EUV scanner with different magnification in both x and y directions, and it could be available to use in manufacturing in 2021 [1]. ASML has also introduced of its fifth-generation EUV scanner, the NXE:3400B, with improved resolution, overlay and focus [11]. However, the accomplishment of EUVL as part of the integrated patterning techniques remains a critical issue and therefore the workability of EUVL as a patterning technique continues to accelerate.

2.3 Advantages and Disadvantages

Advantages of EUVL are high throughput, wide process windows and extendibility to future nodes. It uses a smaller wavelength which leads to more densely packed components on the microchip, creating faster processing power. Hence, faster computer processors can be achieved with EUVL. This technique has the potential to provide economic sustainability with its applications in nearly every field including engineering and medical fields. Another advantage of EUVL is cost-effectiveness. Reduced power consumption and a lessened number of exposures make the EUVL more cost-effective in most patterning processes. Disadvantages of this lithography technique are higher startup costs, complexity, reliability and relative infrastructure immaturity.

3 Maskless Lithography

3.1 Mechanism

EBL and FIBL are maskless techniques that are widely used in nanostructure patterning and IC fabrications with its ability to form arbitrary two-dimensional patterns down to the nanometer scale. EBL uses an accelerated electron beam to dramatically modify the solubility of a resist material during a subsequent development step. The electron beam is focused on the resist and then scanned on the surface of the resist with the diameter as small as a couple of nanometers in a dot by dot fashion. Then the patterns can be transferred to the substrate material by etching like other lithographic methods.

Similarly, FIBL involves the exposure by an accelerated ion beam to directly hit the sample surface. When high-speed ions hit the sample surface, energy is transmitted to atoms on the surface, which leads to five possible reactions: (1) sputtering of neutral ionized and excited surface atoms, (2) electron emission, (3) displacement of atoms in the solid, (4) emission of photons, and (5) chemical reactions. Based on these phenomena, FIBL systems are also employed for depositing materials such as tungsten, platinum, and carbon via ion-beam-induced deposition and the implantation that can modify a material surface. Figure 3 shows the process steps of EBL and FIBL system.

3.2 Status and Challenges

However, both methods suffer from low throughput that limits their applications within research and mask/mold fabrication. To increase the system throughput, multiple e-beam direct write (MEBDW) lithography concepts have been pursued with nanometer resolution, using $> 10{,}000$ e-beams writing in parallel [43]. To make direct write practicable for wafers, significant developments in productivity will be required. In recent years, some progresses have been reported including MAPPER (a 5 kV raster wafer writer) [44], IMS (50 kV raster mask writer, single source, many spots in single lens field) [45] and multibeam wafer writer [46]. These are the promising solutions in exposure cost reduction for 20-nm half pitch and beyond. Mapper's 3rd generation platform (FLX) using 650,000 beamlets has been introduced with a target of 40 wafers per hour throughput [47].

As the feature size is shrinking, the resist material plays a significant role for attaining required resolution in EBL. Because of its high sensitivity, sharp contrast and better roughness, PMMA is one of the high-resolution resists that is commonly used in EBL process. Like EUVL, same CARs are often used in EBL and they also suffer the same problem to minimize the RLS trade-off. One of the examples of commercially successful inorganic non-CAR resists used for EBL is Hydrogen silsesquioxane (HSQ) which shows high-resolution (sub $-$ 5 nm) capability, high etch resistance and small local CDU [48, 49]. However, these resists display relatively low sensitivity. Hence, new high-resolution inorganic resist materials with high sensitivity have been proposed such as metal containing resists.

Mapper Lithography, CEA-Leti and Raith are the leading providers and are working to develop turnkey solutions for EBL and FIB systems. In the last decade, less than 10-nm resolution capability by maskless lithography has been repeatedly reported [50–52]. Electron microscope equipped with pattern generator modules enables nanoscale patterning within desired areas. The nanometer pattern generation system (NPGS) is one of the popular SEM (scanning electron microscope) lithography system that provides a powerful, versatile and user-friendly system for doing advanced EBL or ion beam lithography using a commercial SEM, scanning transmission electron microscope (STEM) or helium ion microscope (HIM) [53]. According to ITRS roadmap, the key challenges for these maskless technologies is to build a pilot tool for patterning entire wafers with chip like patterns and overlay control. The earliest insertion of such kind of technology is expected in 2021, and the target would be the '5 nm' logic node [1].

3.3 Advantages and Disadvantages

Electron beam and focused ion beam lithography have advantages of high resolution, high density, high sensitivity and high reliability. As these techniques are maskless, they are the ideal tools for flexible generation for low-volume applications. Due to their intrinsically high resolution,

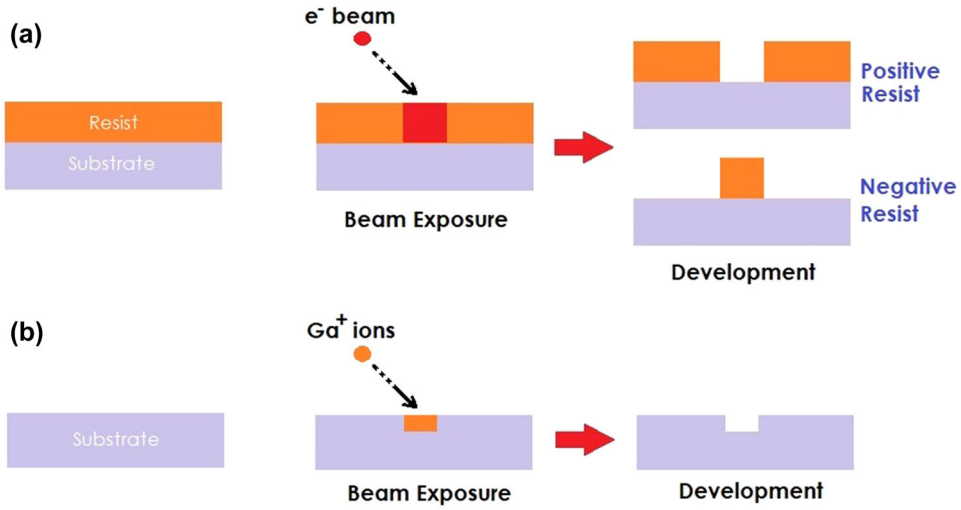

Fig. 3 The process steps of **a** EBL and **b** FIBL system

excellent pattern definition can be achieved. They are highly automated and very accurate control of pattern with direct writing. EBL has greater depth of focus and also a great choice for the formation of masks and templates for the optical lithography and nanoimprint lithography. On the other hand, it has the drawback of low speed and low throughput. It is complicated and expensive system as well. It also suffers from scattering and over exposure problems. Hence this method is not efficient for industrial processing.

4 Nanoimprint Lithography

4.1 Mechanism

Nanoimprint lithography is an advanced nanofabrication method that is capable of high-throughput patterning of nanostructures with high resolution (down to the 5-nm regime). Because of the low cost, reduced process steps and high fidelity, NIL became an attractive technique for a wide range of applications. Nanoimprint lithography methods can be classified into four categories: thermal NIL, UV-NIL, laser-assisted NIL and electrochemical nanoimprints. The basic steps of NIL process are shown in Fig. 4.

In thermal NIL, a fine film of a thermoplastic polymer (imprint resist) is deposited first by spin coating onto the substrate. The next step is to press the prefabricated mold with the substrate together under a certain pressure. Subsequent heating is used above the polymer's glass transition point to achieve the softened polymeric film. In the post-thermal cooling process, the substrate is cooled down, and mold is removed from it, while keeping the pattern resist on the substrate. Finally, an etching process is used to remove the resist residual layer. Youn et al. [54] described a thermal roller NIL approach where the stamp is connected with two moveable springs through the pullers. Replicating of ultra-precision micron scale structures can be achieved with this thermal roller imprinting process at the scan speed of 0.1–10 mm/s.

UV-NIL is a room temperature and low-pressure imprint technique which involves coating of the sample surface with a UV-curable liquid resist. The resist material is exposed to the UV light and the subsequent solidification of the resist under UV radiation. Afterward, an optically transparent mold is pressed into the substrate to extract the patterns. An advantage of using transparent mold is to offer the possibility for easy optical and high-precision alignment. This benefit is employed in step-and-flash imprint lithography (S-FIL), an advanced version of UV-NIL, which can nanopattern the whole wafer in a reduced processing time. In S-FIL, the imprint material (low-viscosity, photo-curable monomer) is dispensed dropwise on the substrate.

The laser-assisted direct imprint (LADI) is a resistless technique that does not require etching. With this technique, a single excimer laser pulse is exposed through the transparent quartz mold to melt a thin surface layer of silicon substrate. Then, the resulting liquid layer is embossed by the quartz mold. Finally, the mold is released after the substrate has cooled down. Various nanostructures with sub-10-nm resolution could be imprinted into silicon wafer using LADI with the embossing time below 250 ns. The capability of high-resolution and high-speed patterning makes the LADI as a promising technique for a variety of applications, and it can be extended to other materials (polysilicon, Ge, and dielectrics) and processing techniques. Similarly, laser-assisted nanoimprint (LAN) lithography utilizes a single excimer laser pulse to melt the polymer. Then a fused quartz mold is used to pattern the nanostructures. This technique can be used in patterning various polymer films on a Si or quartz substrate with high

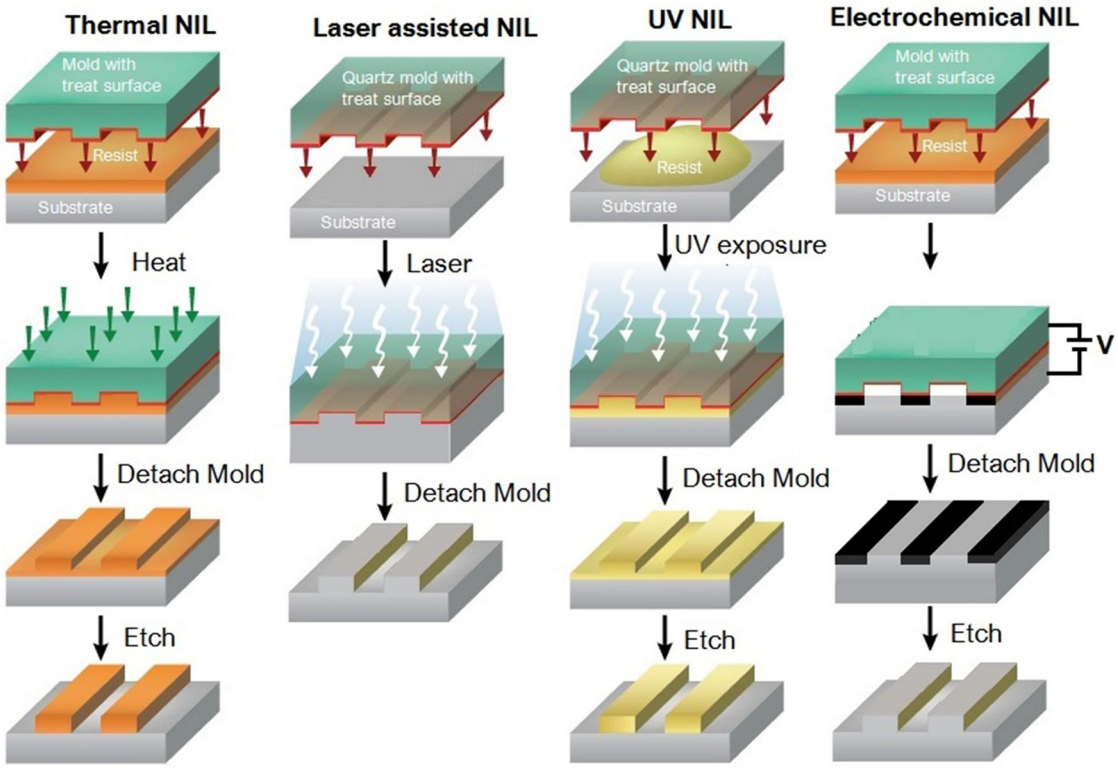

Fig. 4 Basic NIL process steps

fidelity over the entire mold area. Using LAN technique, the imprinting time could be less than 500 ns. The heating and expansion of the substrate and mold can also be reduced significantly so that better overlay alignment between the two can be achieved.

Electrochemical nanoimprinting is a resistless approach that uses a mold fabricated from a superionic conductor. In this process, a voltage is applied between the mold and the target substrate. Once the surfaces of the mold are in contact with the substrate, current flows between them. The strong electric flux from the protrusive parts of the mold to the substrate results anodic oxidation of the substrate surface corresponding to the protrusive parts of the mold with the moisture present between the mold and the substrate. Subsequently, the substrate is etched to achieve the nanostructures like other methods.

4.2 Status and Challenges

Nevertheless, some challenges have prohibited NIL from being adopted on a larger scale such as defectivity, contamination, throughput and overlay issues. Defectivity plays a significant role to meet the cost of ownership (CoO) requirements. Defectivity in NIL process includes non-filled defects, solid phase defects during separation process and particle defects. Non-filled defects are formed due to the contamination to the underlying adhesion layer. Another reason for these defects is shorter resist spread times. During separation process, shear forces imparted between the mask and wafer can slit the feature. Careful controlling of the system during separation can mitigate these defects. To reduce the particle defects, which are located on the wafer and mask, some approaches have been taken including air curtain system and polishing [55, 56]. Recently, it has been revealed that defectivity level has been lessened to below 1 pcs per cm^2 at a throughput of 15 wafers per hour [57]. Another key issue of NIL that should be realized is nano-defect management (NDM) technology that includes defect inspection of templates and imprinted wafer, the resist material innovation and the defect mitigation. These problems can be mitigated through intensive collaboration with various providers. Moreover, substantial studies are required on post-etching resist defects and resist pattern etching resistance under sub-20-nm node [58].

One of the critical issues for NIL is high overlay accuracy. Generally, the current devices now require an overlay of better than 4 nm, 3 σ. For the demanded overlay accuracy, a lot of technology enhancements are required such as the improvement in overlay control accuracy, image placement accuracy and mix-and-match technique. Fukuhara et al. [59] demonstrated that an overlay of 4.5 nm 3 σ and 7.5 nm 3 σ can be achieved for the NIL-to-NIL process

and NIL-to-optical process, respectively, using current NIL tool. They also confirmed the overlay residual of 2.5 nm 3 σ for NIL-to-NIL and 4.5 nm 3 σ for NIL-to-optical. It is very close to the target, but it requires further improvement to meet the future demand. However, the CDU and LER are found to be less than 2 nm [57].

The throughput of a nanoimprint system is influenced by several parameters. One of the contributors is resist fill time. By careful optimization of several parameters (resist drop volume, system controls, material engineering, design for imprint and system controls), fill time can be decreased. It has been reported that throughput per imprint station improved significantly to 15 wafers per hour with a 1.5 s fill time [60]. Now it is targeted at 80 wafers per hour on a four station. One of the major influences of NIL technology is the capability of large-area printing. Large-area patterning with high density and high fidelity has been reported in the earlier reports [61, 62]. For high-resolution large-area patterning, roll-type UV-NIL process with a flexible transparent thin stamp has been proposed [63]. Last few years significant development of a high-speed and large-area roll-to-roll (RTR) and roll-to-plate (RTP) NIL apparatus for large-area patterning of flexible substrates have been demonstrated [64–67].

The effect of the imprinting parameters need to be realized such as temperature, loading force, aspect ratio and imprinting velocity on formability. In addition, it is necessary to optimize the etching process carefully for high-resolution replica fabrication. To accelerate this technology adoption, recently CEA-Leti and EV Group initiated a new program called INSPIRE to diversify the NIL applications beyond semiconductors [68]. Canon also designs nanoimprint lithography tools by collaborating with other vendors and the end users [69].

4.3 Advantages and Disadvantages

NIL is the extremely simple process and offers a promising low-cost alternative lithography technology with some other advantages such as high resolution, CDU and smaller LER. NIL is a fast process. Since it can be used to fabricate nanopatterns at a large scale in a short time, this can be a high-throughput technique. It has also low cost of ownership and high-resolution extendibility. Nevertheless, NIL could offer its 3D patterning capability for the advancement of 3D chip technology. Because of its flexibility and ability to combine with other techniques, it has created huge opportunities for the future lithographic techniques for many others potential applications. However, low overlay structure accuracy and thermal expansion effects are the disadvantages of the NIL. One of the drawbacks of NIL over other nanofabrication techniques is the flexibility of patterning. The mold must be remanufactured when the designed pattern is changed slightly. Another disadvantage is the current reliance on other lithography techniques to fabricate the mold, and the mold fabrication needs lots of money and time.

5 Directed Self-Assembly

5.1 Mechanism

DSA is one of the promising techniques for high-volume low-cost manufacturing at a sub-lithographic resolution. DSA enables finer resolution that attracted a great deal of interest from major semiconductor manufacturers. Recent developments in DSA materials and processing make it compelling next-generation patterning techniques. There are two types of DSA processes: 'epitaxial self-assembly' (Chemo-epitaxy) and 'graphoepitaxy.' In epitaxial self-assembly, dense chemical patterns are employed to direct block copolymer (BCP) self-assembly. Highly ordered nanopatterns can be achieved if the period of the surface chemical pattern is proportionate with the equilibrium period of the BCP self-assembled nanostructure. Graphoepitaxy guides patterning by topographical geometry for DSA. The selective wetting of a BCP component at the trench side walls enforces the lateral ordering of the self-assembled BCP nanodomains along the trenches. Thus, it improves the pattern density by subdividing the topographical pre-pattern. Figure 5 presents the schematic illustration of the two processes [70].

5.2 Status and Challenges

DSA pattern defects, pattern uniformity, pattern placement accuracy, material quality control, cost and ease of integration into manufacturing flows are the critical issues to adopt DSA technology on semiconductor manufacturing. Missing and bridge holes are the typical defect types of

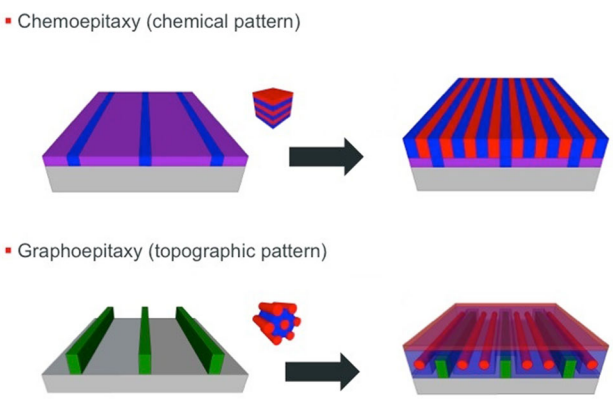

Fig. 5 Schematic illustration of DSA processes [70]

DSA holes in physical guide. Researchers are also focusing on recognizing the factors that are responsible for the assembly defects (dislocations and line-period bridges). The sources for these defects are guide pattern mismatching, particles on the substrate and chemical issues. Missing defects are related to critical dimension (CD) and the surface affinity of the guide pattern, while the dislocation defects are associated with insufficient bake process [71]. Pathangi et al. [72] presented the 14-nm half-pitch DSA line/space patterning into the Si substrate with reduced defectivity. More recently it has been claimed that a dense (pitch 120 nm) contact area superior to 0.01 mm^2 free of DSA-related defects is achieved [73]. Moreover, to improve pattern quality, some experiments have been performed on various etch mask materials and etch process conditions [74].

LER is another challenge of DSA line patterns. For HVM industries, the LER number should be about 10% of the target critical dimension. It has been suggested that optimization of pattern transfer process is one of the effective ways to improve the LER of DSA pattern. By using this method, LER can be improved less than 2 nm [75]. Further improvement is required for the sub-10-nm pattering node. The interfacial length between the two domains has an effect on the LER of DSA lines. Since, it is related to the Flory–Huggins interaction parameter (χ) of BSPs, one solution to improve the LER could be the adoption of BCPs with a higher χ number. However, the high χ block copolymers are still not easily available.

Another issue of DSA of BCPs is the pattern density. Some pattern density enhancement approaches have been proposed including 'thermal flow process,' 'lift-off process,' and 'pattern trimming process' [76–80]. By utilizing a low-topography resist, pre-pattern $\sim$ 5 teradot/in^2 dot arrays with long-range order have been demonstrated [74]. Highly ordered patterns using PS-b-PDMS have been reported in some publications [81, 82]. The minimum feature size is inherently determined by χ of BSPs. High χ BCP, P2VP-b-PDMS has been reported that can generate 6-nm scale line/space pattern [82]. Recently, a research group from the Argonne National Laboratory has developed a new way to create some of the world's thinnest wires using DSA process that could enable mass manufacturing with standard types of equipment [83].

DSA can also integrate bottom-up self-assembly with top-down conventional lithography. It can enhance the capabilities of other lithographic techniques that enable manufacturing at a drastically reduced cost. The probable integration of DSA with ArF immersion photolithography for 16-nm line/space DRAM process scheduled in 2018 [84]. Researchers are investigating the possibility of hybrid DSA processes (combination of both chemo- and graphoelements) which can be possible alternatives for sub-5-nm process nodes. They have the potential to widen the area of applications for DSA. Morita et al. [85] described a low-cost lithography process for making sub-15-nm pattern using DSA on nanoimprinting guide. Developments of several new processes have been reported such as CHIPS flow [86], LiNe process [87], SMART^{TM} process [88] and COOL process [89]. Recently, several application fields for DSA other than semiconductor device process such as flexible/transferable DSA technology utilizing chemically modified graphene (CMG) have been demonstrated [90, 91]. Several DSA consortiums (CEA-Leti, IBM and IMEC) are involved in systematic investigation to integrate DSA effectively into commercial semiconductor process. However, further research will be required on process optimization, perfect defect control, effective pattern transfer and relevant material development to make DSA capable of various commercial device manufacturing as a next-generation lithography solution.

5.3 Advantages and Disadvantages

By DSA, the overall resolution can be increased to a level that is compatible with the 7- and 5-nm logic nodes. DSA could simplify and reduce the process steps. It can ease process integration and provide low-cost processing in advanced semiconductor processes. The other advantages of DSA are reduced defectivity through material and process optimization, increased pattern fidelity, better material quality control at HVM and high throughput. The block copolymers have defects repair tendency in the patterns manufactured by other photolithographic techniques. With this ability, DSA can play a major role in the future of semiconductor fabrication. In addition, required pattern geometries are all possible using designed DSA. By DSA, it is possible to define accurately the orientation, structural dimensions and pattern density. However, in terms of LER and CD control, DSA seems still to be well behind EUVL. Other disadvantages are defectivity, limited pattern types, random orientation and relative long processing time.

6 Comparison and Discussion

Table 2 shows the comparison of the various lithography techniques in terms of resolution size, overlay accuracy, throughput, defect density and cost. Each technique has its own strengths and limitations. Although, these lithography techniques show the promising capability to meet the future demand, they need further improvement in some aspects. They are shown in spider charts in Fig. 6. In terms of resolution, all the next-generation lithography methods have the ability to achieve resolution levels 10 nm and beyond. However, maskless and nanoimprint lithography

Table 2 Comparison of NGL techniques

Parameters	193 ArF [94]	EUVL	Maskless	NIL	DSA
Resolution	10 nm SAQP	< 10 nm [11]	< 5 nm [95]	< 10 nm [69]	< 10 nm [83, 98]
Overlay	< 2.3 nm	< 2 nm [8]	< 20 nm [96]	4.5 nm [59]	< 2 nm [99]
Throughput	> 250 wafers/h	> 150 wafers/h [11]	40 wafers/h [47]	15 wafers/h per imprint station [60]	~150 wafers/h track process with 5 min anneal time [100]
Defect density	< 1 cm^{-2}	< 1 cm^{-2} [8]	< 1 cm^{-2} [97]	< 1 cm^{-2} [57]	~ 0 cm^{-2} [73]
Cost	High	Very High	High	Low	Low

are limited by low throughput. Slow blanking speed is one of the major issues for the EBL system speed and the system complexity let it difficult to improve. In NIL, some factors are responsible for low throughput such as imprint time, mold modification and imprinting process. Large-area patterning may enhance the throughput, but further improvement is needed to meet the industrial requirements. High overlay accuracy is one of the significant issues in NGL techniques. Within 2020, the required overlay is anticipated to be 3–4 nm for DRAM, flash and logic devices [92]. Overlay in NIL has been achieved below 5 nm while tens of nm in maskless lithography. For better overlay accuracy, a lot of technology improvements are required such as overlay control accuracy for tools, the metrology to precisely measure alignment and image placement accuracy.

However, the probability of defects increases with the enhanced resolution. Although, it is difficult to improve defect density due to the contact nature in NIL process, substantial researches are taking place to improve it close to the required value. Along with other issues, defectivity is still the main challenge to DSA implementation to various commercial device manufacturing situations as a NGL solution. In last 2 years, defect density has been improved significantly from 24 cm^{-2} to ~ 0 defect cm^{-2} [73, 93]. Two more orders of magnitude are still needed to meet the industrial requirement of 0.01 defects cm^{-2}. Finally yet importantly, the deciding factor for the lithography techniques is its cost efficiency rather than its technical performance. EUVL infrastructure and tools are costly and large numbers of mask steps required make the technique relatively expensive. Maskless lithography is also costly due to its expensive electronics. On the contrary, NIL and DSA are the promising low-cost techniques for the future patterning nodes.

7 Conclusion

For many years, nanolithography technology has contributed to the advance in the nanomanufacturing industry and is influencing the future of nanoscience and technology. Flexibility, high throughput, high resolution, high reliability, high efficiency and low cost are the requirements for the nanolithography techniques to meet the future demand. Conventional photolithography has been the main lithography technique that meets the current throughput demand for the semiconductor industry but comes with its resolution limit. In the last decade, considerable effort has been made in the development of nanolithography techniques for mass production of integrated circuits. Through this review, an overall status of the potential next-generation lithography techniques has been provided.

- EUVL is expected to be available shortly with high-resolution capability but its adoption in HVM industry remains uncertain. The EUVL infrastructure needs substantial progress including source reliability, LER/LWR improvement and defectivity. More studies are required to develop the issues related to cost of ownership. EUVL can be more cost-effective by enabling new integration schemes through other techniques (planarization, DSA). It can also include multi-patterning (Double expose), LELE process to prepare this technique for next-generation patterning in future.
- Although, EBL and FIBL techniques have high-density ultra-high-resolution patterning capability, patterning speed significantly limits their application within low-volume production. To attain high performance from these techniques, the tool, the resist parameters, and the overall lithography process must be optimized.
- NIL has demonstrated the potentials to achieve the increasing demand for high-volume production. Despite of the huge commercial success, there are still many challenges that lie in NIL fabrication processes.

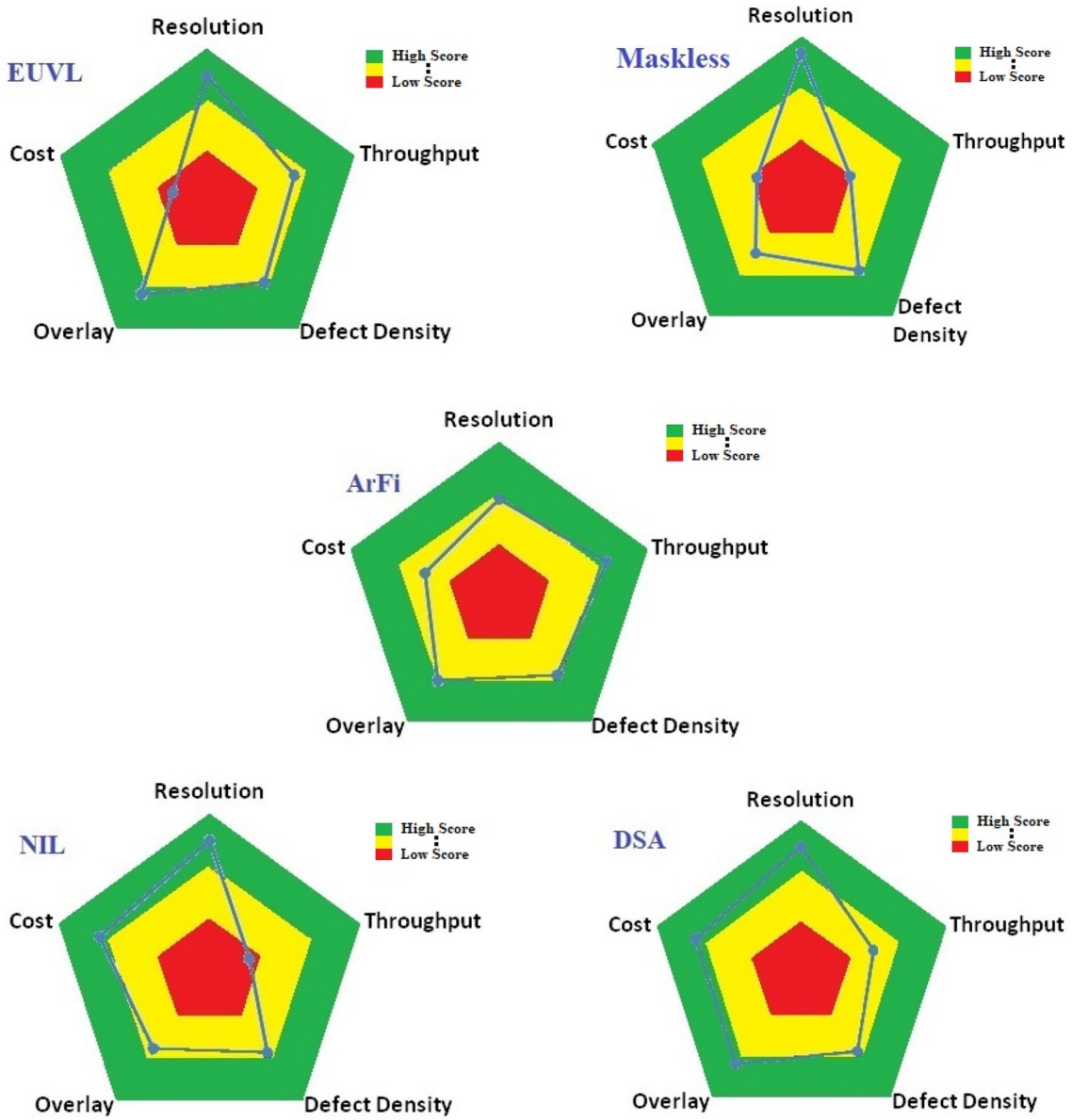

Fig. 6 Spider charts comparing promising NGL techniques

Defectivity and overlay accuracy remains the main concerns and further improvements are required to meet the industrial requirements.

- DSA is considered as a promising patterning option that can reduce multi-patterning strategies. Despite being made satisfactory progress, some issues related to defectivity, placement accuracy and tool design need to be investigated properly. In addition, the challenges of DSA integration into fab flow and designing chips around the technology also need to be addressed before the complete implementation in manufacturing.

All these techniques are still being developed to reach the roadmap requirements and are expected to come across as a novel next-generation lithography technique.

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Rashed Md. Murad Hasan is a Doctoral candidate of DMEM at the University of Strathclyde, UK. He is also an Assistant Professor in Chittagong University of Engineering and Technology, Bangladesh. His research interests include nanofabrication, advanced manufacturing techniques and materials science. He has published numerous articles in peer-reviewed journals and international conferences.

Dr Xichun Luo is a Professor in ultra precision manufacturing and technical director of Centre for Precision Manufacturing at the University of Strathclyde. He is Fellow of the International Society for Nanomanufacturing. His research interests include ultra precision machining, micromachining and nanomanufacturing with more than 100 papers in peer-reviewed journals and international conferences.