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Ultra-high on-current in two-dimensional Tl_2O TFETs with tunneling width modulation

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ABSTRACT Tunneling field-effect transistors (TFETs) have attracted tremendous attention as post-complementary metal oxide semiconductor low-power-dissipation devices. Based on the band-to-band tunneling mechanism, TFETs hold the potential for suppressing the subthreshold swing (SS) below 60 mV dec^{-1}. However, the relatively low on-state current compared with metal-oxide-semiconductor FETs hinders the practical application of the traditional TFETs. Herein, we propose that two-dimensional (2D) Tl_2O possesses a direct and moderate bandgap, small effective mass for electrons and holes, unique threefold degenerate, and strong anisotropic electronic structures, which is suitable for the channel material of the pocket-doped TFETs. Benefiting from the reduced tunneling width led by the pocket, the 2D Tl_2O TFET with a 10-nm gate length possesses an ultra-high on-state current of 3449 μA μm^{-1} with a sub-thermal SS of 49 mV dec^{-1}. Notably, the on-state current increases to 441% compared with no pocket doping and successfully meets the International Roadmap for Devices and Systems (IRDS) high-performance requests for the year 2028. This work demonstrates the great potential of 2D Tl_2O pocket TFETs for next-generation low-power-dissipation and high-performance nanoelectronics.

Keywords: first-principles calculations, 2D materials, electronic structure properties, transport properties, density functional theory

INTRODUCTION

Power consumption has grown to be a serious concern for sophisticated nanoelectronics due to the shrinkage in transistor dimensions over the past five decades [1]. For this reason, tunneling field-effect transistors (TFETs) with the band-to-band tunneling (BTBT) mechanism have been proposed. Sub-thermal switching in TFETs, that is, suppressing the subthreshold swing (SS) below a thermal limit of 60 mV dec^{-1}, could effectively reduce the supply voltage for power dissipation scaling [2]. Nevertheless, due to the BTBT transport, TFETs often have an on-state current that is several orders of magnitude lower than that of metal-oxide-semiconductor FETs (MOSFETs) [3]. Therefore, achieving high-performance TFETs with sub-thermal SS can be a crucial and meaningful challenge for future energy-efficient circuits.

Because of their benefits in reducing carrier scattering and enhancing electrostatic capability, atomically thin two-dimensional (2D) semiconductor channels such as black phosphorene (BP), MoS_2, InSe, $MoSi_2N_4$, and Bi_2O_2Se, have been thoroughly investigated [4–13]. Among numerous 2D channels, 2D BP is particularly noteworthy for high-performance TFETs owing to its superior electronic characteristics and is expected to provide a high on-current exceeding 2000 μA μm^{-1} [14]. On the other hand, the practical applications of BP are inevitably challenged by ambient instability [3]. High carrier mobilities and a direct and moderate bandgap are essential to achieve high-performance TFETs while searching for innovative 2D channels. Recently, monolayer Tl_2O has been proposed as a novel semiconductor with a direct-bandgap and high carrier mobility, which is similar to graphene and MoS_2 in terms of thermal stability and low cleavage energy [15–17]. It is noteworthy to notice that monolayer Tl_2O holds high carrier mobilities for both electrons and holes. This is unique but appealing for high-performance TFET applications, where charges are transported *via* conduction and valence bands. Consequently, it is intriguing to employ the 2D Tl_2O for high-performance TFETs and evaluate its transport performance.

In this study, we comprehensively examine the electronic characteristics and transport performance of monolayer Tl_2O. The results show that 2D Tl_2O possesses competitive electronic properties with a direct and moderate bandgap of 1.02 eV (1.57 eV for HSE06) and small average effective masses for electrons and holes (0.12–0.30 m_0). Notably, the on-state current of the Tl_2O TFET reaches 3449 μA μm^{-1} with a pocket doping adjustment, which is the original 441% in comparison to the pristine device. The superior transport characteristics originate from two aspects. First, the on-current in 2D Tl_2O TFETs is increased to around 1500 μA μm^{-1}, boosted by the high carrier mobilities and multifold degenerate states. Moreover, the pocket optimization shortens the tunneling length to further promote the on-current. Additionally, the modulated band edges also suppress the leakage current and enhance the switching qualities. As a result, with a sub-thermal SS of 49 mV dec^{-1}, the pocket-engineered 2D Tl_2O TFET surpasses the International Roadmap for Devices and Systems (IRDS) high-performance demand with an on-state current of 3449 μA μm^{-1}. Our results reveal that the 2D Tl_2O pocket TFET is a superior alternative for cutting-edge low-power and high-performance circuits.

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CALCULATION METHODS

The geometric optimization of 2D Tl_2O is studied using the Vienna *ab initio* simulation package (VASP) [18,19], based on density functional theory (DFT). The Perdew–Burke–Ernzerhof (PBE) form of the generalized gradient approximation (GGA) is utilized to describe the exchange-correlation interaction. To avoid periodic interaction, a vacuum layer of 40 Å along the *z* direction is adopted. The Monkhorst–Pack *k*-points are set at 15 × 15 × 1. The cutoff energy is 500 eV, and the convergence criteria for energy and force are set to 10^{-5} eV and 10^{-2} eV Å^{-1}, respectively.

The electronic properties and device performance of 2D Tl_2O are calculated using the Quantum Atomistix Toolkit (ATK) package [20], employing the DFT method and the non-equilibrium Green function (NEGF). The state-of-the-art *ab* initio quantum transport simulation combining DFT and NEGF formalism is an accurate theoretical approach for studying carrier transport [21]. The PseudoDojo pseudopotential and GGA-PBE function are applied. The density mesh cutoff is set to 75 Ha. The *k*-grids are sampled with 15 × 15 × 1 and 51 × 1 × 151 for the simulation of electronic and transport properties, respectively. In the transport simulation process, the periodic, Neumann, and Dirichlet boundary conditions are adopted for the transverse, vertical, and transport directions, respectively [22]. In order to obtain the appropriate doping level in the device model, the atomic compensation charge method is utilized to introduce the extra charge [23,24]. The drain current I_{DS} is calculated based on the Landauer–Bűttiker formula. I_{DS} at a given bias voltage V_{DD} and gate voltage V_{GS} is obtained by the following formula:

$$I_{DS}(V_{DD}, V_{GS}) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E, V_{DD}, V_{GS})\}\left[f_S(E-\mu_S)-f_D(E-\mu_D)\right]dE,$$

where $T(E, V_{DD}, V_{GS})$, $f_{S/D}$, and $\mu_{S/D}$ represent the transmission coefficient, the Fermi-Dirac distribution functions for the source/drain, and the electrochemical potentials of the source/drain, respectively. The *k*-dependent transmission coefficient $T_{k//}(E)$ is obtained by the following equation:

$$T_{k//}(E)=\mathrm{Tr}[\Gamma^{S}_{k//}(E)G_{k_{//}}(E)\Gamma^{D}_{k//}(E)G^{\dagger}_{k//}(E)],$$

where $\Gamma^{S/D}_{k_{//}}(E)=i(\Sigma_{S/D}-\Sigma^{\dagger}_{S/D})$ represents the broadening width derived from the source/drain in the form of self-energy $\Sigma_{S/D}$. $G_{k//}(E)$ and $G^{\dagger}_{k//}(E)$ are the retard and advanced Green's functions, respectively. The average of the *k*-dependent transmission coefficient leads to the transmission coefficient $T(E)$. The electrode temperature is set to 300 K.

RESULTS AND DISCUSSION

The monolayer Tl_2O with a hexagonal lattice is optimized based on the DFT calculations, as shown in Fig. 1a. In monolayer Tl_2O, a sandwich structure consists of two layers of Tl atoms and an intermediate layer of O atoms. Each unit cell contains one O atom and two Tl atoms, with the lattice constants $a = b = 3.59$ Å. The orbital-resolved band structure of monolayer Tl_2O is investigated along high-symmetry lines and plotted in Fig. 1b, reflecting a direct bandgap of 1.02 eV. The conduction band minimum (CBM) and valence band maximum (VBM) are

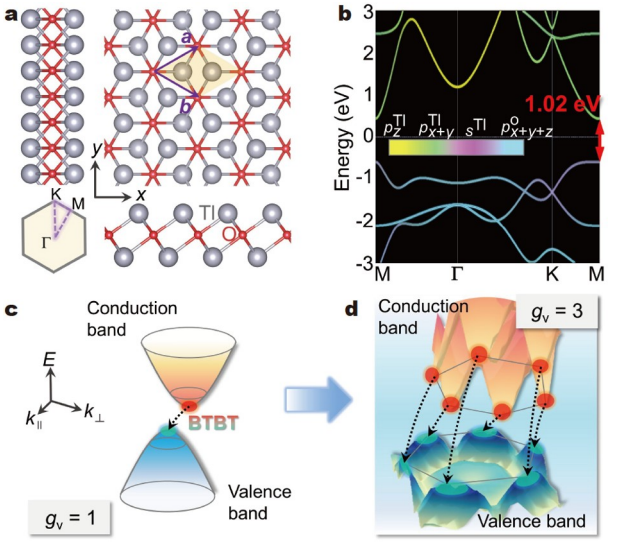

Figure 1 (a) Optimized structure and (b) orbital-resolved band structure of monolayer Tl_2O. The BTBT schematic of (c) a parabolic band channel with valley degeneracy g_v = 1 and (d) monolayer Tl_2O with g_v = 3. The 3D band structure of the lowest conduction band and the highest valence band are plotted in red and green, respectively.

located at the M point. In the monolayer Tl_2O, the CBM is dominated by the Tl p_x and p_y orbitals, while the VBM is composed of the O p_{x+y+z} and Tl s orbitals. Notably, around the CBM and VBM, the energy dispersion exhibits anisotropic properties. The stronger energy dispersion is achieved along the M-Γ direction compared with the M-K direction for both the lowest CB and highest VB. In particular, an almost "flat band" is observed along the M-K direction in the highest VB. Here, the band structure of the monolayer Tl_2O is simulated without considering the spin-orbital coupling effect, which only notably pulled the band in the deep energy level [16].

To better understand the anisotropy of monolayer Tl_2O in the transport process, the contour plots of the energy dispersion are depicted in Fig. 2. The different colors refer to the different energy levels, as displayed in the color bars. Apparently, the CBM and VBM of monolayer Tl_2O are threefold degenerate, since both of them are located at the M point in the hexagonal first Brillouin zone. As shown in Fig. 2a, when transport along the *x* direction, the three valleys possess different energy dispersions. Compared with the valley 1, the valleys 2 and 3 have the weaker energy dispersion and larger effective mass along the *x* direction. Here, the effective mass of electrons and holes along the *x* and *y* directions is summarized in the Fig. 2c. We use the average of the effective mass of the three valleys to evaluate the values along the *x* and *y* transport directions, which are 0.12 m_0 and 0.19 m_0 for the electron, respectively. The values indicate a weak anisotropy in the behavior of electrons. In addition, the hole effective mass exhibits more significantly anisotropic properties when transport in different directions. As shown in Fig. 2b, the "flat band" around the VBM has a prominent impact on the large effective mass along the *y* direction in the valley 1. Then, the average effective mass for the hole is 0.30 m_0 and 3.43 m_0 along the *x* and *y* directions, respectively. Notably, the latter value is eleven times larger than the former. For both electrons and holes, the small values of effective mass are achieved along the *x* direction. Furthermore, the carrier mobilities calculated by

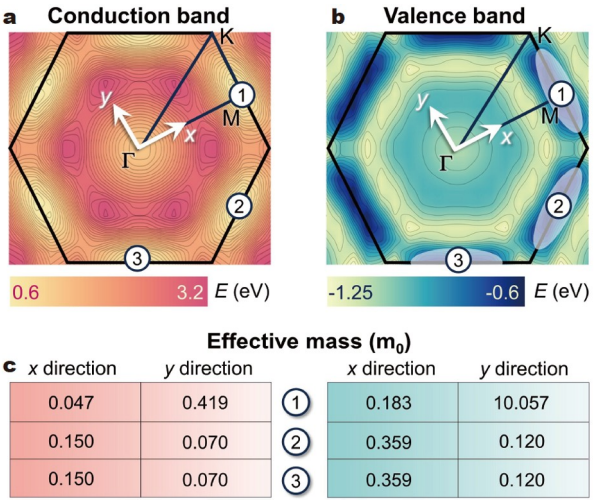

Figure 2 Contour plots of the energy dispersion for (a) the lowest conduction band and (b) the highest valence band in monolayer Tl_2O. The first Brillouin zone is marked with the black solid line. (c) The effective mass (m_0) of electrons (left) and holes (right) along the x and y directions for the three different valleys.

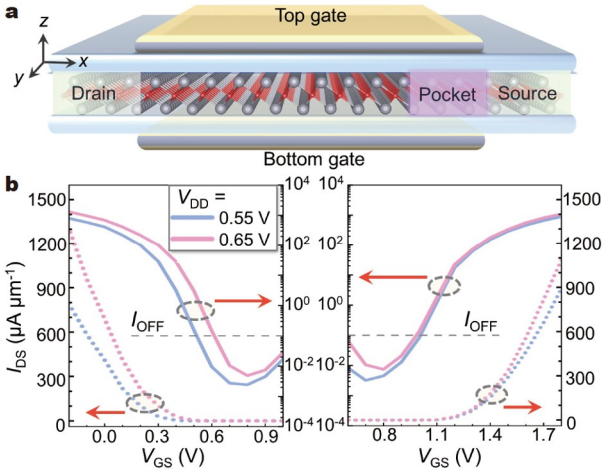

Figure 3 (a) Diagram of dual-gate monolayer Tl_2O p-TFET with pocket. The purple square refers to the pocket engineering region. (b) I-V curves of pristine p- and n-TFETs with supply voltage (V_{DD}) of 0.55 and 0.65 V.

Ma *et al.* [15] exhibit ultra-high values along the x direction for both electrons and holes (3342 and 4302 $cm^2 V^{-1} s^{-1}$). The strong anisotropy of carrier mobilities is similar to BP [15], which also demonstrates excellent potential for carrier transport. Thus, with the direct and appropriate bandgap value, the outstanding and anisotropic electronic properties for both electron and hole indicate the promising application potential for monolayer Tl_2O TFETs [25,26].

Moreover, according to the Landauer formula $I = \frac{2q}{h}\int T(E)M(E)\left[f_S(E) - f_D(E)\right]dE$, the multiple valley degeneracy (g_v) is conducive to increasing the number of modes $M(E)$ and then boosts the current [27]. Unlike a parabolic band semiconductor with g_v = 1, the CBM and VBM of monolayer Tl_2O exhibit threefold degenerate (g_v = 3). Therefore, as shown in Fig. 1c, d, the 2D Tl_2O TFETs are expected to effectively enhance the BTBT through the conduction and valence bands, thereby promoting tunneling current.

Given the significantly high carrier mobilities, the transport properties of 2D Tl_2O TFETs are evaluated along the x direction. Fig. 3a shows the device diagram. Here, the permittivity and thickness of the top and bottom gate dielectric are set to 3.9 ε_0 and 0.5 nm, respectively. The gate length (L_g) of 10 nm is employed for all the Tl_2O TFETs. The doping concentration in the source/drain is optimized to $5 \times 10^{13}/1 \times 10^{13}$ cm^{-2}. The test of different doping levels for the source and drain is shown in Fig. S1. In the p-/n-TFETs, the right/left electrode is selected as the source with n-doped/p-doped. Moreover, unlike the pristine device structure, the pocket configuration is also applied for performance modulation and is located next to the source and under the gate control. The pocket region is p-/n-doped in the p-/n-TFETs, which is opposite to the doping type of the source. The pocket region with a 1 nm length is represented by the purple square, as shown in Fig. 3a.

First, the transfer characteristics of the pristine p- and n-TFETs of monolayer Tl_2O are assessed in Fig. 3b. Here, the on-state current I_{ON} is extracted from the on-state gate voltage V_{GS} (on), defined by $|V_{GS}\text{ (on)} - V_{GS}\text{ (off)}| = V_{DD}$. The off-state current I_{OFF} is always set to 0.1 μA μm^{-1} for high-performance application. Under the V_{DD} of 0.55 and 0.65 V, the I_{ON} of p-TFETs reaches 455 and 782 μA μm^{-1}, while the n-TFETs still maintain good performance with I_{ON} = 385 and 648 μA μm^{-1}, respectively. Benefiting from the threefold degenerate band edges and the small effective mass along the x direction for electrons and holes, the values of I_{ON} at V_{DD} = 0.65 V are competitive in the TFETs case, but the IRDS demand is still too high to reach [28].

With the gated-Esaki-diode (GED) structure, the electric field can be enhanced at the PN junction compared with the NI junction at the source-channel interface in the pristine device. Different from the traditional structure, the channel is fully p-doped, same as the drain electrode. Here, the source is also n-doped at 5.0×10^{13} cm^{-2}. Therefore, the GED structure is employed to improve the device performance. The diagram of the device structure is shown in the insert of Fig. 4a. The channel and drain region are p-doped, with the drain doping concentration (N_D) changing. However, in the 2D Tl_2O TFETs, the improvement has limited contribution to the I_{ON} and SS. In detail, as shown in Fig. 4a, with the doping concentration ranging, the current-voltage (I-V) characteristics only change slightly. With $N_D = 5.0 \times 10^{12}$ cm^{-2}, the transistor exhibits relatively better on-current and SS characteristics, where the I_{ON} increases by 1.4% with a 6.7% reduction of SS compared with the pristine p-TFET.

Compared with the fully doped channel in the GED structure, the shorter pocket doping region (1 nm-length) in the intrinsic channel can be expected to introduce a smaller leakage current. Meanwhile, the PN junction still takes effect and enhances the BTBT near the source. Furthermore, pocket-engineered monolayer Tl_2O TFETs are evaluated with a variation in doping concentration for the pocket region (N_P). As shown in Fig. 4b, with heavier doped pockets, the I_{ON} increases and the leakage current is also reduced. With $N_P = 1.0 \times 10^{14}$ cm^{-2}, the I_{ON} significantly increases to 3694 μA μm^{-1}, far beyond the IRDS high-performance 2028 goal of 1979 μA μm^{-1}. Moreover, as N_P changes from 5.0×10^{13} to 1.0×10^{14} cm^{-2}, the I-V curves alter only to a slight extent, indicating that the lighter doping still leads to excellent device performance. With $N_P = 7.5 \times$

10^{13} cm^{-2}, the device maintains a high I_{ON} of 3449 μA μm^{-1} with SS = 49 mV dec^{-1}. In the following discussion, considering slightly better SS behavior, the pocket TFET is represented by the device with N_P = 7.5 × 10^{13} cm^{-2} at V_{DD} = 0.65 V. Also, the GED-engineered TFET mentioned below implies the device with N_D = 5.0 × 10^{12} cm^{-2} at V_{DD} = 0.65 V.

Based on the IRDS requirement for the year 2034, the device performance should be evaluated under a supply voltage of 0.55 V. Inspired by the superior transport characteristics of the 2D Tl_2O TFETs at V_{DD} = 0.65 V, Fig. 4c scales the V_{DD} to 0.55 V and plots the corresponding *I-V* curves. Here, with GED and pocket structures, the I_{ON} of 483 and 2418 μA μm^{-1} are obtained, respectively. The latter value exceeds the IRDS 2034 high-performance goal of 1504 μA μm^{-1}, demonstrating the potential of the Tl_2O pocket TFETs. In addition, the device performance data of Tl_2O TFETs are summarized in Table S1, and the comparison is shown in Fig. 5a. Using the modulation of GED and pocket, both the I_{ON} and SS behaviors are improved. With the pocket engineering, the I_{ON} increases to 441%–531% while SS is suppressed to 65%–72% of the pristine device.

Besides, considering the underestimation of bandgap through PBE functional, the hybrid functional (HSE06) is employed to assess the transport properties. The band structure of monolayer Tl_2O based on the HSE06 calculation is plotted in Fig. S2. Here, the bandgap value of 1.57 eV is consistent well with the value of 1.56 eV in the previous report [15]. Then, based on the HSE06 calculation, the *I-V* curves of the pristine and pocket 2D Tl_2O TFETs are displayed in Fig. S3. As shown in Fig. S3a, the pristine device exhibits a lower saturation current and I_{ON} due to the tunneling degradation caused by the larger bandgap at the HSE06 level. However, with the pocket configuration, the decrease in saturation current is acceptable and the I_{ON} maintains an ultra-high value of 2371 μA μm^{-1}, as shown in Fig. S3b. In this case, the I_{ON} even approaches 875% of that in the original device. Furthermore, the SS is suppressed by the larger bandgap, resulting in a reduced value of 44 mV dec^{-1}. Hence, the results unequivocally show that pocket configuration is an effective strategy for achieving ultra-high on-current in 2D Tl_2O TFETs.

For a more comprehensive evaluation, Fig. 5b compares the I_{ON} and SS performance of the Tl_2O pocket TFET with other 2D FETs (including TFETs and MOSFETs). Here, I_{OFF} is fixed at 0.1 μA μm^{-1} for high-performance applications. Furthermore, all of the compared data are at the PBE level. As shown in Fig. 5b, the optimal performance region is marked by the square with the blue dashed line in the top left corner. Clearly, the Tl_2O pocket TFET possesses excellent performance with ultra-high on-current and a low SS value below the thermal limit of 60 mV dec^{-1}. More specifically, compared with BP, InSe, Bi_2O_2Se and MoS_2 MOSFETs, the I_{ON} of the Tl_2O TFET is superior with the value exceeding 3000 μA μm^{-1} [29–32]. Meanwhile, the

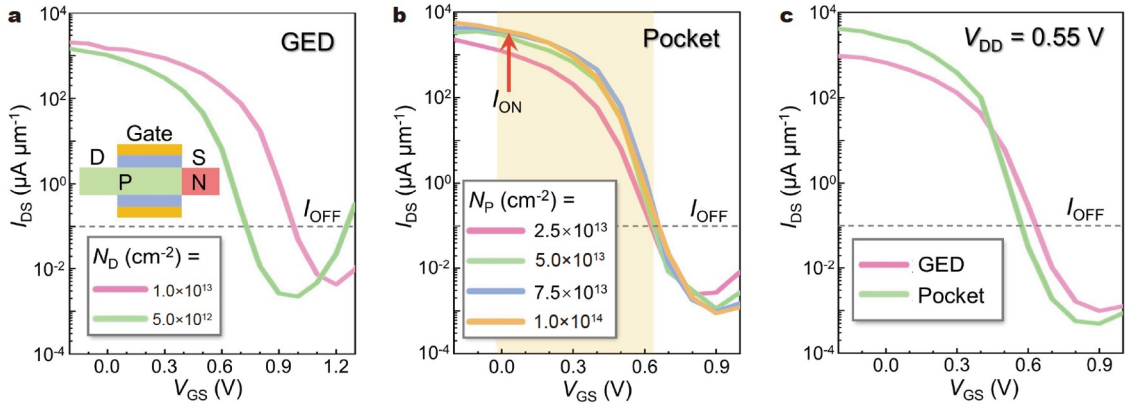

Figure 4 *I-V* curves of 2D Tl_2O p-TFETs with (a) the GED structure and (b) pocket engineering, under varying doping concentration at V_{DD} = 0.65 V. The width of the yellow square refers to 0.65 V. (c) The *I-V* curves of 2D Tl_2O p-TFETs with GED (N_D = 5.0 × 10^{12} cm^{-2}) and pocket (N_P = 7.5 × 10^{13} cm^{-2}) optimization at V_{DD} = 0.55 V.

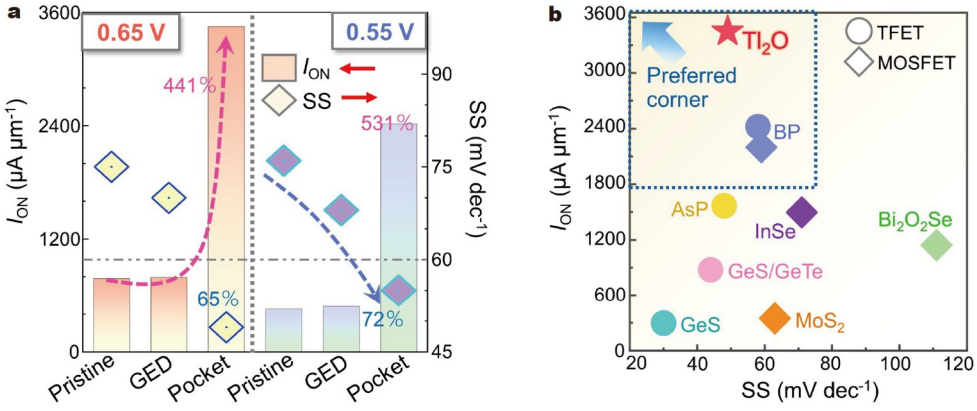

Figure 5 (a) I_{ON} and SS of the pristine, GED- and pocket-engineered 2D Tl_2O p-TFETs. (b) I_{ON} and SS of the pocket-engineered 2D Tl_2O p-TFET (V_{DD} = 0.65 V) compared with other 2D FETs.

SS is comparable to other 2D TFETs for sub-thermal transport [14,33,34].

In order to investigate the enhanced transport behavior in the pocket case, the local density of states (LDOS) and spectral current of the monolayer Tl_2O pocket TFETs are compared with that of the pristine device, as depicted in Fig. 6. The mechanism diagram of the BTBT process is shown in the insert of the right panel of Fig. 6b, and the tunneling window (ΔE) and tunneling length (λ) as two crucial parameters are also marked in the diagram. Here, the heavily p-doped pocket enables an obviously sharper band bending at the tunneling junction, as highlighted with the white dashed square in the right panel of Fig. 6a. In this case, when the TFETs are turned off and $\Delta E < 0$, the pristine TFET bears a larger ambipolar leakage current compared with the pocket TFET because of the shorter λ in the bias window. As shown in Fig. 6b, both types of TFETs are switched on at V_{GS} = −0.01 V, where the tunneling window $\Delta E > 0$. Notably, with a much sharper band bending, the pocket TFET even degrades λ to nearly zero, significantly boosting the tunneling process. Moreover, carriers could transport in two directions at the PN junction near the source to further promote the drain current. As a result, as shown in Fig. 6b, the 2D Tl_2O pocket TFET exhibits a much higher peak in the spectral current when compared with the pristine device. Moreover, the sharper band bending can lead to steeper SS. As shown in the mechanism diagram inserted in Fig. 6b, the sharp band in the pocket TFET and the smooth band in the pristine one are represented by the red and white lines, respectively. Since the red line tends to abruptly switch with the V_{GS} variation, the turn-on frequency is increased at the onset region ($\Delta E \leqslant 2kT$) [35] and the SS can be effectively suppressed. The phenomenon is consistent with the SS of 49 mV dec^{-1} in the monolayer Tl_2O pocket TFET, which is only 65% of the pristine device. Since the upper limit of FETs depends on the intrinsic material properties and modulation strategies, the monolayer Tl_2O possesses outstanding electronic properties for achieving high saturation current, and the pocket effectively promotes the BTBT.

Furthermore, as two key transistor indicators, the power dissipation PDP = $(Q_{ON} - Q_{OFF}) \times V_{DD}/w$ and delay time $\tau = (Q_{ON} - Q_{OFF})/(I_{ON} \times w)$ of the 2D Tl_2O TFETs are also evaluated. Here, Q_{ON}/Q_{OFF} represents the total charge of the channel at on-state/off-state, and w refers to the device width. The PDP and τ of the pristine/pocket TFET are 0.059/0.108 fJ μm^{-1} and 0.116/0.048 ps, respectively, fulfilling the IRDS 2028 requirements of 0.156 fJ μm^{-1} and 0.122 ps. Fig. S4 displays the PDP and τ of Tl_2O TFETs and other 2D FETs [14,30–34]. The energy-delay product (EDP = PDP × τ) is further employed to evaluate the ultra-fast and energy-efficient 2D FETs, as marked by the gray dashed line in Fig. S4. A lower EDP indicates better device performance. The EDP values of 5.18 × 10^{-30}–6.84 × 10^{-30} J s μm^{-1} in Tl_2O TFETs are much lower than the value of 1.90 × 10^{-29} J s μm^{-1} in the IRDS standard. Furthermore, the EDP of Tl_2O TFETs is lower than that of 2D BP and Bi_2O_2Se MOSFETs and comparable to that of 2D AsP and GeS TFETs. The lower EDP value indicates the low energy consumption and fast switching speed ability in 2D Tl_2O TFETs. Accordingly, the above results demonstrate the appealing high-performance 2D Tl_2O TFETs for next-generation transistors.

For practical application, some challenges remain in terms of the ideal band bending at the source-pocket interface and scalable pocket doping region. There are some feasible approaches that can extend the experiment possibilities. First, to form

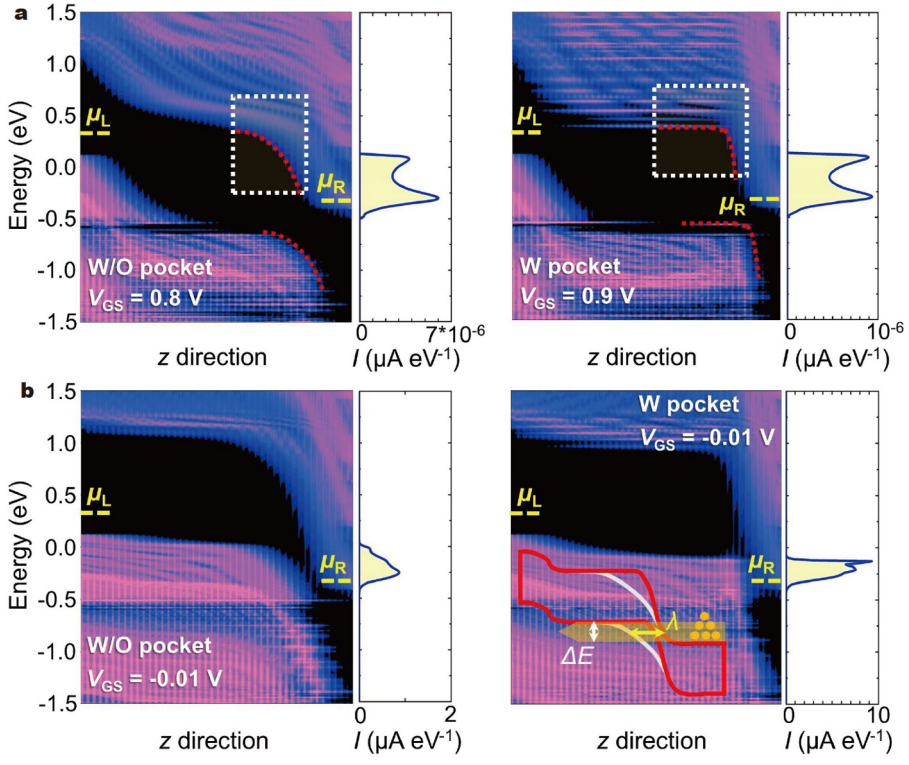

Figure 6 Position-resolved LDOS and spectral current of monolayer Tl_2O pristine (left) and pocket (right) TFETs at (a) the states with minimum leakage current and (b) V_{GS} = −0.01 V.

sharper band bending, experimental and theoretical studies have been proposed to address this issue. For experimental cases, ferroelectric and electrostatic doping can be employed to control the edge of PN junctions, and the doping layer α-$RuCl_3$ and h-BN spacer achieve an ultra-sharp lateral PN junction in graphene [36–38]. According to the theoretical guidance, applying low- and high-*k* oxides, and modulating the contact distance and dielectrics can also sharpen the potential profile [39,40]. Moreover, currently, the surface charge transfer method and a remote doping method have been adopted for the realization of pocket doping [41,42]. Utilizing the edge of graphene and 1D materials can achieve 0.34 and ~1.00 nm contact, which leads to the potential for doping in an ultra-scaled pocket with the electrostatic doping method [43,44]. Other doping methods can be combined with advanced lithography techniques for diverse possibilities [45]. Furthermore, the device performance under 10 and 12 nm for the intrinsic channel with 2 and 3-nm pockets is investigated, as shown in Fig. S5. With the increase in device and pocket length, the performance at the saturation state remains at a very similarly high level. Thus, the pocket-engineered Tl_2O TFETs have great performance potential and higher experimental feasibility with size adjustability for future nanoelectronics.

CONCLUSIONS

In conclusion, we investigate the electronic structure of monolayer Tl_2O and modulate the device characteristics of the 2D TFETs on a 10-nm scale. Our results reveal that monolayer Tl_2O holds a direct bandgap, small effective mass, anisotropic electronic structure, and threefold degeneracy for both electrons and holes. With attractive electronic characteristics and pocket modulation, the Tl_2O TFET surpasses the IRDS high-performance requirement with an on-state current of 3449 μA $μm^{-1}$ and SS reduced to 49 mV dec^{-1}. While achieving the sub-thermal SS, the on-current increases to more than 440% of the original value, suggesting that pocket engineering is a very meaningful strategy for 2D Tl_2O. This work demonstrates the compelling potential of pocket-engineered 2D Tl_2O TFETs for future energy-efficient and high-performance electronics.

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Supplementary information Supporting data are available in the online version of the paper.

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基于隧穿宽度调制的具有超高开态电流的二维Tl_2O隧穿场效应晶体管

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摘要 隧穿场效应晶体管作为后CMOS时代的低功耗器件引起了人们的极大关注. 基于带间隧穿机制, 隧穿场效应晶体管具有抑制亚阈值摆幅低于60 mV dec^{-1}的潜力. 然而, 与金属氧化物半导体场效应晶体管相比, 传统隧穿场效应晶体管的开态电流相对较低, 阻碍了其实际应用. 在此, 我们提出二维Tl_2O材料具有直接且合适大小的带隙, 小的电子和空穴有效质量, 独特的三重简并和强各向异性电子结构, 这适合作为口袋掺杂隧穿场效应晶体管的沟道材料. 得益于口袋导致的降低的隧穿宽度, 栅极长度为10 nm的二维Tl_2O隧穿场效应晶体管具有3449 μA μm^{-1}的超高开态电流, 具有亚热的亚阈值摆幅, 其值为49 mV dec^{-1}. 值得注意的是, 与未实施口袋掺杂的情况相比, 开态电流的值提高到441%, 并且成功满足了国际设备和系统路线图对于2028年高性能器件的要求. 这项工作展示了二维Tl_2O口袋隧穿场效应晶体管在下一代低功耗高性能纳米电子学中的巨大潜力.