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Low-power high-mobility organic single-crystal field-effect transistor

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ABSTRACT **Evolving flexible electronics requires the development of high-mobility and low-power organic field-effect transistors (OFETs) that are crucial for emerging displays, sensors, and label technologies. Among diverse materials, polymer gate dielectrics and two-dimensional (2D) organic crystals have intrinsic flexibility and natural compatibility with each other for OFETs with high performance; however, their combination lacks non-impurity and non-damage construction strategies. In this study, we developed a desirable OFET system using damage-free transfer of 2D organic single crystal, dinaphtho[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene on a unique polymer dielectric layer, poly(amic acid) (PAA). Benefiting from the unique PAA surface nanostructure and the long-range ordered characteristics of the 2D organic single crystal, the resulting OFETs show remarkable performance with high mobility and low operating voltage of 18.7 $cm^2 V^{-1} s^{-1}$ and −3 V, respectively. The result indicates that combining polymer gate dielectric with 2D organic single crystal using a high-quality method can produce flexible electronic devices with high performance.**

Keywords: organic field-effect transistor, polymer dielectrics, 2D organic crystals, high-mobility, low power consumption

INTRODUCTION

The development of low-power, high-mobility organic field-effect transistors (OFETs) offers significant potential for flexible and printed organic electronics [1–5]. Thus, the use of polymer gate dielectrics in a transistor configuration has become the main consideration because of its crucial role in charge transport and operating voltage. Moreover, polymer dielectrics are naturally compatible with both organic semiconductor layers and plastic substrates, thus allowing for a wide range of applications [6–9]. A large variety of polymer materials, such as polystyrene, poly(methyl methacrylate), polyimide (PI), and perfluoro(1-butenyl vinyl ether), have been widely used as the dielectric layer of OFETs [6,10,11], and their significance in enhancing device performance can be attributed to the following: (i) polymer dielectrics commonly have low-*k* characteristics, eradicating dipole disorder that degrades the transistor performance in high-*k* dielectrics [12–15]. (ii) Polymers with designable molecular structures can achieve much lower interfacial densities of defect states than their inorganic dielectric counterparts [16–19]. Combining with the ability to control the thickness of the polymer film, this promising property effectively enables low-voltage operation for OFETs. (iii) The surface properties of polymers can be designed or modified to enhance the ordered packing of organic semiconductor molecules, thus improving charge transport properties. For example, Ji *et al.* [20,21] reported that the self-corrugated nanogrooved structure and the strong polar surface of poly(amic acid) (PAA, precursor of PI) allow more ordered packing of pentacene molecules on their surface to achieve unprecedented mobility.

In addition to the benefits of polymer dielectrics, organic semiconductor crystals are also crucial for obtaining high-performance OFETs because they have minimal impurities, no grain boundaries, and low-density defect states [22–35]. The key task in combining their advantages is to generate high-quality organic semiconductor crystals on a polymer dielectric layer [28]. For example, Li's group developed solution-processable few-layered 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT) crystals on ferroelectric polymer dielectrics with a high mobility of 5.6 $cm^2 V^{-1} s^{-1}$ [29,30]. Jiang *et al.* [31] reported a spatial confinement method for producing n-type monolayer crystals on divinyltetramethylsiloxane-bis(benzocyclobutene) derivative dielectric layer using natural solution volatilization. Furthermore, the monolayer n-type crystal shows maximum electron mobility of 1.24 $cm^2 V^{-1} s^{-1}$, which is a competitive mobility value in monolayer transistors. Zhao *et al.* [32] recently reported that using patterned polymer dielectric layers with different polarities, highly aligned C8-BTBT crystal arrays with uniform crystallographic orientation were facilely assembled in a strong polarity region using solution shearing. However, the challenge of the above studies is not only in the inevitable introduction of solvent contamination for both organic semiconductors and polymer dielectrics because of their vulnerability, but also the lack of single domain characteristics for the grown organic crystals usually plagued by the solution methods. These limitations hinder the pursuit of the ultimate intrinsic performance of OFET devices. Thus, there is an urgent need to construct a desirable OFET system by combining organic single crystals and polymer gate dielectric with low contamination characteristics, which not only lays the foundation for high-performance applications but also benefits the unraveling of the intrinsic physics of OFET devices.

In this study, high-quality two-dimensional (2D) organic crystals of dinaphtho[2,3-*b*:2′,3′-*f*]-thieno[3,2-*b*]thiophene (DNTT) were grown *via* a free-standing fashion using a vapor method, thus making them easily transferable to any target

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substrates. On this basis, an ideal OFET device was constructed *via* the mechanical transfer of the DNTT single-crystal on the PAA surface with minimal contamination characteristics. As expected, an ultra-high mobility of approximately 18.7 $cm^2 V^{-1} s^{-1}$ was achieved for the DNTT, which is the highest value for this material reported so far [36–39]. Furthermore, a low operating voltage of −3 V was required because of the ultralow interfacial defect density of states, making it a promising choice for low-power applications.

EXPERIMENTAL SECTION

Material preparation and 2D organic crystal growth

The p-type organic semiconductor of DNTT was purchased from Luminescence Technology Corp (99%) and was used for crystal growth without further purification. The heavily doped n-type SiO_2/Si with a 300 nm-thick SiO_2 layer was successively cleaned using deionized water, acetone, and isopropanol for 5 min, and then blown dry using a N_2 stream. Physical vapor transport was used to prepare 2D DNTT crystals using ultrapure argon (Ar) as the carrier gas. The sublimation temperature was approximately 240°C. After a few hours of growth, platelet-like, yellow, and extremely thin crystals (less than 100 nm) were obtained. The DNTT crystals were likely to grow vertically on the substrate, allowing the mechanical probe to transfer them. Considerable attention was required while handling the crystals because they were extremely fragile.

Fabrication of PAA dielectrics

PAA was synthesized using the previously published procedure in Scheme S1 [20]. 4,4′-Bis(*N*-phenyl-1-naphthylamino) biphenyl and *N*,*N*-dimethylacetamide were purchased from Aldrich and 3A Chemicals, respectively. Indium tin oxide (ITO)-coated glass substrates was sequentially cleaned by sonication in deionized water and isopropanol for 10 min respectively, and then dried with nitrogen and treated with O_2 plasma (80 W, 10 min). PAA dielectric was deposited on the top of ITO/glass substrates by spin-coating at 2000 r min^{-1} for 90 s. The developed PAA film had an annealing-free thickness of 182 nm and capacitance of 27.5 nF cm^{-2}.

Fabrication and device characterization of OFETs

To fabricate the 2D DNTT-based OFETs, we manually transferred the DNTT crystal onto the PAA dielectric layer using a micromanipulator probe under the observation of an optical microscope. Finally, 200 μm × 40 μm Au stripes were stamped on the DNTT crystal as the source and drain contact electrodes, and then the OFET with a bottom-gate/top-contact (BGTC) configuration based on 2D DNTT crystals was fabricated. The OFETs' characteristics were measured in a clean and shielded box using a micromanipulator 6150 probe station connected to a Keithley SCS 4200. The dielectric constant of PAA can be calculated using the following equation:

$$C_i = \frac{\varepsilon_0 \varepsilon_r}{d}, \tag{1}$$

where ε_0 is the vacuum permittivity, C_i is the unit-area capacitance, ε_r is the dielectric constant, and d is the dielectric thickness.

The carrier mobility, μ, was calculated from the transfer curves in the saturated regime at a drain voltage of −3 V based on the following equation:

$$I_{DS} = \left(\frac{W}{2L}\right) C_i \mu (V_{GS} - V_{th})^2, \tag{2}$$

where I_{DS} is the source-drain current, L is the channel length of the DNTT crystal between the source and drain electrodes, W is the channel width of the DNTT crystal, and the exact values of L and W were obtained from the optical image of the device (Fig. S1). Furthermore, μ is the field-effect mobility, while V_{th} and V_{GS} are the threshold and gate voltages, respectively. C_i is the specific capacitance, which was obtained based on the capacitance of the dielectric layer. The subthreshold swing, SS, which is extracted as the I_{DS} *versus* V_{GS} curve in the subthreshold region, can be expressed as follows:

$$SS = \ln(10)\frac{KT}{q}\left(\frac{C_i + q^2 D_{it}}{C_i}\right), \tag{3}$$

where T is the absolute temperature, K is the Boltzman constant, q is the absolute value of the electron charge, and D_{it} is the interface trap state density.

Instrumentation and test conditions

Plasma treatment was performed using Gala Instrument Prep2. Nikon ECLIPSE Ci-POL polarized optical microscopes with a blue filter were used to analyze optical and cross-polarized optical microscope images. Intelligent mode atomic force microscopy (AFM) was performed using a Bruker Dimension Icon microscope in the tapping mode. Powder X-ray diffraction (XRD) measurements were performed using a Rigaku Smartlab diffractometer in the reflection mode at 45 kV and 200 mA with monochromatic Cu Kα (λ = 1.541 Å) radiation. Transmission electron microscopy (TEM) and selected area electron diffraction (SAED) measurements were conducted using a JEOL 2011F TEM microscope. The 2D DNTT crystal was transferred onto the Cu grid directly for TEM measurement. All electrical characterizations were recorded at room temperature in ambient air using a Keithley 4200 SCS semiconductor parameter analyzer and a Micromanipulator 6150 probe station.

RESULTS AND DISCUSSION

PAA as a gate dielectric with rich polar groups (–COOH and –CONH) has emerged as a promising dielectric material for high-performance flexible OFETs [20]. Because the carboxyl groups pointing out the surface, the PAA dielectric's surface forms a unique corrugated nanogroove structure *via* the strong interaction of hydrogen bonding, and the strongly polar surface can optimize the compatibility between the semiconductor and gate dielectric, which improves film crystallinity, increases domain size, and reduces interface trap density, thus promoting the charge transport performance [20,21]. Meanwhile, high-quality organic semiconductor single crystals effectively enhance OFET device performance. Among the growth techniques of organic crystals, the solution method inevitably introduces defects into the crystal as the solvent evaporates and easily contaminates the carrier transport interface. In this regard, the vapor method is more favorable for producing high-quality organic single crystals, which maximizes the performance of OFET devices [25,40,41]. Because of the possibility of converting the PAA to PI at the high temperature required in the vapor method [20], the single-crystal was fabricated on the PAA dielectric layer *via* mechanical transfer rather than *in situ*

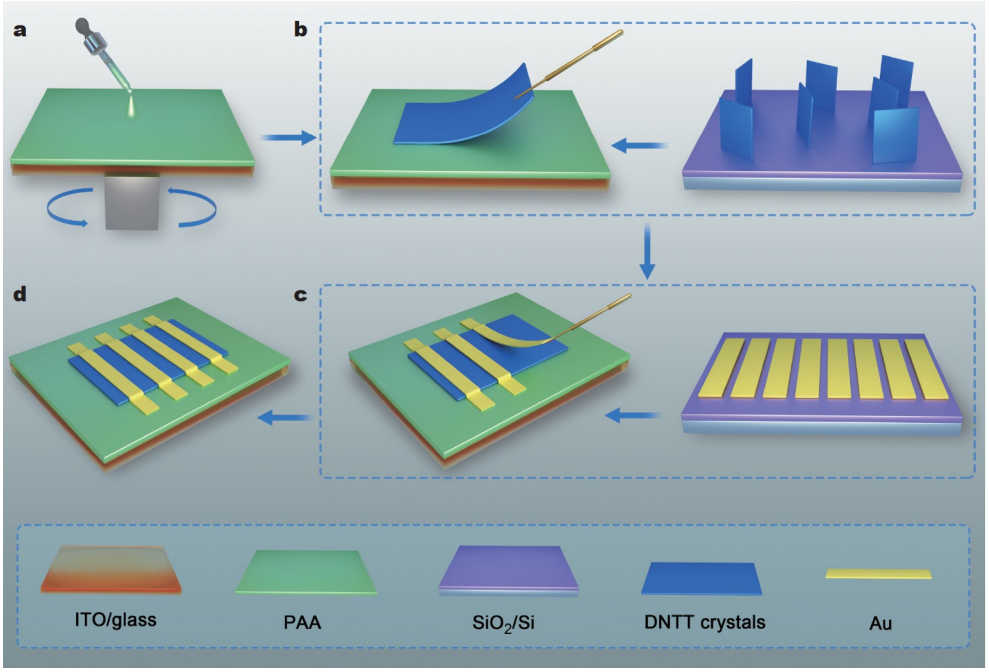

Figure 1 Schematic of the device fabrication process. (a) Spin-coating polymer film of PAA; (b) Transfer of DNTT crystals onto PAA polymer dielectrics. First, freestanding DNTT crystals were prepared on Si/SiO_2 substrates using a vapor growth method. Subsequently, a DNTT crystal was transferred to the PAA substrate using a mechanical probe, which can be achieved by relying on the electrostatic interaction between the probe and the crystal. (c) Transfer of Au strip films onto the DNTT crystal. Au strip films with the size of 200 μm × 40 μm were thermally evaporated on Si/SiO_2 substrate using a shadow mask, and then the Au strip film was peeled off, transferred, and stamped on the DNTT crystal enabled by the mechanical probe. (d) Completed OFET device combining PAA gate dielectrics with DNTT single crystals.

growth. Fig. 1 depicts the fabrication procedure of OFETs (for details, see EXPERIMENTAL SECTION). High-quality single DNTT crystals were first prepared on SiO_2/Si substrates using a vapor method, and then the crystals were transferred onto PAA dielectric layers using a mechanical probe under an optical microscope. Further, Au rectangular films with a thickness of 120 nm were peeled off from the substrate and attached to the DNTT crystal as source/drain electrodes to complete the OFET device.

The quality of the dielectric/semiconductor interface strongly affects the charge transport property [6]. The preparation of pinhole-free and atomic flatness dielectric layers is a prerequisite for the fabrication of high-performance OFET devices. To verify the quality of the PAA dielectric, a smooth surface with a root-mean-square (RMS) of 0.45 nm over an area of 15 μm × 15 μm was achieved as the AFM images show (Fig. 2a), which helped reduce the interface trap density and form a high-quality semiconductor/dielectric interface. Fig. S2a shows the capacitance device based on a sandwich structure of Au/PAA/ITO with an electrode area of 200 μm × 200 μm. The capacitance per unit-area (C_i) of the PAA dielectric layer was measured to be 27.5 nF cm^{-2} at frequencies ranging from 1 kHz to 3 MHz (Fig. 2b). Furthermore, the PAA film was determined by a thickness of 182 nm using AFM height analysis (Fig. 2c, d), which exhibited a low leakage current density of approximately 10^{-8} A cm^{-2} (Fig. S2b). Thus, the dielectric constant can be calculated to be approximately 5.6, which is consistent with previous reports [20]. The results show that we have created a high-quality PAA dielectric layer with atomic flatness and good insulating properties, which is ready for further OFET device fabrication.

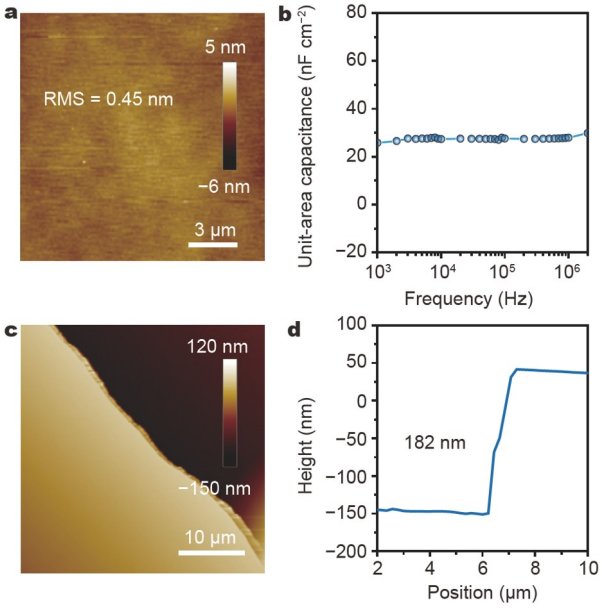

Figure 2 PAA dielectric properties. (a) Surface morphology of the spin-coated PAA film on ITO/glass substrates; the corresponding RMS roughness is 0.45 nm. (b) Frequency dependence of unit-area capacitance for PAA dielectrics, showing a value of approximately 27.5 nF cm^{-2}. (c) PAA thickness used in the capacitor device. (d) Line profile in the AFM image showing a thickness of 182 nm.

Furthermore, the low-defect organic crystal with the highest degree of order is also essential for forming a high-quality semiconductor/dielectric interface. In this study, the organic

semiconductor DNTT molecule is adopted because of its impressive charge transport properties and superior air stability [42], and a vapor-grown method was used to prepare the DNTT into high-quality single crystals because of its solvent-free and purified advantages. A vapor-grown method can efficiently fabricate DNTT crystals into 2D morphologies with freestanding features, which can be easily transferred to the PAA substrate using a probe-assisted technique. Clear and regular boundaries can be observed between the crystal and the PAA surface (Fig. 3a, b), in which the entire crystal displays a uniform color, which indicates its high quality. Furthermore, the DNTT crystal exhibits large lateral dimensions, with the length of 431 μm and the width of 211 μm (Fig. S3). Fig. 3c–f show cross-polarized optical microscope images of 2D DNTT crystals. When the DNTT crystals were rotated according to the polarizer's axis, the color of the entire crystal changed continuously and uniformly from dark to light, indicating the absence of grain boundaries, i.e., the single-crystal nature.

Out-of-plane powder XRD was further performed (Fig. S4) to gain more insights into the crystalline properties of DNTT. A series of narrow and sharp diffraction peaks are observed, which indicates the high quality of the DNTT crystals. Three strong diffraction peaks are located at 2θ = 5.48°, 10.93°, and 16.45°, which could be indexed as (001), (002), and (003) planes according to the single-crystal structure of DNTT (DNTT belongs to the monoclinic crystal system, where a = 6.187 Å, b = 7.662 Å, c = 16.208 Å, α = 90.0°, β = 92.5°, and γ = 90.0°) [42]. All peaks indexed with the (00l) plane family manifest that the DNTT crystal's 2D surface parallel to the PAA substrate is the a-b plane. Fig. 4a–d show the typical bright-field TEM image and the corresponding SAED pattern of a DNTT crystal. The TEM crystal image shows a smooth surface over the selected area. SAED patterns are completely identical at different positions of the crystal, which fully confirms its single-crystal nature. AFM morphology exhibits a flat surface and smooth boundary of the DNTT crystal, which has a thickness of 41.95 nm (Fig. 4e). Fig. 4f shows an RMS roughness of 0.338 nm for the DNTT crystal, which indicates its atomic level flat surface. The trap density of the semiconductor/dielectric interface can be minimized because of the high quality of 2D DNTT crystals. Fig. S5 shows the schematically molecular stacking structure of the DNTT crystal on the PAA surface by combining these characterization results. The DNTT crystal with a herringbone packing motif exhibits CH-π interactions between adjacent molecules in the a-b plane, which serves as the driving force for forming the large-area 2D crystals. Furthermore, the corresponding CH-π interactions in the a-b 2D plane can facilitate charge transport parallel to the substrate direction.

Fig. 5a illustrates the structure of the fabricated OFETs in a BGTC configuration. Fig. 5b, c show the representative transfer and output characteristics of the OFETs. The device exhibits excellent p-type properties, such as a large ON/OFF current (I_{on}/I_{off}) ratio, steep subthreshold swing, and low operating voltage of 10^7, 132 mV dec^{-1}, and −3 V, respectively. Notably, the highest mobility of the OFET device is as high as 18.7 cm^2 V^{-1} s^{-1}, which is extracted from the saturated region, and the average mobility of 15 devices is calculated as 15.5 cm^2 V^{-1} s^{-1} (Fig. 5d). The average values of threshold voltage, I_{on}/I_{off} ratio, and subthreshold swing are 0.24 V, 6.27 × 10^7, and 142 mV dec^{-1}, respectively (Fig. S6 and Table S1). Moreover, the device can withstand temperatures less than 140°C (Fig. S7). High-quality crystals and the related interfacial conditions in OFET structures are the keys to their high-performance; thus, the reasons for obtaining high performance can be attributed to the following three factors: (i) vapor-prepared 2D DNTT crystals have high-quality single-crystal properties, providing the advantages of long-range order, absence of grain boundaries, low density of defect states, and well-defined molecular packing structure. (ii) PAA dielectric with the polar groups (–COOH/–CONH) on the dielectric surface can form a unique corrugated nanogroove structure that can facilitate charge transport performance. To confirm this, the DNTT film was also fabricated on the PAA surface using vacuum thermal evaporation, which exhibited a significantly larger grain size of over 1 μm compared with those reported in the literature (Fig. S8) [43]. Fig. S9 shows the carrier mobility of 8.9 cm^2 V^{-1} s^{-1} for the DNTT thin-film devices, which also outperforms several reported DNTT thin-film OFETs because of the excellent surface PAA properties. (iii) Because of the high-

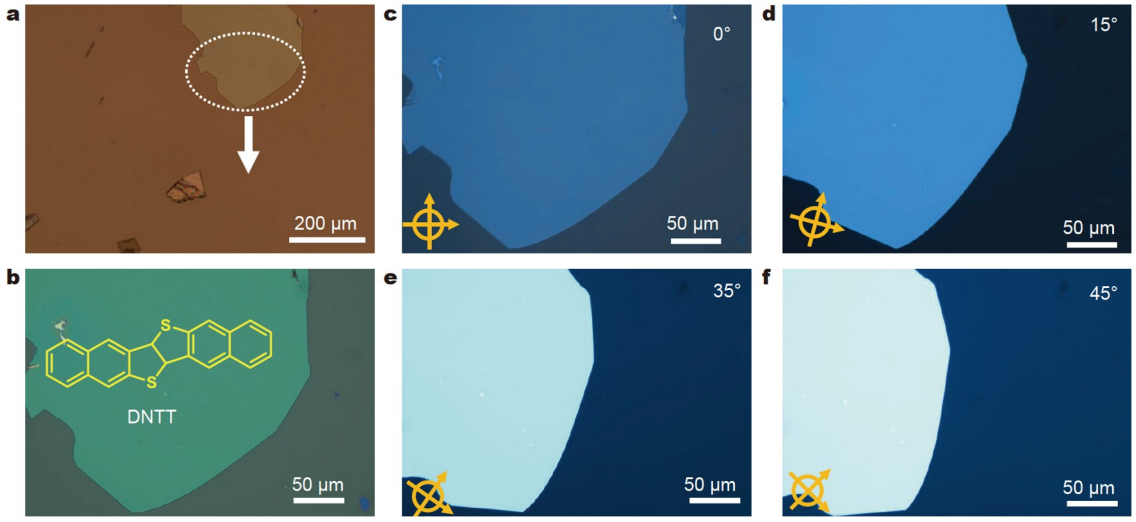

Figure 3 Optical microscopy characterization of DNTT single crystals transferred onto the PAA-modified ITO/glass substrate. (a, b) Optical image of large-sized 2D DNTT crystal fabricated using the vapor growth technique. (c–f) Polarized images of DNTT crystal with different rotation angles to the axis of the crossed polarizers. The large-area uniform color change over the entire crystal confirms the high-quality single-crystal DNTT nature.

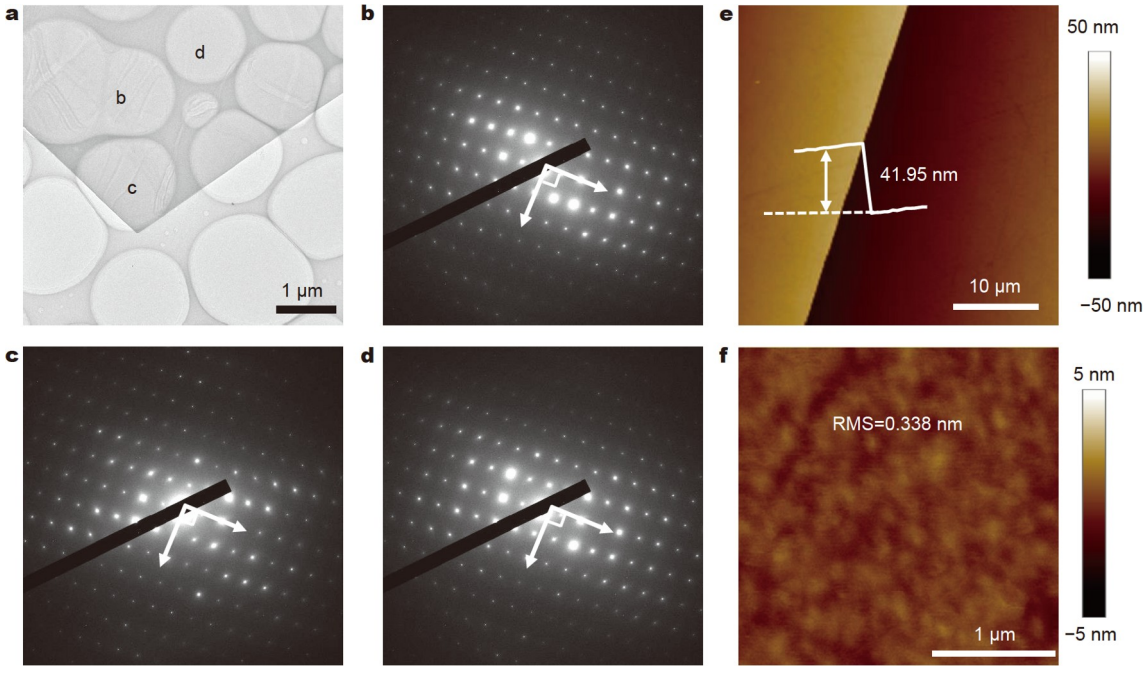

Figure 4 (a–d) TEM image and the corresponding SAED patterns of an individual DNTT crystal, with the identical SAED shown at different parts of the DNTT crystal in (a) confirming its single domain nature. (e) AFM images of a typical DNTT crystal on a PAA substrate with the thickness estimated at 41.95 nm and approximately 50 molecular layers. (f) AFM image of the DNTT crystal surface with an RMS roughness of 0.338 nm.

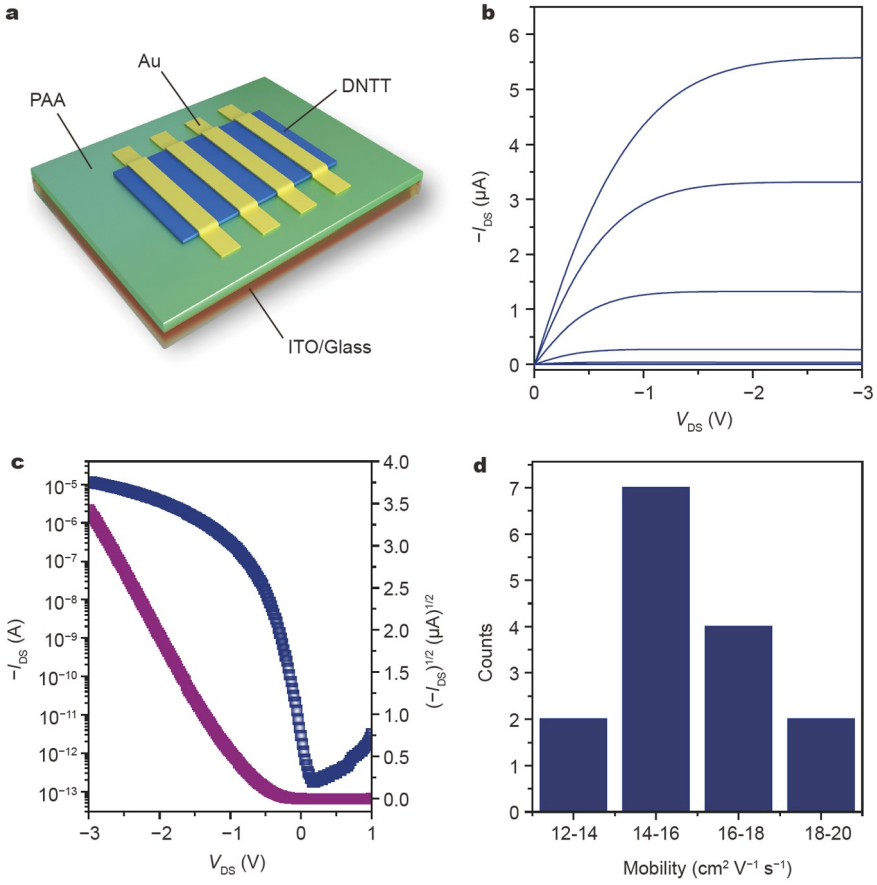

Figure 5 Transistor characteristics. (a) Schematic of the DNTT-based transistor on the PAA dielectric layer with transferred Au (120 nm) films as the source and drain electrodes. (b) Output and (c) transfer characteristics of a typical DNTT-based OFET fabricated on the PAA substrate. (d) Mobility distribution of the OFETs.

quality 2D DNTT crystal, PAA dielectric layer, and their super-clean combination *via* a damage-free transfer technique, an ideal OFET system is created with minimal contamination characteristics and ultrahigh quality semiconductor/dielectric interface, which exhibits negligible hysteresis (Fig. S10). These desirable properties collectively contribute to the high performance of the fabricated OFET devices. Further, we compared the recently reported low-voltage operating OFETs based on DNTT materials in Table S2 [39,44–50]. As demonstrated, the field-effect mobility in our study is significantly higher than that in previous reports. Moreover, the drain current exceeds 1.1×10^5 A with a gate voltage of −3 V, which is one of the highest values of the on-state current in all reported low-voltage OFETs.

Further, device stability is also crucial for achieving OFET-based commercial products. Typical devices suffer from electrical instability because of unavoidable charge trapping at their active layer, dielectric, or interfaces. As expected, the high-quality organic single-crystal combined with extremely low density of interfacial defect states in this study can improve the stability of devices. To verify this, a bias-stressed test was performed for the developed OFETs under realistic electrical conditions. Fig. S11a shows the transfer characteristics of the OFET device under negative bias stress (i.e., $V_{GS} = V_{DS} = -3$ V) for more than 1 h, in which the transfer characteristics of the device before and after stress are almost identical. The threshold voltage exhibits a negligible shift with a characteristic decay time of $\sim 10^3$ s (Fig. S11b), which indicates good device stability. Fig. S11c, d show the relative change of the extracted μ_{sat} and V_{th} over time under the bias stress. It can be seen that the electrical properties are stable under the applied bias voltage. The results show that combining high-quality polymer gate dielectric and 2D organic single crystals is greatly beneficial to achieving highly stable OFET devices.

CONCLUSIONS

In summary, we developed a damage-free transfer method for building an ideal OFET system by combing a polymer gate dielectric with 2D organic crystals. Impressively, the OFET devices display the highest (average) mobility of 18.7 (15.5 $cm^2 V^{-1} s^{-1}$) and a low operating voltage of −3 V. The excellent performance of the OFET device can be attributed to the high quality of 2D DNTT single crystals, the unique surface nanostructures of the PAA dielectrics, and the super-clean combination of the former and latter through the physical assembly. These results indicate that a rational OFET structural design can achieve an increase in device performance, indicating great prospects for future high-performance flexible electronics.

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Conflict of interest The authors declare that they have no conflict of interest.

Supplementary information Experimental details and supporting data are available in the online version of the paper.

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低功耗高迁移率有机单晶场效应晶体管

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摘要 不断发展的柔性电子产品需要开发兼具高迁移率和低功率的有机场效应晶体管(OFET), 这对于新兴的显示器、传感器和标签科技都至关重要. 在众多材料中, 聚合物栅极电介质和二维有机晶体为构建高性能OFET提供了本征柔性和天然的相容性, 但是, 两者的结合仍然缺少无杂质、无损伤的构筑策略. 在此, 我们通过一种无损转移技术将二维有机二萘并[2,3-*b*:2′,3′-*f*]噻吩并[3,2-*b*]噻吩(DNTT)单晶转移到一种独特的聚合物介电层(聚酰胺酸 (PAA))上, 构筑了一个理想的OFET体系. 得益于PAA表面独特的纳米结构和二维有机单晶的长程有序特性, 所得的OFET器件表现出优异的性能, 包括18.7 $cm^2\ V^{-1}\ s^{-1}$的最高迁移率和−3 V的低工作电压. 这些结果说明将聚合物栅极介电层与二维有机单晶高质量结合是构筑高性能柔性电子器件的理想途径.

