SCIENCE CHINA Materials ARTICLES

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Published online 4 December 2020 | https://doi.org/10.1007/s40843-020-1534-2
Sci China Mater 2021, 64(5): 1219–1229

Floating-gate photosensitive synaptic transistors with tunable functions for neuromorphic computing

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ABSTRACT **Synaptic devices that merge memory and processing functions into one unit have broad application potentials in neuromorphic computing, soft robots, and human-machine interfaces. However, most previously reported synaptic devices exhibit fixed performance once been fabricated, which limits their application in diverse scenarios. Here, we report floating-gate photosensitive synaptic transistors with charge-trapping perovskite quantum dots (PQDs) and atomic layer deposited (ALD) Al_2O_3 tunneling layers, which exhibit typical synaptic behaviors including excitatory postsynaptic current (EPSC), pair-pulse facilitation and dynamic filtering characteristics under both electrical or optical signal stimulation. Further, the combination of the high-quality Al_2O_3 tuning layer and highly photosensitive PQDs charge-trapping layer provides the devices with extensively tunable synaptic performance under optical and electrical co-modulation. Applying light during electrical modulation can significantly improve both the synaptic weight changes and the nonlinearity of weight updates, while the memory effect under light modulation can be obviously adjusted by the gate voltage. The pattern learning and forgetting processes for "0" and "1" with different synaptic weights and memory times are further demonstrated in the device array. Overall, this work provides synaptic devices with tunable functions for building complex and robust artificial neural networks.**

Keywords: synaptic device, floating-gate transistor, perovskite quantum dot, tunable synaptic function, optical and electrical co-modulation

INTRODUCTION

With the advent of the "Big Data Era" and the "Internet of Things", various tasks ranging from big data analysis, vehicle autonomous driving, real-time health monitoring to visual and auditory recognition have proliferated worldwide [1,2]. Digital logic computers based on the von Neumann architecture are no longer efficient when processing such large amounts of complex data because it requires complex algorithms, long processing time and huge energy consumption. Fortunately, brain-inspired computing technology has shown the potential for high-speed, low-energy consumption in big data processing and intelligent perception [3,4]. The main idea of brain-inspired computing is to imitate the structure and working functions of the brain [5]. Since synaptic plasticity has been proven to be the physiological basis of brain computing and learning, great attention has been paid to the development of synapse-like devices [6–14].

By using two-terminal non-volatile devices (e.g., two-terminal memristors, phase change memories) and three-terminal/multi-terminal transistors (e.g., floating-gate transistors, electrochemical transistors), synaptic functions have been well mimicked [15–19]. More encouragingly, these synapse-like devices have already made some important advances in data classification [20], machine vision [21], neural prosthesis [22], soft robotics [23], and neural signal analysis [24]. Although significant progress has been made, most of these devices exhibit fixed performance once been made. Synaptic devices with tunable functions are highly desirable for powerful computing systems that can be applied to various scenarios. Recently, several strategies have been developed to adjust the intrinsic synaptic plasticity in fixed materials and device structures. For example, Han *et al.* [25] reported the use of the low-temperature solvent engineering, i.e., altering solvent compositions, to tune the synaptic plasticity of crystallized poly(3-hexylthiophene) (P3HT) nanowire-based synaptic transistors. By adjusting the composition of the co-solvent, it is easy to achieve adjustable synaptic plasticity between short-term and

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long-term on crystalline P3HT nanofiber-based synaptic devices. Kim *et al.* [26] demonstrated artificial synapses composed of 2D, quasi-2D, and 3D halide perovskite film, and investigated the dimensionality-dependent plasticity. By adjusting the dimensionality of the perovskite layer, the retention time can be controlled. However, the method of co-solvent engineering and adjusting the material dimensionality can only be used to adjust the device performance before the device has been made. Li *et al.* [27] reported on floating-gate synaptic transistors capable of accelerated learning through temperature-facilitated synaptic plasticity modulation. Although the temperature can be controlled to achieve dynamic adjustment of synaptic plasticity, it also means that the ambient temperature may affect the device performance. In addition, it is difficult to adjust the temperature for each synaptic device in practical applications.

Herein, we report a floating-gate synaptic transistor with adjustable functions/performance by introducing photosensitive materials as the charge-trapping layer. All-inorganic cesium lead bromide ($CsPbBr_3$) perovskite quantum dots (PQDs) are used as the photosensitive charge-trapping material because of their excellent optoelectronic properties and good environmental stability. The atomic layer deposited (ALD) Al_2O_3 films with precisely controllable thicknesses are utilized as the tunneling layer. The combination of the photosensitive charge-trapping $CsPbBr_3$ PQDs and the Al_2O_3 tuning layer provides the devices with adjustable synaptic plasticity under optical and electrical co-modulation. Light, as another input signal control terminal besides gate voltage, can significantly increase the weight change and meanwhile avoid the deterioration of weight update non-linearity (NL). The memory effect under light stimulation can also be tuned by different gate biases. The pattern learning and forgetting processes for "0" and "1" with different synaptic weights and memory times are successfully simulated in the device array.

EXPERIMENTAL SECTION

Device fabrication

The $CsPbBr_3$ PQD solution was synthesized according to previous report [28]. The charge-trapping layer was fabricated by spin-coating the PQD solution onto a pre-cleaned Si wafer with 300-nm SiO_2 at 3000 r min^{-1} for 60 s, followed by drying under vacuum for 1 h. Then, 8-nm-thick Al_2O_3 tunneling layer was deposited on the top of the $CsPbBr_3$ PQD layer by using ALD technology (Picosun ALD R200), and trimethylaluminum (TMA) and oxygen plasma (O_2) were used as precursor and reactant, respectively. Subsequently, 60-nm pentacene film was deposited by thermal evaporation. Finally, 70-nm Au electrodes were thermally evaporated onto the films through a shadow mask under a vacuum of 8×10^{-4} Pa. The width (W) and length (L) of the device are 500 and 100 μm, respectively.

Material and device characterization

UV-vis absorption spectra and photoluminescence (PL) spectra were taken from a Lambda 750 UV-visible spectrophotometer and an F-320 spectrophotometer (Tianjin Gangdong Sci.&Tech. Co., Ltd), respectively. Dynamic light scattering (DLS) curve was measured by a light scattering instrument (Modulated 3D LS, Switzerland). X-ray diffraction (XRD) spectra were measured by using an X-Ray diffractometer (Bruker Advance D8) with Cu Kα radiation (1.54 Å) at 40 kV. Transmission electron microscopy (TEM) image was observed by an FEI TECNAI G2 S-TWIN F20. Scanning electron microscopy (SEM) images were obtained from a field emission electron microscope (Zeiss SIGAMA HD). The monochromatic lights were provided by Xenon arc lamp filtered with a double grating monochromator (Omno 330150, Beijing NBeT, China) or mounted collimated LEDs (Thorlabs). The transistor characteristics and synaptic functions were measured on a Cascade probe station (Summit 11000M) by using a semiconductor device analyzer (Agilent B1500A) in air at room temperature.

RESULTS AND DISCUSSION

A schematic diagram of the floating-gate synaptic transistor with pentacene channel and Au source/drain electrodes fabricated on p^{++} Si substrate is shown in Fig. 1a. Pentacene is a commonly used organic semiconductor in thin-film transistors and synaptic devices, which exhibits relatively high mobility, simple fabrication, decent stability and low cost [29]. A thermally grown SiO_2 film (300 nm), spin-coated $CsPbBr_3$ PQDs and an ALD Al_2O_3 film (10 nm) were employed as the blocking layer, charge-trapping layer and tunneling layer, respectively. In a certain range (5–15 nm), larger thickness of the tuning layer generally leads to longer retention time, but also higher writing and erasing voltages [30]. The $CsPbBr_3$ PQD solution was prepared according to previous report [28], and characterized by using PL, UV-Vis spectrophotometer, and DLS. The PL and UV-Vis absorption spectra exhibit emission peak and absorption edge both at around 520 nm, indicating the bandgap of the $CsPbBr_3$ PQDs is about 2.35 eV (Fig. 1b). The average size of the

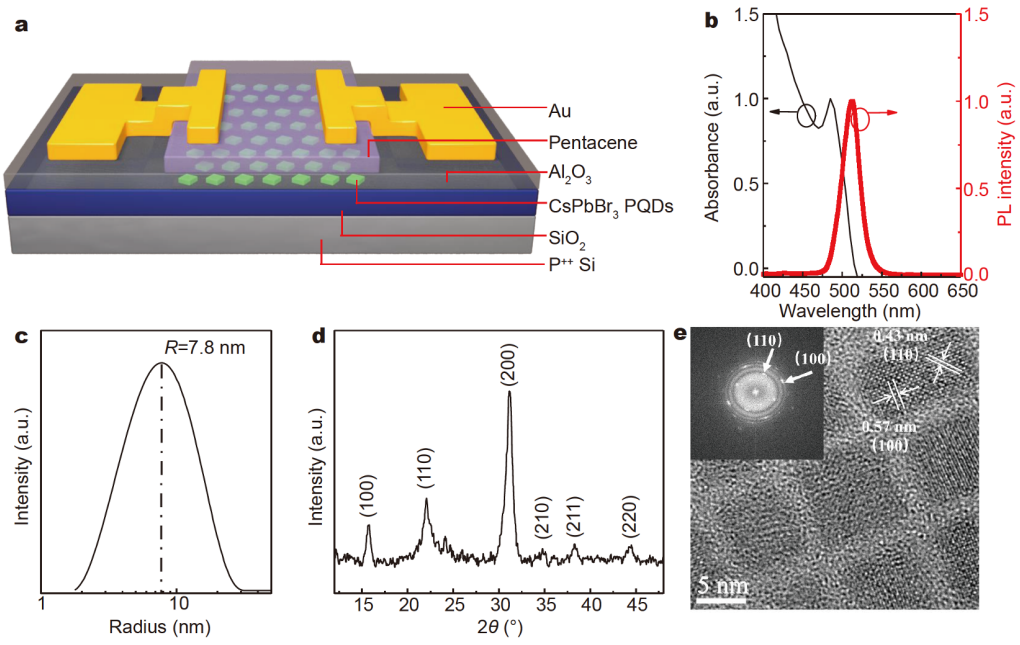

Figure 1 Schematic and characterizations of the device with $CsPbBr_3$ PQDs. (a) A schematic diagram of the floating-gate synaptic transistor with the $CsPbBr_3$ PQD charge-trapping layer and Al_2O_3 tunneling layer; (b) UV-Vis absorption and PL spectra and (c) size distribution of the $CsPbBr_3$ PQDs; (d) XRD pattern and (e) HRTEM image of the spin-coated $CsPbBr_3$ PQD film (inset: electron diffraction corresponding to the selected area).

$CsPbBr_3$ PQDs is 7.8 nm according to the DLS results (Fig. 1c). Then, the charge-trapping layer was deposited by spin-coating the $CsPbBr_3$ PQD solution on the SiO_2 film. XRD was used to investigate the structure of the $CsPbBr_3$ PQDs (Fig. 1d). The diffraction peaks at 2θ = 15.1°, 21.5°, 30.5°, 34.3°, 37.7° and 43.7° correspond to (100), (110), (200), (210), (211) and (220) crystal planes of cubic $CsPbBr_3$ QDs, respectively [31]. The SEM images of the $CsPbBr_3$ PQD layer show well distributed nanoparticles (Fig. S1). Further, the $CsPbBr_3$ PQD layer exhibits highly crystalline cubic structure with an average size of 8 nm, as observed under the high-resolution TEM (HRTEM) (Fig. 1e). The lattice spacings of 0.57 and 0.43 nm observed in the selected area electron diffraction are well corresponding to the (100) and (110) planes of cubic crystal $CsPbBr_3$ PQDs, which further reveals the formation of cubic perovskite phases [32].

The transfer curves (I_d-V_g) and output characteristics (I_d-V_d) of the floating-gate synaptic transistor are presented in Fig. S2a–c. The large hysteresis window observed from the I_d-V_g curve could be attributed to the charge-trapping effect of $CsPbBr_3$ PQDs, because the hysteresis window of the device without $CsPbBr_3$ PQDs is rather small (Fig. S2d). On the other hand, PQDs have been widely utilized to fabricate optoelectronic devices including photosensors [33], photomemories [34] and photo-sensory neurons [8] because of their excellent photosensitivity. In our case, the introduction of $CsPbBr_3$ PQDs is expected to provide the devices with photosensitivity, so that light can be used as another control signal to adjust the device performance. Therefore, the photosensitivity of the floating-gate synaptic transistors was investigated. As the light wavelength was reduced from 530 to 350 nm, the channel current increased significantly, indicating an excellent photosensitivity (Fig. S2c). It should be noted that the photosensitivity of the device is induced by the $CsPbBr_3$ PQD layer instead of the pentacene channel (Fig. S2e and f). Fig. S3a shows the writing/erasing characteristics of the floating-gate synaptic transistor under positive and negative gate voltages. After being written at −20 V/2 s, the I_d-V_g curves showed a large threshold voltage shift (I_d-V_g curve window of 9 V) to the left of the initial curve. However, when a positive voltage pulse of 20 V/8 s was applied to the gate, the I_d-V_g curves exhibited a very limited change, indicating that the device is difficult to erase electrically. With the assist of light (wavelength of 490 nm), the device presented larger threshold voltage shifts in both writing and erasing processes as compared with the only electrical writing/erasing. The above results reveal that the $CsPbBr_3$ PQD layer provides the device with enhanced photosensitivity and photomemory behavior (Fig. S3b and c).

The mechanism of the photomemory behavior is illustrated with the energy band diagram of the device, as shown in Fig. S4.

A biological synapse refers to a specialized structure that transmits the impulse of one neuron to another [35]. The bio-signal processing, learning and memory are established in the human brain through modifying the release of neurotransmitters in synapses. The coexistence of computing and memory in synapses has inspired scientists to imitate synapse functions to overcome the "von Neumann bottleneck" of traditional digital computers [7,14,36–39]. Over the past few years, floating-gate transistors have received extensive attention in mimicking synaptic functions because of their gate controllable channel conductance and nonvolatile memory effect [40–42]. Since our floating-gate device has two control terminals (gate voltage and light), it can realize adjustable synaptic functions, thus providing the possibility of building a robust neural circuit for different application scenarios. To simulate biological synapses, the gate and the channel of the transistors are generally regarded as the presynaptic membrane and postsynaptic membrane, respectively. In our device, both gate and light can be regarded as the presynaptic membrane, while the channel is regarded as the postsynaptic membrane. The channel current or the conductance is defined as the synaptic weight.

We firstly investigated the synaptic performance under electrical signals only. In order to emulate the simple synaptic event induced by the electrical stimulus, i.e., excitatory postsynaptic current (EPSC), a relative positive presynaptic pulse (−15 to −5 V/50 ms) was applied to the bottom gate while keeping the V_{ds} = 50 mV, as shown in Fig. 2a. After the relative positive gate pulse, the current increased rapidly to 18 nA, and then slowly decreased to the initial current, which indicates that a typical EPSC behavior was successfully simulated. Besides, the current with an instantaneous drop followed by a slow recovery, i.e., inhibitory postsynaptic current (IPSC), was similarly realized by applying relative negative pulses (Fig. 2b, −15

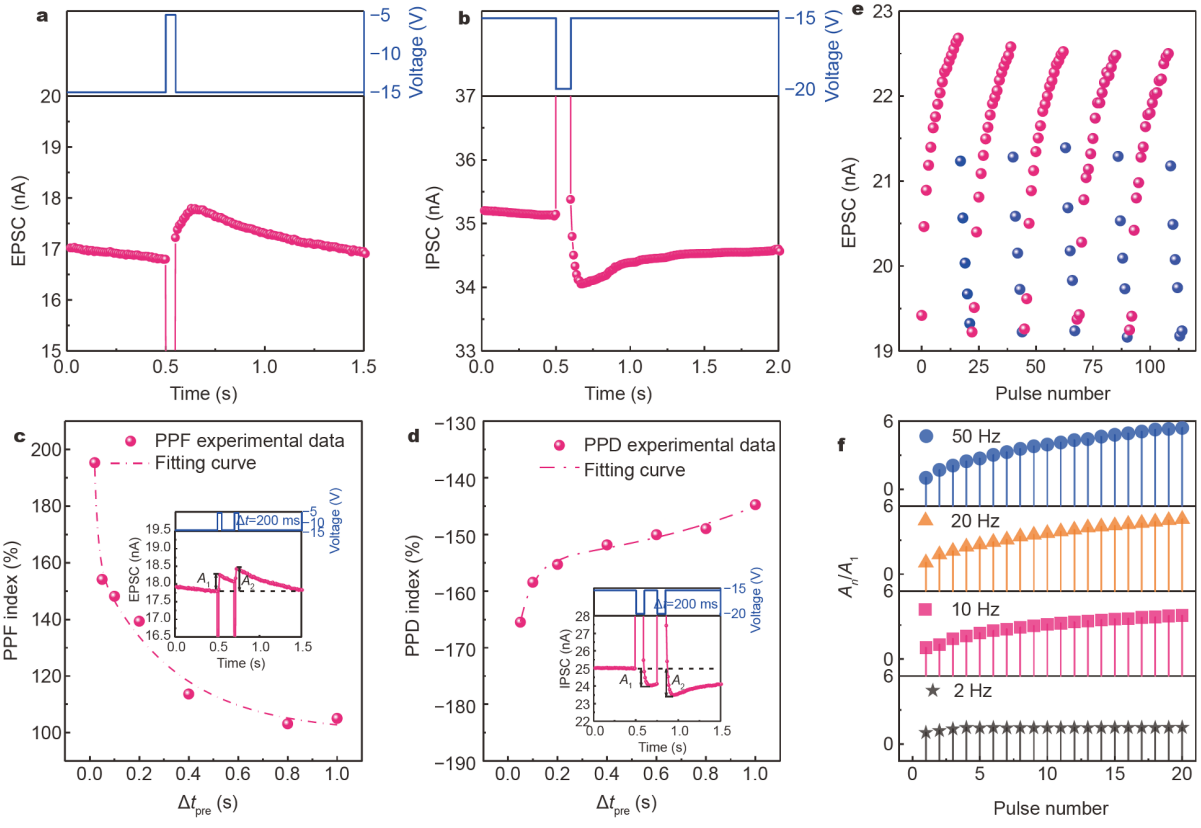

Figure 2 Synaptic behaviors of the device under electrical modulation. (a) EPSC triggered by a relative positive presynaptic pulse (−15 to −5 V/50 ms); (b) IPSC response to a relative negative presynaptic pulse (−15 to −20 V/100 ms). Dependence of the (c) PPF and (d) PPD indexes on interspike interval (inset: EPSC or IPSC generated by two successive presynaptic pulses). (e) The increase and decrease of channel current induced by the continuous and repeated stimuli; (f) dynamic filtering characteristics.

to −20 V/100 ms). Fig. S5 shows the energy band diagram of the floating-gate synaptic transistor under electrical pulse stimulation. At the base voltage V_g = −15 V, the trapped and de-trapped holes will reach a dynamic equilibrium, thus the current remains stable (Fig. S5a). When the relative positive voltage pulse (−15 to −5 V/50 ms) is applied, the equilibrium state is broken, causing extra holes to be transferred from the $CsPbBr_3$ PQD floating-gate to the channel (Fig. S5b). This generates a sharp increase in the concentration of holes in the channel, and thus instantaneously enhances the current (EPSC). After the voltage pulse, the hole distribution in the device would go back to the dynamic equilibrium state, hence the current gradually decreases back to the baseline. The IPSC behaviors under relative negative voltage pulse (−15 to −20 V/100 ms) can be explained similarly (Fig. S5c). Pair-pulse facilitation and depression (PPF and PPD) are typical forms of short-term plasticity (STP). As shown in the inset of Fig. 2c, two consecutive relative positive pulses (−15 to −5 V/50 ms) with an interval of 200 ms lead to superimposed enhancements of the current. The peak value of the EPSC generated by the second voltage pulse is larger than the peak value of the EPSC generated by the first one, indicating a PPF behavior. Similarly, PPD behavior was also mimicked by two consecutive relative negative pulses (−15 to −20 V/100 ms) with an interval of 200 ms, as shown in the inset of Fig. 2d. In order to briefly describe the relationship between the weight change and the interval of two consecutive pulses, the ratio of the amplitude of the second EPSC (or IPSC) (A_2) to the first one (A_1) is defined as the facilitation ratio (A_2/A_1), which illustrates the degrees of weight strengthening and weakening. Thus, the PPF (PPD) index as a function of interval time (Δt_{pre}) was studied, as shown in Fig. 2c and d. Both the PPF and PPD indexes gradually decay as the interval time increases. Generally, the decay of the PPF (PPD) indexes as a function of the pulse interval can be fitted with the following double exponential function [43]:

$$\mathrm{PPF(PPD)} = 1 + C_1\exp\left(-\frac{t}{\tau_1}\right) + C_2\exp\left(-\frac{t}{\tau_2}\right), \quad (1)$$

where t is the pulse interval, C_1 and C_2 are the initial facilitation magnitudes of the rapid and slow phases, respectively. τ_1 and τ_2 are the characteristic relaxation times of the rapid and slow phases, respectively. The well-fitted curve indicates that the biological PPF and PPD behaviors were successfully emulated. Besides, synaptic potentiation and depression were also realized by using numbers of continuous and repeated stimuli (Fig. 2e). The interval between two adjacent stimuli should be much shorter than the time for the charge distribution to return back to the equilibrium state, otherwise no superimposed potentiation or depression will be observed. This behavior can be utilized to mimic the high-pass filter function of the bio-synapse. For the lower-frequency pulses, the current remains almost unchanged. As the pulse frequency gradually increases, the potentiation of the current becomes increasingly obvious, which indicates the ability to filter information by frequency (Fig. 2f).

Then, the effect of light, as another input signal control terminal, on synaptic functions of the floating-gate transistors during electrical modulation was further studied. Fig. 3a demonstrates the EPSCs generated by only the voltage pulse and the light-voltage mixed pulses (light: λ = 490 nm, 250 μW cm^{-2}, voltage: −15 to −5 V/50 ms), respectively. Both the currents presented similarly sharp increase and slow decay, while the EPSC significantly increased from 1 to 15 nA with the co-modulation of the light. Such EPSC enhancement under light co-modulation was found for many different voltage pulses (Fig. 3b). As shown in Fig. 3c, the IPSC induced by positive electrical pulses is also improved with light co-modulation. Fig. 3d summarizes the effect of light co-modulation on both EPSC and IPSC under electrical gate-voltage pulses with different widths, and the EPSCs and IPSCs were increased by light co-modulation for all the cases. This behavior is because that the $CsPbBr_3$ PQDs in the floating gate generate electron-hole pairs under light, hence the positive voltage pulses can transfer more holes from the floating gate to the channel, resulting in larger EPSCs/IPSCs. Then, the effect of light co-modulation on synaptic weight during continuous and repeated electrical modulation was investigated, as shown in Fig. 3e. The current changes generated by light-assisted electrical pulses are larger than those caused by only electrical pulses, whether during weight increase or decrease. The differences in current changes are more significant in the first several enhancements/reductions, and tend to be smaller as the number of pulses increases. The training caused by each pulse will produce different responses to the weight update according to the present weight state. Therefore, the cumulative effect on the weight update (ΔG) does not follow a simple linear relationship. In order to investigate the NL change under the electrical modulation and the light-electrical co-modulation, 50 pulses were applied to induce the increase or decrease of the weights, respectively. The ΔG under different modulations is plotted as a function of the number (N) of the pulses, as shown in Fig. 3f. The change of NL can be quantitatively described

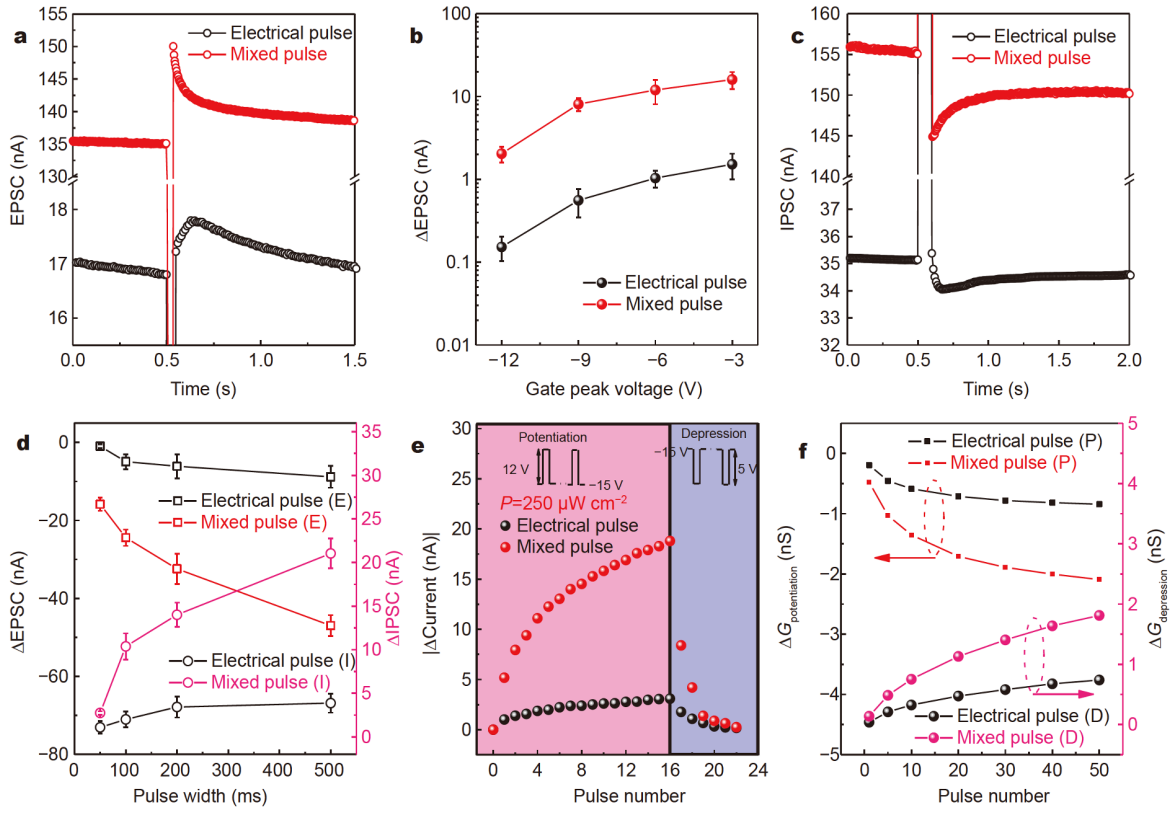

Figure 3 Comparison of synaptic behaviors of the device under electrical modulation only with that under light-assisted electrical modulation. (a) EPSCs triggered by electrical and light-electrical mixed pulses; (b) EPSC changes induced by electrical and mixed pulses as a function of the pulse amplitude; (c) IPSCs triggered by electrical and mixed pulses; (d) EPSC (labeled as E) and IPSC (labeled as I) changes induced by electrical and mixed pulses as a function of the pulse width; (e) current potentiation and depression characteristics induced by continuous electrical and mixed pulses; (f) ΔG generated by electrical and mixed pulses as a function of the pulse number in potentiation (labeled as P) and depression (labeled as D) state. Error bars in (b) and (d) are obtained from five different measurements.

as [41]

$$\mathrm{NL} = \frac{\max\left|G_{\mathrm{p}}(n) - G_{\mathrm{d}}(n)\right|}{G_{\mathrm{p}}(50) - G_{\mathrm{p}}(1)}, \tag{2}$$

where $G_{\mathrm{p}}(n)$ and $G_{\mathrm{d}}(n)$ are the conductance increment and reduction caused by the corresponding pulse ($1 \leq N \leq 50$). The NL values calculated by Equation (2) under 20, 40, and 50 electrical modulation pulses are 0.118, 0.296 and 0.409, respectively. Interestingly, the calculated NL values under the same number of pulses under the co-modulation are 0.080, 0.239 and 0.356, respectively, which are lower than those under the electrical modulation. Thus, the floating-gate photosensitive device shows enhanced degree and linearity of synaptic weight changes under light-electrical co-modulation, which is beneficial for improving the recognition rate in image identification applications.

Moreover, the floating-gate transistors also possess synaptic behaviors induced by only light modulation, which is benefited from the strong light absorption capability of the $CsPbBr_3$ PQDs. Fig. 4a shows a typical EPSC behavior triggered by a light pulse (λ = 490 nm, 100 ms, P = 250 μW cm^{-2}) recorded at constant V_{ds} = −10 V and V_{gs} = 0 V. The inset illustrates that as the light pulse width increases from 50 ms to 20 s, the amplitude of the associated EPSC increases from 50 to 375 pA. The EPSC trigged by the optical stimulus keeps at a stable intermediate value instead of returning back to the initial value after the light pulse. The non-volatile memory effect could be attributed to the floating-gate device structure, and the detailed mechanism is illustrated in Fig. S6a. Optical-stimulated PPF was successfully imitated in the device by applying two consecutive light pulses (Fig. 4b). Further, the "learning experience" functions, including the processes of physiological learning, forgetting, and re-learning behaviors, were demonstrated in the device un-

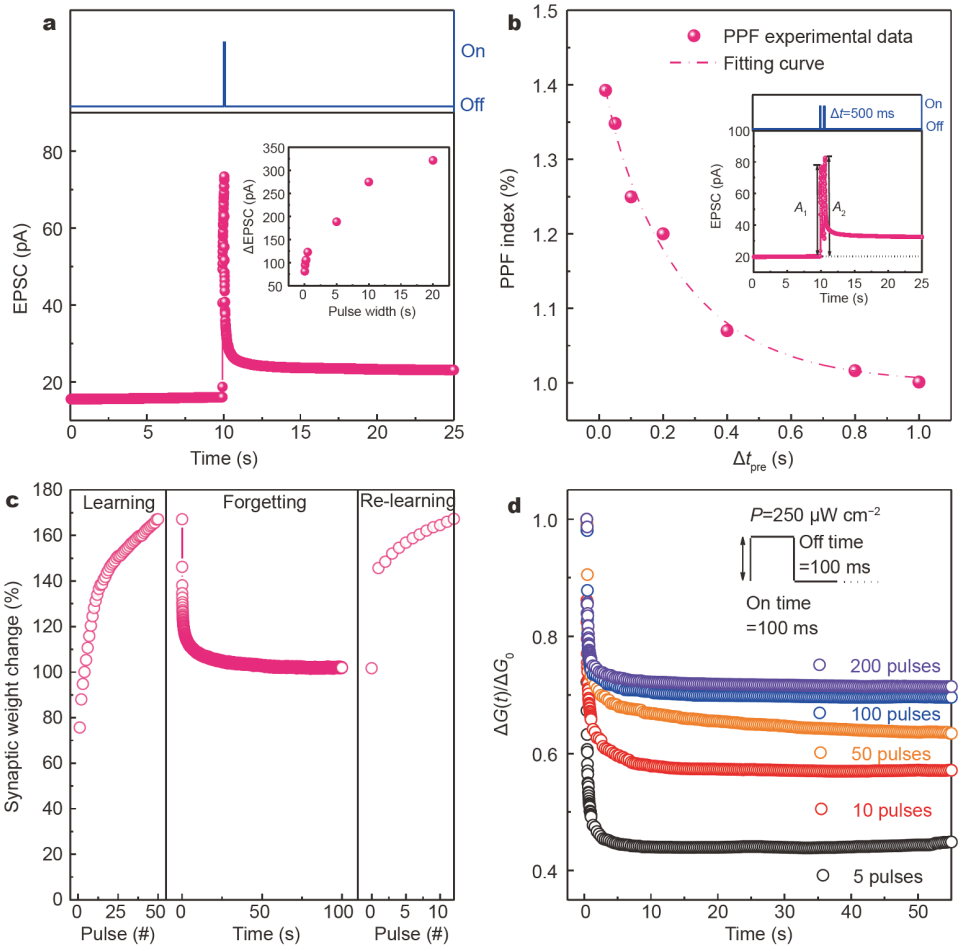

Figure 4 Synaptic behaviors of the device under optical modulation. (a) EPSC triggered by a presynaptic light spike (λ = 490 nm, 100 ms, P = 250 μW cm^{-2}) and recorded at constant V_{ds} = −10 V and V_{gs} = 0 V (inset: EPSC change as a function of the pulse width); (b) dependence of the PPF index on the inter-spike interval (inset: EPSC generated by two successive light pulses); (c) demonstration of learning, forgetting, and re-learning behaviors; (d) decay of normalized channel conductance change ($\Delta G/\Delta G_0$) recorded after the last pulse for various pulse numbers.

der optical modulation. As shown in Fig. 4c, the synaptic weight changes induced by 50 consecutive light stimuli exhibit gradual increase, which refers to the learning process. After the light pulses, the synaptic weight appears an immediate decay firstly and then shows a slow reduction process, which is similar to the behavior of forgetting in human psychology. Interestingly, it only takes 12 same light pulses to increase the synaptic weight back to the preceding level at the second "learning process", which can be considered as the imitation of the "re-learning" behavior. In addition, the forgetting behavior was further investigated with different numbers of light pulses, as shown in Fig. 4d. The final normalized channel conductance change increases from 0.45 to 0.74 as the number of light pulses increases from 5 to 100, namely the memory level improves as the light pulse number increases.

The effect of gate voltage on the synaptic performance of floating-gate synaptic transistors under light modulation was also investigated. Under different gate biases, the device showed different light-stimulated synaptic plasticity, as shown in Fig. 5a. At V_{gs} = −5 V, the normalized EPSC curve eventually returned to the baseline eventually, demonstrating an obvious volatility memory and typical STP. As V_{gs} increased from −5 to 5 V, the end-currents of the EPSC curves increased gradually, and the devices showed a long-term plasticity (LTP) under V_{gs} = 5 V. Fig. 5b illustrates the synaptic weight change as a function of gate bias. At V_{gs} = −5 V, the steady-state weight change is 3% and the fitted decay τ is 2.96 s, while at V_{gs} = 5 V, the steady-state weight change and the fitted decay τ are 63% and 5456 s, respectively. The detailed

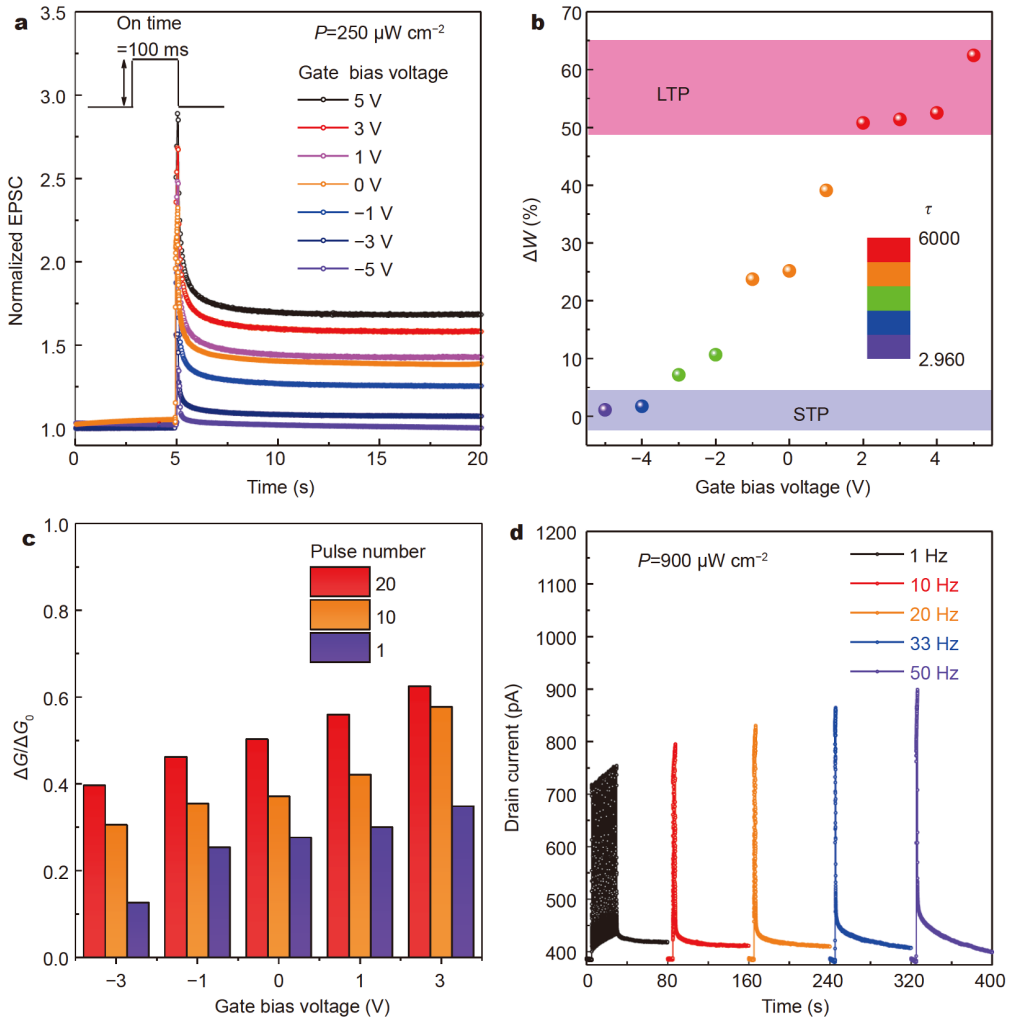

Figure 5 Comparison of synaptic behaviors of the device under optical modulation only with that under gate bias-assisted optical modulation. (a) EPSCs trigged by light pulses under different gate biases; (b) synaptic weight change as a function of gate bias; (c) normalized channel conductance change ($\Delta G/\Delta G_0$) for different pulse numbers and gate biases; (d) EPSC curves (V_{ds} = −10 V and V_{gs} = −5 V) in response to the successive light stimulus (λ = 490 nm, 100 ms, P = 900 μW cm^{-2}, 20 light pulses) with different frequencies.

mechanism is illustrated in Fig. S6b. Therefore, the memory effect of the device under light modulation, from short-term to long-term plasticity, can be adjusted by the gate bias. We further investigated the effect of light pulse number on the normalized synaptic weight change at different gate voltages. In brief, larger light pulse number and higher positive gate bias result in higher steady-state weight changes (Fig. S7). Fig. 5c summarizes the relationship between the normalized synaptic weight change and the gate bias under different light pulse numbers. Apparently, the synaptic weight can be extensively modulated *via* both pulse number and gate bias. A typical dynamic high-pass filtering function under light modulation was also achieved in our devices, as shown in Fig. 5d and Fig. S8.

Finally, a device array was employed to demonstrate the pattern-learning and forgetting processes with tunable synaptic functions under optical and electrical co-modulation (Fig. 6). In a 4×6 device array, gate bias pulses and light-assisted electrical modulation were applied to the devices in the left half part to generate a number pattern "1" (devices labeled as ① and ②, respectively, Fig. S9); while light pulses and gate bias-assisted light modulation were applied to the devices in the right half part to generate pattern "0" (devices labeled as ③ and ④, respectively, Fig. S9). Then, the current changes of the device array as a function of time are plotted in Fig. 6. The left part displays the pattern "1" immediately after the voltage

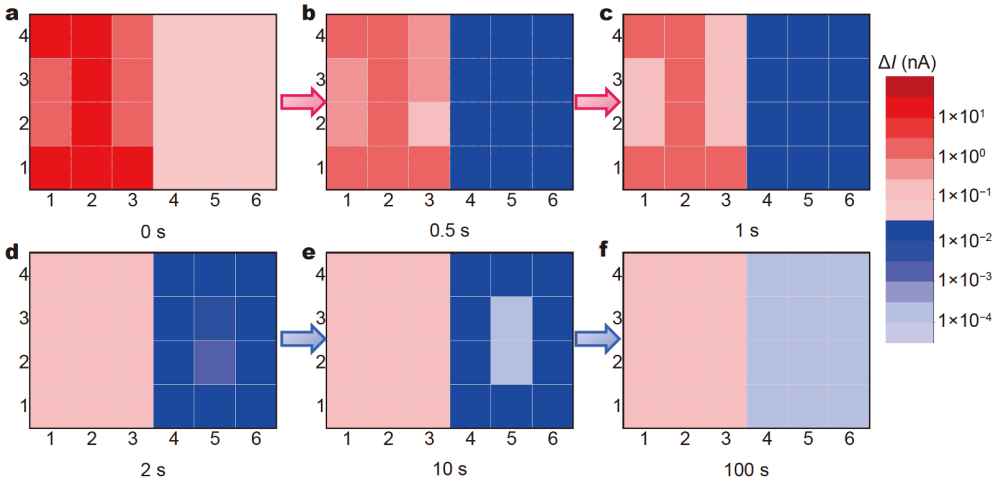

Figure 6 Learning and forgetting processes of the patterns "0" and "1" with different synaptic weights and memory times in the device array under optical and electrical co-modulation. Current changes as compared with the baselines for the device array after the stimulating pulses at (a) 0, (b) 0.5, (c) 1, (d) 2, (e) 10 and (f) 100 s.

pulses, because the light-assisted electrical modulation leads to larger EPSCs for the associated devices. Afterwards, the display of pattern "1" weakens gradually and completely disappears at 2 s, corresponding to STP. In contrast, the right part devices present similar current changes in a short time (around 1 s) after the stimulating pulses. After 2 s, the pattern "0" starts to appear since the gate bias-assisted light modulation provides the devices with higher steady-state current change after the pulses, as compared with the only light modulation. The display of the pattern "0" can last till dozens of seconds, which is associated with LTP. These results thus demonstrate that our device possesses tunable synaptic weights and memory times.

CONCLUSIONS

To summarize, we have reported a floating-gate photosensitive synaptic transistor with charge-trapping $CsPbBr_3$ PQDs and ALD-grown Al_2O_3 tunneling layer. With combining advantages of the ultrathin Al_2O_3 film and the photosensitive $CsPbBr_3$ PQD charge-trapping layer, the synaptic functions of the devices can be extensively adjusted by electrical and optical signal co-modulation. Using light as a modulation terminal can significantly increase the weight change under electrical stimulation while avoiding the deterioration of the weight update NL. Meanwhile, the memory effect under light stimulation can be significantly enhanced by applying gate bias. The device array further demonstrated learning and forgetting processes of the patterns "0" and "1" with different synaptic weights and memory times. Therefore, our device with tunable synaptic functions possesses potential for building complex and robust artificial neural networks.

Received 10 August 2020; accepted 30 September 2020; published online 4 December 2020

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Acknowledgements This work was supported by the National Natural Science Foundation of China (61874029).

Author contributions Wu X and Ding SJ designed the devices and experiments; Li L performed the experiments; Li L and Wu X wrote the paper; all the authors discussed the results.

Conflict of interest The authors declare that they have no conflict of interest.

Supplementary information Experimental details and supporting data are available in the online version of the paper.

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用于神经形态计算的具有可调功能的浮栅光敏突触晶体管

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摘要 将记忆和处理功能整合为一个单元的突触器件在神经形态计算、软机器人和人机交互等方面具有广泛的应用潜力. 然而, 先前报道的大多数突触器件一旦制造出来就表现出固定的性能, 这限制了它们在不同场景中的应用. 在这里, 我们报道了一种以钙钛矿量子点为电荷俘获层、以原子层沉积的Al_2O_3为隧穿层的浮栅光敏突触晶体管. 在电或者光信号的刺激下, 该器件都能展示出典型的突触行为, 包括兴奋性突触后电流、双脉冲异化和动态滤波特性. 进一步地, 器件中高质量Al_2O_3隧穿层和高光敏的钙钛矿量子点电荷俘获层使得其突触可塑性可以在光和电信号的共同调制下实现大范围的调节. 在电调制过程中施加光信号可以显著改善突触权重的变化和权值更新的非线性, 而光调制下的记忆效应可以明显地受到栅极电压的调节. 该器件的阵列进一步展示了对图案"0"和"1"的不同突触权重或记忆时间的学习和遗忘过程. 综上, 这项工作为构建复杂而稳固的人工神经网络提供了具有可调功能的突触器件.

